Design Challenges in Power Handling Techniques in Nano Scale Cmos Devices

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Abstract. VLSI design currently enables us to build million transistor chips. In the current and coming decades VLSI design will become highly complex. Minimization of power consumption is essential for high performance VLSI systems. In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second source of power dissipation comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power will be comparable to dynamic power dissipation. Furthermore, the leakage power shall also become highly significant. High leakage current in nano-scale regime is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modelling of different leakage components is very important for estimation and reduction of leakage power especially for low-power applications. 40% or even higher percentage of the total power consumption is due to the leakage in transistors [2]. This percentage will increase with technology scaling unless effective techniques are introduced to bring leakage under control. This paper focuses on different techniques such as run time and design time techniques are introduced to accomplish power. Handling in nano-scale CMOS devices and provides a detailed overview of these. SPICE results are given for two nano-regime technology nodes.

Keywords: CMOS, Power dissipation, leakage current, multiple Vth, scaling, stacking effect, sub threshold current, tunnelling.

1 Introduction

To achieve lower power consumption, CMOS devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years (3). Supply voltage has been scaled down in order to keep the power consumption under control.

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Types of power consumption in a cmos Circuit
1. Static power consumption
2. Dynamic power consumption

1.1 Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1, Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from Vdd to GND, the resultant quiescent (steady-state) current is zero, hence, static power consumption (Pq) is zero However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate.Total static power consumption (Pst), can be obtained as shown in equation.

$$Pst=\sum(leakagecurrent)\times(supplyvoltage) \quad (1)$$

The leakage current I_d (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices

1.2 Dynamic Power Consumption

For a CMOS circuit, the total power dissipation includes dynamic and static components. In the standby mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage current through each transistor. The dynamic (switching) (P_d) power and leakage power (P_{leak}) are expressed as

$P_d = \alpha f C V^2_{dd}$, $P_{leak} = \sum$ (leakage current) $\times$ (supply voltage)

$$Psc= \frac{kf\tau(V_{DD}-2Vt)^3}{12} \quad (2)$$

where α is the switching activity is the operation frequency is the load capacitance, V_{dd} is the supply voltage, and I_{leak} is the cumulative leakage current due to all the components of the leakage current .leakage current (power) increases dramatically in the scaled devices. Particularly, with reduction of threshold voltage (to achieve high performance), leakage power becomes a significant component of the total power consumption in both active and standby modes of operation.

Total power consumption is the sum of static and dynamic power consumption.

$$P = (C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f) + V_{DD} I_{leak} \quad (3)$$

As technology is scaling down dynamic power consumption is reducing absolutely and static power is increasing relatively. Reports indicate that 40% or even higher percentage of the total power consumption is due to the leakage of transistors.

2 Consequence of Scaling is Short Channel Effect

a. Threshold Voltage Variation (Threshold roll-off)
b. Mobility Degradation
c. Drain-Induced Barrier Lowering

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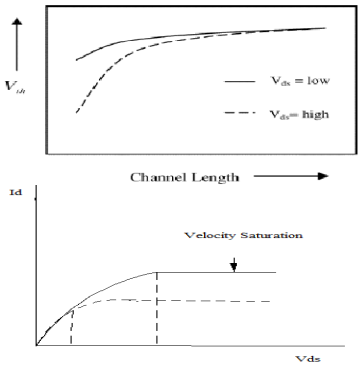
2.1 Threshold Voltage Variation (Threshold Roll-Off)

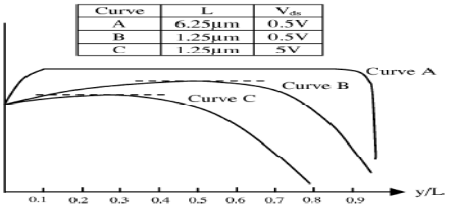
V_{th} lowers as length decreases.This is because depletion region associated with S/D region protrude into the channel area considerably thereby reducing the immobile charge that must be imaged by the charge on the gate.



Mobility Degradation with Vertical Field: At large gate to source voltage, the high electric field developed between the Gate and channel confines the carrier to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility.

2.2 Drain-Induced Barrier Lowering

It becomes lower when high drain voltage is applied to a short channel device, the barrier height is lowered even more, resulting in further decrease of the threshold voltage.



2.3 Types of Leakages in MOS for NANO Regime

Reverse bias current, Sub threshold leakage current, Gate oxide tunnelling leakage, hot carrier injection leakage; Gate induced drain leakage and Punch through leakage.

Design time techniques	Run time techniques	
	Standby leakage reduction	**Active leakage reduction**
Dual V_{th}	Natural Stacking , Sleep Transistor, FBB/RBB	DVTS

3 Runtime Techniques

A common architectural technique to keep the power of fast, hot circuits within bounds has been to freeze the circuits place them in a standby state any time they are not needed. Standby-leakage reduction techniques exploit this idea to place certain sections of the circuit in standby mode (low-leakage mode) when they are not required.

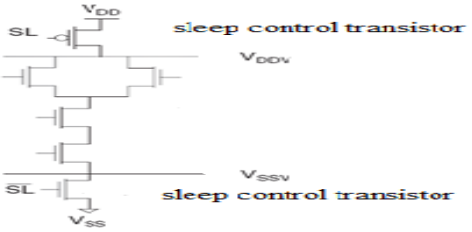


Fig. 1. MTCM (Ref 3)

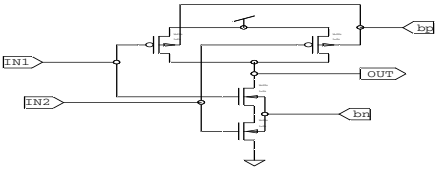


Fig. 2. VTCMOS

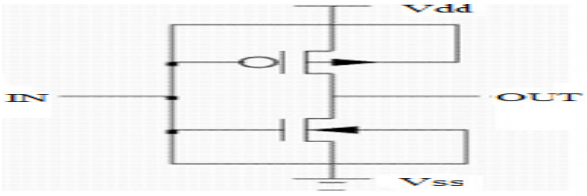


Fig. 3. DTCMOS (Ref 1)

3.1 Multiple Threshold Voltage CMOS (MTCMOS)

This technique inserts an extra series-connected (sleep) transistor in the pull-down/pullup path of a gate and turns it off in standby mode. The extra transistor is on during normal operation. This provides a substantial savings in leakage current during standby mode this technique is only usable for non critical paths. The stacking effect is best understood by considering a two-input NAND gate as shown in Fig.4. When both (M1) and (M2) are turned off, the voltage at the intermediate node (Vm) is positive due to small drain current. Positive potential at the intermediate node has three effects.

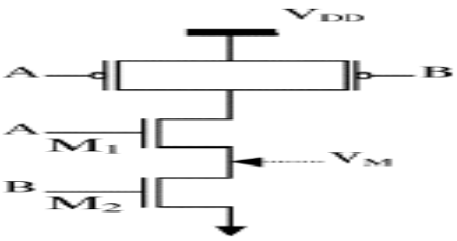


Fig. 4. Stacking Effect (Ref 3)

Variable Threshold CMOS (VTCMOS): It is a body-biasing design technique to achieve different threshold voltages; this scheme uses a self-substrate-bias circuit to control the body bias. In standby mode, it applies a deep reverse body bias (RBB) to increase the threshold voltage and to cut off the leakage current.

4 Experimental Results

Simulation analysis has been carried out for NAND gate for two technologies i.e. 180nm and 350nm. SPICE simulations results obtained are given in Tables 1 and 2.

Table 1. Leakge power for NAND gate in 180nm technology

180nm	Conventiona lNAND	VT CMOS	Stacking effect	MT CMOS
Leakage power	13.82uW	0.140uW	7.0866nW	3.3944Pw

Table 2. Leakage power for NAND gate in 350nm technology

350nm	Conventional NAND	VT CMOS	Stacking effect	MT CMOS
Leakage Power	14.07uW	66nW	0.48nW	3.75pW

From the tables1 & 2, Leakage power reduces with VT CMOS (body bias) Technique appr.10 times reduction, with transistor stacking effect Technique appr.1000 times Reduction, with MTCMOS(sleep transistor) Technique appr.10000 times reduction is possible.

5 Conclusion

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. In current Nano regime CMOS devices with low threshold voltages, sub threshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. Design time techniques and Run time techniques such as Dual vth, MTCMOS, VTCMOS and Dynamic Vth scaling can effectively reduce the leakage current in high-performance logic.

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