Design and Implementation of 4-bit High Speed Array Multiplier for Image Coding

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Abstract. Multipliers are the utmost commonly used elements in today's digital electronics. In digital signal processing systems, hardware multiplication is critical for obtaining high data throughput. Based on the increasing applications of electronic devices, various types of multipliers have emerged. Array Multiplier is the most fundamental multiplier of all. The main goal of our project is to create an optimized and fast 4-bit array multiplier. Parallel Array Multipliers are used in DSP applications to do multiplication at high speeds while meeting performance criteria. The simulations are run on the Xilinx 14.7 ISE Design Suite.

Keywords: Critical Latency · Array Multiplier · Propagation Latency · Power · Area · Speed

1 Introduction

Many digital signal processing applications and operations are performed by multipliers. Researchers have primarily focused on design factors to improve the performance due to advancements in present technologies. There are a variety of computation blocks in DSP processors, such as multiplexers, adders, and MACs. These goals are aimed at achieving high speed, accuracy, low power consumption, and layout regularity. When compared to previous versions, the speed of operation of these blocks has increased. Generally, multipliers are executed at different speeds depending on the semiconductor technology and multiplier architecture.

Literature Survey

Various multipliers are discussed in this article [1] through Array Multipliers, Constant Coefficient Multiplications, and Vedic Multiplications. A multiplier employs arrays of full adders and half adders to multiply two binary values. A set of AND gates is used to eliminate the partial product terms [2]. The hardware construction of a * b bit multiplier is given by (axb) AND gates (a-1). b adders. In this case, there are b half adders and (a-2). b full adders. The array multiplier does multiplication in the standard manner. It

S. Nandan Mohanty et al. (Eds.): ICISML 2022, LNICST 470, pp. 382–389, 2023.
https://doi.org/10.1007/978-3-031-35078-8_32

resembles a regular structure. As a result, wiring and layout are simplified to a great extent. In an array multiplier, the add and shift algorithm is used. It is simple to implement, but a large area is required and a significant amount of time delay [3]. Since RCA is the slowest adder when compared with other adders accessible. Carry Save is used to add partial products, while RCA is used for total summation in CSA multipliers. The addition of partial products in CSA multipliers is done in Carry save form, while RCA is only used at the end of the process for summing the products. There is no need to wait until all of the partial products are generated before summing them in this approach. The addition of partial products is possible as soon as the partial products formed [4]. This multiplier has the significant advantage of being a daily structure. Another benefit of the array multiplier is that it is easy to implement in a pipelined architecture. The size of the array multiplier is a significant restriction. Arrays develop at a rate proportionate to the squares of the element size as the component size grows. It is classified as a traditional multiplier. After the chip area, one of the primary important design goals in the development of an integrated circuit for any embedded system is power dissipation. Power loss in every automated device is equivalent to the number of changeovers. Signal Processing Units frequently use switching procedures. The multiplier unit is the most fundamental component of a signal processing circuit. Because the speed and throughput rate of a signal processing system are always important factors, a high speed and low power multiplier unit is perfect for every signal processor unit. Because speed and throughput rate are always considerations of a signal processing system, a high speed and low power multiplier unit is ideal for every signal processor unit. Low power circuits have become prominent in today's world due to the rapid expansion of portable electronic systems such as desktops, laptops, calculators, and mobile phones. For a VLSI designer, low-power and high-throughput circuitry design are critical. A high-speed and high-throughput multiplier unit is always a cornerstone to achieving a high-performance Signal Processing system in real-time signal processing. In a computational unit of an electronic system, multipliers dissipate a substantial amount of power. Multiplication, at its most basic, is an abbreviated process of adding an integer to itself a specified number of times [6]. To generate a result, a number i.e. the multiplicand is multiplied by another number-multiplier a certain number of times (product). To recapitulate, multiplication comprises of two essential operations: the formation of partial products and the accumulation of those products. As a result, there are two options for speeding up the multiplication: reducing the number of partial products or accelerating their accumulation. A lesser number of partial products reduce complexity and, as a result, the time it takes to collect the partial products decreases. Both solutions can be used at the same time [7]. In the Central Processing Unit (CPU) of microprocessors and microcontrollers, most signal processing applications, such as convolution, Fast Fourier Transform (FFT), and filtering, use multiplication-based processes. The suggested research work's main aims are to develop different multiplication architectures and methodologies that reduce power dissipation, enhance operation speed, and/or reduce area. The array multiplier derives its name from the multiplication parallelogram. Some partial product inputs should be provided to each level of the parallel adders. The carryout is carried over to the next row. The multiplier's crucial path is indicated by the bold line [8]. All partial products are generated at the same time in a non-pipelined array multiplier. The critical

path is seen to have two parts: vertical and horizontal. In terms of full adder and gate delays, both have the same delay. The vertical and horizontal delays of an n-bit by n-bit array multiplier are identical to those of an n-bit complete adder.

2 Proposed Design

Figure 3 depicts a schematic of the proposed 4 * 4 array multiplier. The add and shift technique is used to model the proposed circuit. The proposed structure consists of full adders, gates, and half adders. There are three key steps in the multiplication algorithm. i) Generation of partial products ii) Reduction of partial products. iii) Summation. The following is the multiplication algorithm for an N-bit multiplier: In the Fig. 2 we have given procedure of multiplication process. By sharing tasks among a large number of computing nodes (virtual machines), the cloud provides users with access to computing power on par with supercomputers. Performing a task efficiently requires a certain number of computing nodes that users may not be aware of. As a result, under provisioning and over provisioning occur frequently. The proposed schematic for 4-bit array multiplier is as shown in the Fig. 1 below

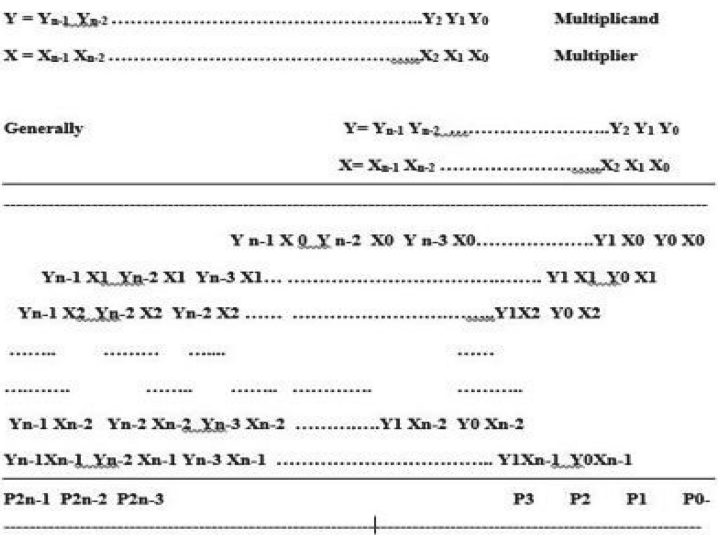

Fig. 1. 4-bit array multiplier

Multiplicand - M bits; Multiplier - N bits Partial Product-M * N bits

Steps in Multiplication:

If the Multiplier's LSB is '1'. The multiplicand is then added to an accumulator, with the multiplier bit changed to the right and the multiplicand bit shifted to the left.

Stop when the multiplier's bits are all zero.

When partial products are added serially, less hardware is needed.

A parallel multiplier can be used to add all of the partial products

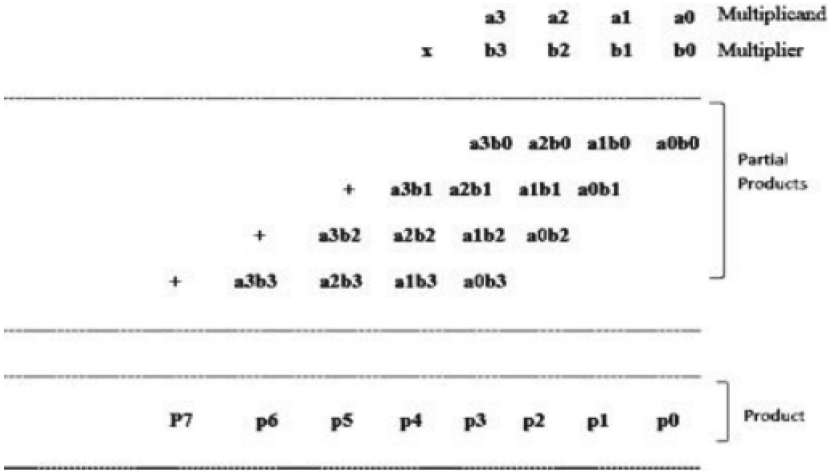

Fig. 2. 4 * 4 array multiplication

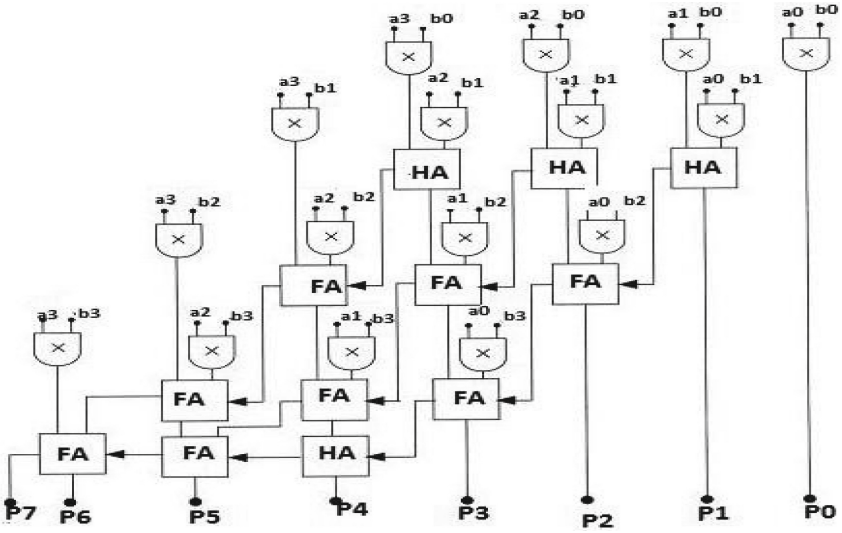

Fig. 3. 4 * 4 Array Multiplier

To reduce the number of partial products generated before adding them compression techniques is used.

Partial product = the multiplicand * multiplier bit

The summation operation is performed with half and full adders, whereas the partial product terms are shifted based on their bit orders, where AND gates are employed for the product. In a m * m array multiplier, partial products are calculated by m * m AND gates, and partial product addition is accomplished by m * (m – 2) Full adders and m Half adders. The partial product's LSB is the leftmost bit, while the partial product's

MSB is the rightmost bit. After multiplication, the partial products are shifted to the left side and are added to get the final result. This method is repeated until there are no more partial products left to be added.

3 Results

When the project code was simulated in Xilinx ISE the RTL schematic and simulated results are as shown below Fig. 4 represents the RTL schematic of array multiplier, Fig. 5 depicts the simulation results of multiplier, Fig. 6 indicates the basic full adder schematic waveform and Fig. 7 illustrates the symbol of 4-bit array multiplier (Table 1).

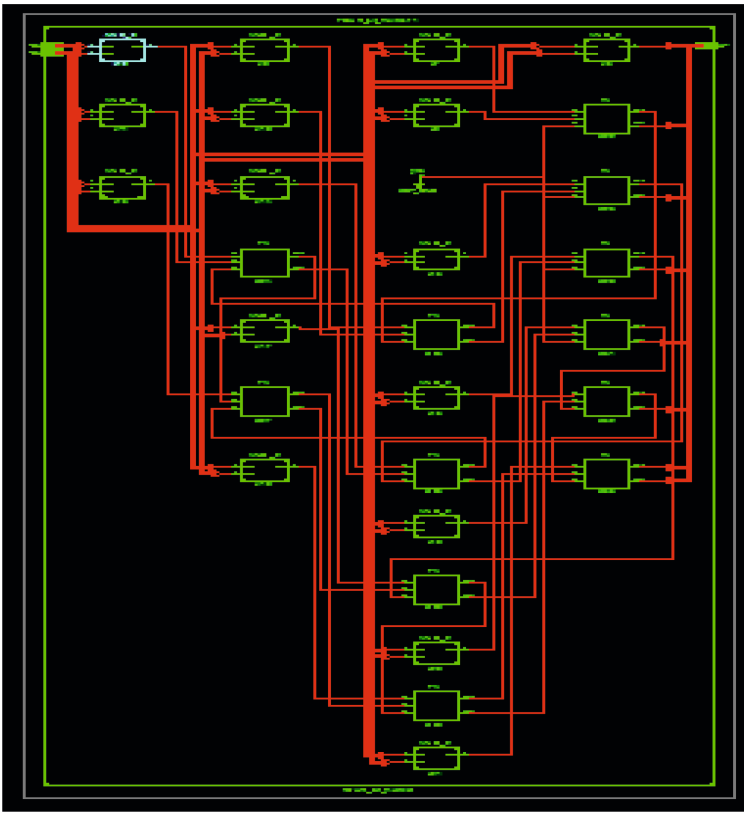

Fig. 4. RTL Schematic of Array Multiplier

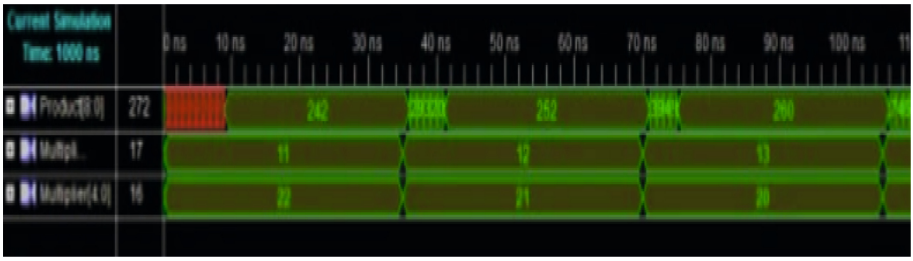

Fig. 5. Simulated result of 4 * 4 Array multiplier

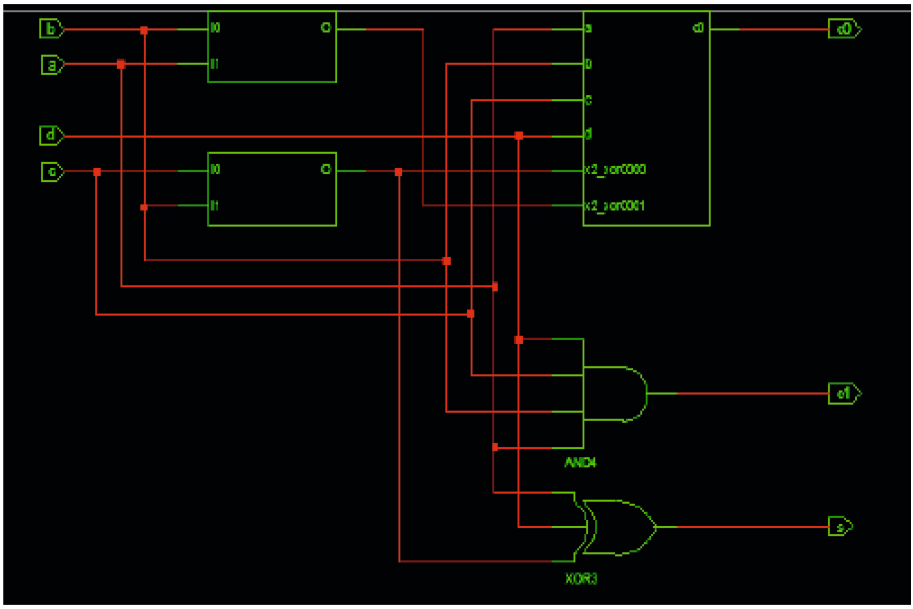

Fig. 6. RTL Schematic of Full Adder

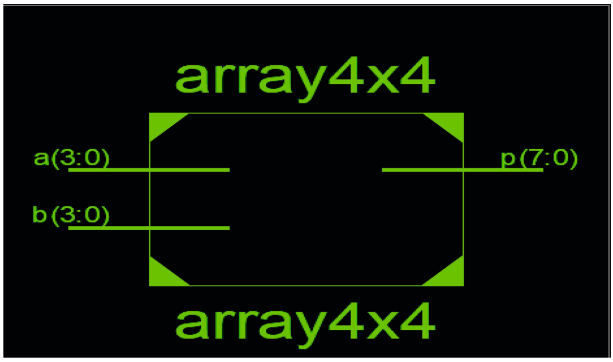

Fig. 7. 4 * 4 multiplier

Table 1. Power and Delay Comparison with existing works

Array Multiplier	Minimum VDDL	Power	Delay
Ref. [2]	250 mV	105.68 nW	7.8 ns
Ref. [5]	250 mV	120.23 nW	24.8 ns
Ref. [6]	350 mV	275.63 nW	5.3 ns
Ref. [7]	100 mV	6.6 nW	16.5 ns
Proposed design	100 mV	1.92 nW	0.95 ns

4 Conclusion

The proposed design of array multiplier has many advantages like it is easily scalable, pipelined and easy to place and route due to its regular shape and also has less complexity. Every design has some or the other drawbacks so similarly the drawback of this design is high power consumption and large area if the bit size is high. This design can be utilized to perform arithmetic operations like filtering, Fourier transforms and image coding and it can be used for high-speed operation.

References

1. Sahoo, S.R., Mahapatra, K.K.: Design of low power and high-speed ripple carry adder using modified feed through logic. In: 2012 International Conference on Communications, Devices and Intelligent Systems (CODIS) (2012). 978-1-4673-4700-6/12/$31.00 ©2012 IEEE
2. Vaidya, S., Dandekar, D.: Delay-power performance comparison of multipliers in VLSI circuit design. Int. J. Comput. Netw. Commun. (IJCNC) **2**(4), 47–56 (2010)
3. Saxena, P., Chandra, D., Kumar, S.: Design of a 1-bit full adder for low power application. (IJAEST) Int. J. Adv. Eng. Sci. Technol. **10**(1), 019–025 (2011)
4. Sunil Gavaskar Reddy, Y., Rajendra Prasad, V.V.G.S.: The power comparison of CMOS and adiabatic full adder circuits. Int. J. VLSI Des. Commun. Syst. (VLSICS) **2**(3), 11 (2011)

5. Ali, M.H., Sahani, A.K.: Study and implementation and comparison of different multipliers based on array, KCM and Vedic mathematics using EDA tools. Int. J. Sci. Res. Publ. **3**(6), 1 (2013). ISSN 2250-3153
6. Ravi, N., Jaya Chandra Prasad, T., Subba Rao, T., Subbiah, Y.: A novel low power, low area array multiplier design for DSP applications. In: Proceedings of 2011 International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN 2011) (2011)
7. Singh, A.K., Prasad, B., Maity, S.: Design and comparison of multipliers using different logic styles. Int. J. Soft Comput. Eng. (IJSCE) **2**, 374–379 (2012). ISSN 2231-2307
8. Kishore Kumar, A., Soma Sundareswari, D., Duraisamy, V., Shunbaga Pradeepa, T.: Design of low power full adder using asynchronous adiabatic logic. Eur. J. Sci.