Key Technologies and Future Developments in the Design of Spaceborne Digital Transparent Processors

Zhongyue Liu[1](✉), Jiatao Cui[1], Jiayu Wang[2], and Yuqian Liu[1]

[1] Institute of Telecommunication and Navigation Satellites of CAST, Beijing 100094, China
liuzhongyue_hit@163.com

[2] Xi'an Institute of Space Radio Technology, Xi'an 710100, Shaanxi, China

Abstract. With the continuous development of satellite communication technology, the people of the traditional commercial communications satellite can only provide service pattern fixed repeater, now already far cannot satisfy the current needs of satellite communications, now the high flux of satellites at the same time of increasing system capacity, has a higher requirement to the flexibility, which uses digital transparent processor (DTP, Digital Transparent Processor and other digital flexible load become the inevitable trend of today's development. This paper introduces the component interface and basic functions of a typical spaceborne digital transparent processor. The key technologies in DTP design are analyzed and the future development of DTP is described. The results and benefits of spaceborne DTP in practical application are explained.

Keywords: DTP · communication satellites · key technologies · future development

1 Introduction

With the rapid development of ground satellite communication application technology, traditional civilian commercial communication satellites can only provide fixed service mode transponders, which are far from meeting the needs of practical applications. It is required to digitize analog transponders and use digital payloads to provide sufficient flexibility for satellite communication systems.

The transponder is realized by three technical routes: analog transparent transponder, regenerative processing transponder and digital transparent forwarding. The traditional analog transparent transponder is limited by the performance of analog filter and microwave exchange matrix, the exchange particle size is coarse, and the adjustment ability is limited, which restricts the system performance. The regenerative process transponder has the guarantee of single channel, high speed and good real-time performance. However, due to the need for signal modulation and demodulation and encoding and decoding, it has high dependence on the system, but the system flexibility is low,

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the equipment complexity is relatively high, and the weight and power consumption are large.

It is hoped that the civil commercial communication satellite can ensure the flexibility of the system with high capacity, and has the advantages of analog transparent transponder and regenerative processing transponder. The Digital Transparent Processor (DTP) appears in the alternative scheme.

Compared with the analog transparent transponder, DTP has the advantages of supporting any subchannel crosslink, upstream spectrum detection, adjustable subchannel gain, flexible use, etc. It is especially suitable for the application scenarios with multi-communication system, multiservice bandwidth and one hop transmission requirements. At the same time, through the management of the subchannel, the resource utilization of the system is improved, and the shortcoming of the analog transparent transponder is overcome.

Compared with the regenerative transponder, DTP does not need to perform signal modulation and demodulation, encode and decode, and only completes the processing of physical subchannels, which is independent of the system and has higher flexibility. It saves a lot of regenerative processing resources for digital channel processing, and the total capacity of the system is large.

The digital transparent processor uses the flexible onboard channelized filtering technology to support information interaction between any frequency band and any bandwidth on board and flexible cross beam interaction, and can flexibly realize the integrated processing of high speed information acquisition services, broadband communication services and measurement and control services, so that the system has the ability to flexibly select the appropriate communication system, divide the best channel and temporary networking. Improve the flexibility and reliability of communication, and realize the flexible exchange of satellite signals and resources. DTP products will gradually replace satellite analog transparent transponders to a certain extent, representing the technical trend of the digital development of satellite payloads in the future, and is extremely important for the subsequent development of military and civilian satellites [1–3].

This paper first introduces the architecture design of DTP, introduces the basic functions, interfaces and components of digital transparent processor, then analyzes the key technologies in DTP design, and finally expounds the future development of DTP, explaining the achievements and benefits of spaceborne DTP in practical applications in the future.

2 Digital Transparent Processor Architecture Design

In the high throughput communication satellite, the DTP link can realize the flexible forward and backward cross-link of user beam, and the traditional “two hop” communication mode of “forward link + backward link” can be changed to the “one hop” communication mode of client to end. Figure 1 shows the information flow of DTP link in USERS to USERS mode.

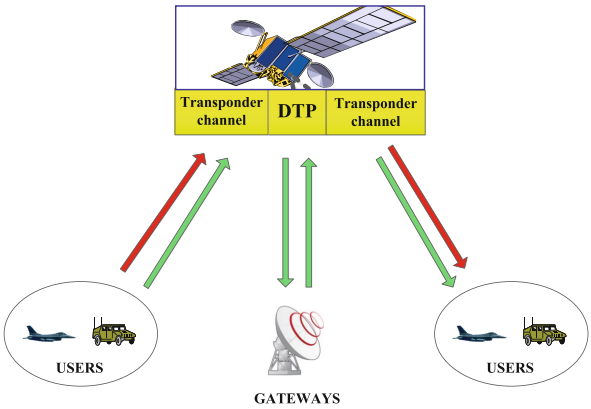

Fig. 1. "One hop" and "two hop" mode information flow diagram

2.1 DTP Components and Interfaces

DTP is mainly composed of channel processing, switch processing, control, frequency synthesizing and power supply, as shown in Fig. 2. Each branch transmits signals through an internal connector, and the channel processing branch is equipped with a special Application Specific Integrated Circuit (ASIC) chip, which has the ability to complete the digital channelization of the input channel and the digital channel synthesis processing of the output channel. At the same time, ADC/DAC(Analog to Digital Converter/Digital to Analog Converter) chip is configured to complete the channel analog to digital and digital to analog conversion function. An extension switch is configured with an ASIC for switching processing and has the ability to perform switching processing on a certain scale of subbands. The control branch completes the receiving and parsing of service remote control instructions, and distributes the corresponding service remote control instructions to the corresponding channel processing ASics and switch processing ASics. At the same time, the working states of channel processing ASics and switch processing ASics are collected and then output after frame processing [4].

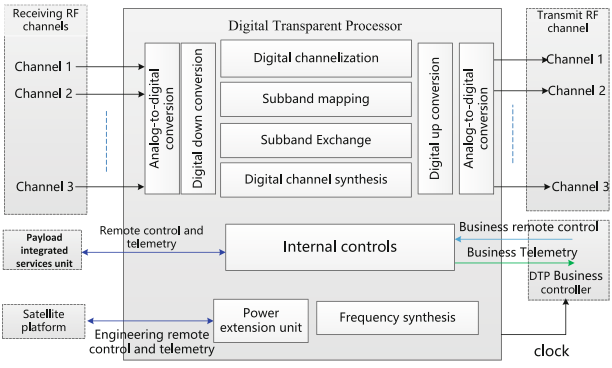

Fig. 2. DTP components and interfaces

The digital transparent processor is connected to the transmitting and receiving radio frequency channel, and there are data and control interfaces between the platform digital tube system, load integrated service unit, DTP service controller and other devices.

2.2 Basic DTP Functions

The basic function of DTP is to process the input upstream IF analog signal through analog to digital conversion, digital channolization, subband mapping, subband switching, subband gain control, digital channel synthesis and digital to analog conversion, and finally output the downstream IF analog signal, as shown in Fig. 3. At the same time, DTP receives external service remote control commands, completes subband mapping, subband switching, and subband gain control of a single machine, monitors the internal working status of a single machine, completes subband and channel power estimation, and frames the status information of a single machine into telemetry information for output.

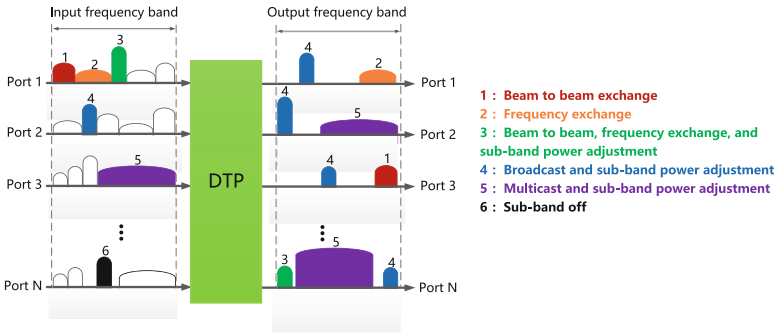

Fig. 3. DTP basic functional mode diagram

3 Digital Transparent Processor Key Technologies

Digital transparent processing transponder technology, involving electrical design and core components, mainly including the following seven aspects of technical difficulties.

3.1 The Engineering Realization of High Speed Digital Channelization with Flexible Bandwidth Configuration

Digital channelization is the realization of channel separation and synthesis in digital domain, and then realize the separation and synthesis of subband signals with dynamic variable bandwidth. The traditional digital channelization method is based on polyphase filter structure, which is characterized by dividing the whole sampling bandwidth into the required number of subchannels in one step. At the same time, because FFT can be used for calculation, the system resource utilization can be greatly reduced [5].

How to ensure the perfect reconstruction of the process of "wideband signal - multiple subbands - wideband signal" without distortion has become an urgent problem to be solved. In the traditional digital channelization technology, the filter obtained according to the perfect filter design method has been developed into a perfect filter bank. The perfect filter bank divides a complete broadband signal into multiple subbands through the filter bank, and then the subband signal passes through the filter bank, which can be nearly perfectly restored to the original information. Figure 4 below shows the subband splicing diagram and the amplitude-frequency response of the spliced subband after channelization and synthesis [6].

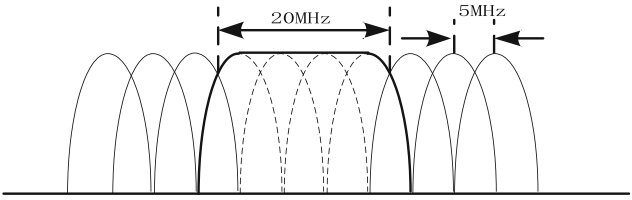

Fig. 4. Subband splicing diagram

Through the design method of the perfect reconstructed prototype filter, the whole frequency resource can be divided into multiple resource blocks according to the subband granularity. The nearly perfect reconstructed complex exponential modulation filter bank means that each filter is obtained by complex exponential modulation of a prototype filter. This filter bank can make use of the polyphase structure in engineering implementation, reduce the filter's demand for system resources, and facilitate engineering implementation as shown in Fig. 5.

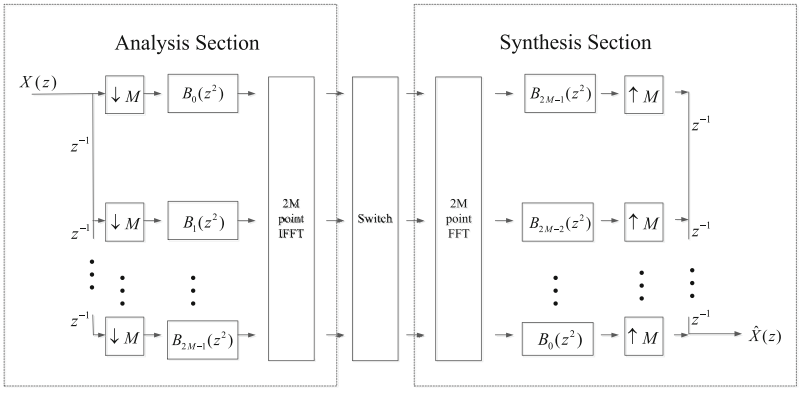

Fig. 5. The engineering implementation of nonuniform bandwidth digital channelizers

3.2 Engineering Implementation of Routing and Switching Technology of Super Large Capacity Subchannel

DTP forwarding of subband information of different frequencies is a subband switching process. Because the complexity of subband switching unit is proportional to the square of the number of switching ports, the number of switching unit ports should be reduced as much as possible in implementation.

Through the introduction of time division multiplexing mechanism, the subband switching unit needs to deal with both time division switching and space division switching. The time division in the subband switching unit is converted into T level and the space division is converted into S level, so the subband switching unit needs to contain at least 1 T level and 1 S level. According to the different connection modes of T-level and S-level, there are two ways to implement the subband switching unit, namely T-S-T and S-T.

The implementation of T-S-T switching structure is simple, and non-blocking switching can be realized by scheduling algorithm. The constraints on the implementation of T-S-T switching structure mainly include synchronization between switching units, the cache rate of time-division switching units and the switching capacity of air-division switching units. Figure 6 below shows the T-S-T implementation of the subband switching unit [7].

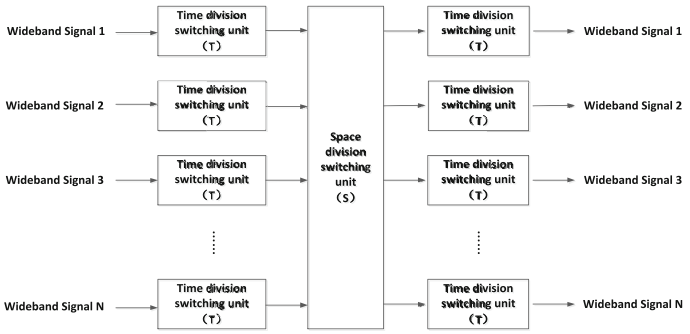

Fig. 6. T-S-T structure of subband switching unit

The S-T switching structure is similar to the T-S-T switching structure. The difference is that the first level time division switching unit is replaced with the input processing unit, as shown in Fig. 7, to complete the packet encapsulation and forwarding path search of subband data, the second level air division switching unit and the third level time division switching unit are changed to asynchronous working mode, and the whole switching structure no longer needs synchronous allocation modules.

Compared with the T-S-T switching structure, the S-T switching structure adopts the packet switching mode and lacks the first-level intermediate slot scheduling, resulting in the output port conflict and loss of switching packets. In order to cope with the output port conflict, the switching capacity of the air division switching unit needs to be further improved. As a result, the data rate between the input processing unit, the air division switching unit and the time division switching unit also needs to be further improved.

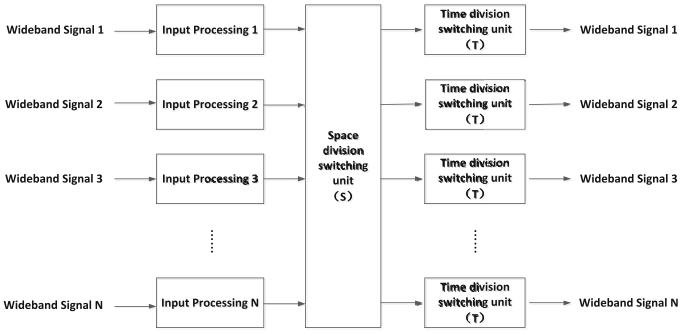

Fig. 7. S-T structure of subband switching unit

For different switching structures, how to optimize the network topology in engineering implementation, improve the reliability and availability of the whole network, and ensure non-blocking high speed channel switching under the condition of network element failure will become the focus of future development.

3.3 The Engineering Realization of Large Scale Complex Digital Integrated Single Machine

For complex integrated single machine, it is required that the power supply network conversion efficiency is high, the energy loss is reduced, and the network is stable and reliable. At the same time, it is necessary to ensure the reliability of the clock and data transmission network, and has self-check and recovery functions. In addition, for very large scale complex integrated digital integrated single-machine, for high integrated circuit boards, large power consumption devices, new and more efficient heat dissipation methods need to be adopted.

At present, the heat dissipation of large power devices in spaceborne single machine mainly depends on the heat dissipation copper or aluminum sheet, one end of the heat sink is crimped on the large-power device, and the other end is connected to the reinforcement bar of the single machine structure. This method mainly relies on copper or aluminum with high thermal resistance for heat conduction, and the heat dissipation path is mainly the reinforcement bar of the single machine structure, which is limited by the design of the reinforcement bar. Generally, there is a narrow heat dissipation path and a long path, and the overall heat dissipation efficiency is low. The current heat dissipation mode cannot meet the heat dissipation requirements of boards with large power consumption.

The heat pipe heat dissipation efficiency is several orders of magnitude higher than that of conventional materials such as copper and aluminum. The heat pipe technology is applied to the heat dissipation of large power components in a single machine. For example, the heat pipe is directly laid on the large-power components (ASICs), which can solve the heat dissipation problem of large power components and improve the overall heat dissipation efficiency of a single machine.

3.4 High Speed and Reliable Data Transmission Technology

At present, there are two technical ways to realize data transmission: optical transmission and electrical transmission. The electrical interface technology is mature and heavy, and the backplane has the advantage of power consumption [8]. The optical interface is less reliable and lighter, and has the advantage over the cable transmission.

At present, according to the calculation of data throughput, the data rate of a single data transmission link between the channelized processor and the switching processor will reach more than 20Gbps in the future, so the data transmission between the processors will be achieved by optical fiber transmission [9].

3.5 Multilevel Clock Allocation Network Management Technology

Under the board architecture based on backplane and high speed connector, the high speed cooperation between the board and the board module puts forward higher requirements for the allocation and management of clock network. The use of the one-level clock allocation management network brings the following two problems to provide clock for all processing modules:

1) The clock path is too long, resulting in a serious decline in the quality of the clock signal waveform;
2) With the limited adjustment ability of the clock allocation management module, the clock signal transmission path between each module is difficult to synchronize.

This problem is solved by using a two level clock allocation management network. As shown in Fig. 8 below, a first level clock allocation management module completes the system clock management of large functional modules between subboards, and multiple second level clock allocation management modules complete the board level clock management between subboards.

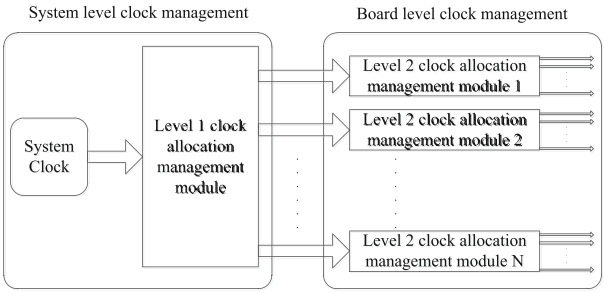

Fig. 8. Schematic diagram of a two level clock allocation management network

3.6 High Speed Signal Transmission Delay Control Technology

In a digital system that works synchronously, the actions of all system components that use clock signals must be coordinated, and the working system will have normal timing.

When the phase difference between clock signals and high speed parallel data signals reaching different IC input clock pins exceeds the maximum tolerance range, various abnormal phenomena will appear in the system.

The main purpose of using high-speed signal transmission delay control technology is to minimize the phase difference between multiple clock signals or parallel data signals. The phase difference can not be eliminated, can only be minimized in the design, the main technical means are as follows:

1) In the two level clock allocation management module, a clock management chip with small difference and adjustable is used.
2) Considering the layout of the subboard and high speed PCB design, SI simulation is carried out on all clock signals and high speed parallel data signal networks by means of high speed signal integrity analysis to ensure that the transmission delay of the physical path is as consistent as possible.

3.7 High Speed ADC/DAC Conversion

With the improvement of digital signal processing technology and digital circuit working speed, as well as the continuous improvement of system sensitivity and other requirements, high requirements are put forward for high-speed and high-precision ADC/DAC indicators.

According to the Nyquist sampling law, the sampling rate must be at least twice the bandwidth of the signal. At the same time, in order to support the flexible standard, the transceiver modules of modern communication are more and more common to use digital IF direct sampling, which further improves the performance requirements for high speed analog to digital conversion chips [10].

In the development process of DTP, analog to digital conversion chips need to sample or output signals of higher and higher frequencies and higher and higher bandwidth. The noise and signal distortion caused by analog to digital or digital to analog conversion are often difficult to compensate for and can have a significant impact on system performance. Therefore, the performance of high speed ADC chip in sampling or analog to digital conversion is very important to the system index. At the same time, in order to complete the complex system function, the power consumption of each submodule in the large system should be as low as possible, so low power ADC/DAC conversion is essential. In short, an ADC/DAC chip with large broadband, low power consumption, high dynamic range and sample rate is one of the key core technologies in the development of DTP.

4 Future Development of Digital Transparent Processors

DTP is the most complex and most powerful spaceborne processing products at present, which uses a large number of advanced processing technologies, and is the concentrated embodiment of the comprehensive development level of aerospace products.

4.1 Future Trends of DTP

At present, the three major satellite manufacturers: Boeing, ADS, and TAS have developed DTP products. DTP technology has gradually expanded from early mobile communications satellites to Ku and Ka band broadband missions, as well as the latest HTS/VHTS missions. Each company has different standards for DTP generation. At present, DTP products can be divided into five generations according to single-port processing bandwidth, as shown in Table 1.

Table 1. DTP generation typical indicators

Argument	The first generation	The second generation	The third generation	The fourth generation	The fifth generation
Number of ports	120	20	14	48 & 128	reachable 160
Port processing bandwidth	30 MHz	125 MHz	250MHz	500 MHz	2.9 GHz
Subchannel spacing	200 kHz	2.6 MHz	250kHz	312.5kHz	3.515 MHz
Weight	160 kg	/	21kg	58 kg & 154 kg	371.2 kg
Power dissipation	1800 W	/	270W	792 W & 2112 W	/
Structure	Discrete vertical + backplane	/	Integrated planking	Discrete vertical	Discrete vertical
Manufacturer	Astrium	Boeing	Astrium	Thales	Thales

In the future, DTP will develop towards greater bandwidth, more functions, lower weight and power consumption. No matter which generation of products, in the era of emergence are very large scale complex integrated digital processing machine, representing the highest level of digital load in aerospace manufacturing at that time.

4.2 Application Result Benefit

DTP is used to enhance the capability of satellite ground integrated satellite communication applications, realize the system integration of various services, build high orbit space based infrastructure, promote the integration of military communications and civil and commercial communications, and realize the autonomous and controllable HTS satellite system.

The breakthrough of DTP technology can form and enhance the development and research capacity of domestic spaceborne super large scale complex processing products, drive the upgrading of high performance and high quality products of related product supporting units of the whole domestic industry chain, and lead the core technology

level improvement and products of domestic technical advantage units. Optimize the product development process, improve the product output efficiency, reduce the weight and power consumption ratio of the product per unit bandwidth, improve the international competitiveness and influence of the product, and lay the technical foundation for the subsequent development of the fifth generation product.

5 Conclusions

This paper introduces the component interface and basic functions of a typical spaceborne digital transparent processor. The key technologies of DTP implementation are analyzed and the future development of DTP is described, and the achievements and benefits of spaceborne DTP in practical application in the future are explained.

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