Low Power VLSI Architecture for Rail To Rail Dynamic Voltage Comparator

S. Karunakaran(✉), S. Srivardhan, M. Harshith, and K. SaiManish

Vardhaman College of Engineering, Hyderabad 501218, India
{s.karunakaran,samalasrivardhan20ece,moredddyharshithreddy20ece,
kawlaskarsaimanish20ece}@vardhaman.org

Abstract. Rail to Rail Dynamic Voltage Comparator (RRDVC) works on very low voltages which is constructed and developed using cadence virtuoso tool. Here 90nm technology was used to construct and analyse the 3 different architectures of Rail to Rail Dynamic Voltage Comparators.Here Three different architectures are made by varying the stages with NOT of AND and NOT of OR. The power dissipation, delay and the power delay products(PDP) are compared for the three different architectures developed by varying the inputs. Comparator circuit takes the analog signal , reference voltage and the clock signal as input and gives the outputs as digital signals with 0's and 1's. not operation of AND and not operation of OR based stages are arranged as per requirement to obtain the three different architectures and the outputs of these stages are combined using latch circuits. The outputs are obtained for different frequencies of input analog signals with the different reference voltage. All these architectures are implemented using basic CMOS transistors. The power dissipations obtained here are 1.9×10^{-6}W , 19×10^{-12}W and 1.7×10^{-6}W for the RRDVC with NOT of AND and OR , NOT of NAND, and NOT of OR based stages respectively. The architecture with NOT of AND stages provides less power when compared to the other architectures.

Keywords: Dynamic comparator · low voltage · RR-DVC · CMOS · low power · PUN-Pull Up Network · PDN-Pull Down network · VGS-Gate to Source Voltage · Cadence Virtuoso

1 Introduction

A Rail-to-Rail Dynamic Voltage Comparator is a specialized type of comparator that overcomes some of the limitations of standard comparators. As the name suggests, it operates with a rail-to-rail input and output voltage range, meaning it can accept and provide output signals that are close to the power supply rails. This feature makes them highly desirable in applications where the input voltage can vary across the full range of the power supply voltage. Using NOT of AND and NOT of OR gates is cost-effective and simpler to manufacture, making them the preferred building blocks for digital logic circuits in integrated circuits (ICs).

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2 Fully-Synthesizable Dynamic Voltage Comparators

It has been noted that transistor current contention affects fully synthesizable dynamic voltage comparators. Lower voltages improperly force NAND gates' outputs in NAND-based stages at the circuit power supply, regardless of the input (the comparator stops working as a result). Hence the project is designed to overcome the current contention and which works at low power, at last use of low power increases the speed of the circuit and gives good outcome.

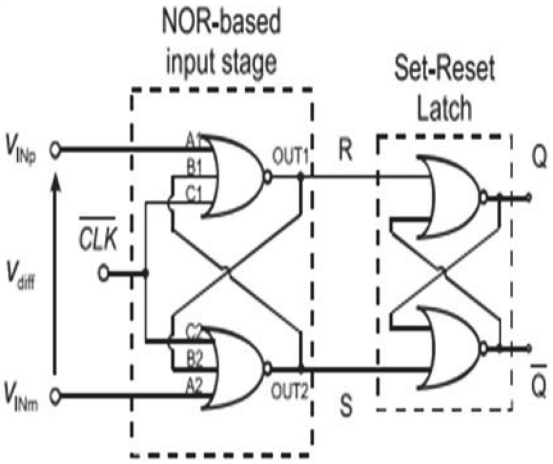

Fig. 1. Fully Synthesizable DVC with not operation of AND using set reset latch.

The DVC in Fig. 1 receives the digital output during the rising edge of the clock signal. The not operation of OR-based stage is created so that the digital output is accessible during the rising edge.

The logic switching and the differential voltage at the analogue input are used to determine the polarity. Reducing the voltage levels of OUT1 and OUT2 within the DVC could lead to a diminished driving capacity and logic levels. The driving by the analogue inputs causes the current in the transistor load terminals of 1st PUN and 2nd PUN to counteract. For the purpose of lowering the common mode input voltage, the Vsg of 1st PUN transistor and 2nd PUN transistor is raised. The current opposes the dropping transients of OUT1 and OUT2.

2.1 Limitations of Dynamic Voltage Comparators:

- Noise Sensitivity
- Propagation Delay
- Offset Voltage
- Limited Input Range
- Power Consumption
- Current Contentions

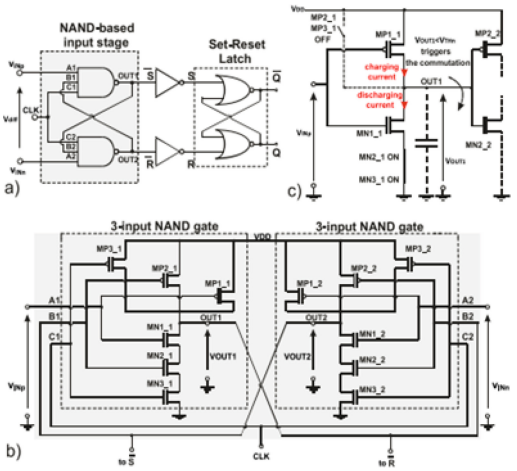

Fig. 2. DVC with not operation of AND based stages a) logic-level and b) transistor-level implementation, c) same circuit during output switching.

2.2 Related Works

Standard-Cell Based: Utilize digital standard cells, enabling design automation and integration with digital circuits. Offer low power and scalability but may suffer from process variations and limited performance.

Analog Based: Employ traditional analog design techniques, achieving higher performance but with larger area and increased design complexity.

3 Existing Architecture of Rail to Rail Dynamic Voltage Comparators:

The RR-DVC in Fig. 3a overrides the circuits of completely synthesizable DV Comparators given in Figs. 1 and 2a half-swing common-mode constraints. According to this picture, the RR-DVC combines the digital outputs of the not operation of AND3 and not operation of OR3-based DVCs in a similar way as traditional rail-to-rail analogue operational amplifiers combine an CMOS transistors differential pair into push-pull differential pair.

Outputs of the not operation of AND Based stage and the not operation of OR based Stage are combined using set-rest latch, a bistable multivibrator. The first stable condition is high output, whereas the second is low production. A Latch has a feedback route that allows information to be maintained by any device.

The Existing Architecture will result in higher power consumption hence new architectures are formed by changing both the input stages with the NOT of AND stages. Usually NOT of AND consumes less power than the NOT of OR

because power supplied to NOT of AND pmos transistors are connected parallel consumes less power whereas NOT of OR consumes more power as pmos transistors connected in series.

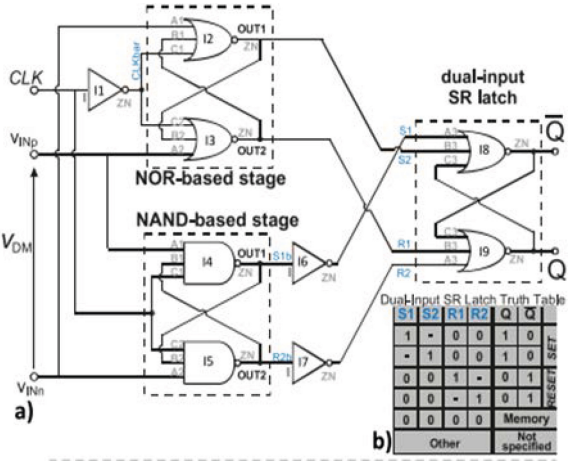

Fig. 3. Existing fully-synthesizable RR-DVC with not operation of AND3 and not operation of OR3 based stages a) logic-level implementation b) logic table of the Set-Reset latch

3.1 Limitations of the Existing RR-DVC:

Higher Power Consumption: RR-DVCs generally consume more power compared to standard DVCs due to the additional circuitry required for railto-rail operation. The extended input and output voltage range necessitates more complex design and increased power dissipation.

Increased Complexity: RR-DVCs have a more intricate design to achieve rail-to-rail functionality, which can make them more challenging to implement and potentially increase the risk of design errors.

Higher Cost: Due to their increased complexity and specialized functionality, RR-DVCs are generally more expensive than standard DVCs.

4 Proposed Architecture of the Rail to Rail Dynamic Voltage Comparator:

It is almost similar to the existing architecture, in the proposed architecture, not operation of AND3 and not operation of OR3 based stages are replaced with the not operation of AND3 based Stages. RR-DVC sum up or merges the digital

results of the two not operation of AND3-based stages. Set-Reset latch is used to mix the outputs of these stages as shown in Fig. 4. Set-Reset Latch is a bistable multivibrator. The first stable condition is high output, whereas the second is low production. A Latch has a feedback route that allows information to be maintained by any device. This circuit is implemented in the cadence virtuoso tool in the 90nm technology. Then the Comparator outputs are obtained. Power can also be calculated using cadence virtuoso tool.

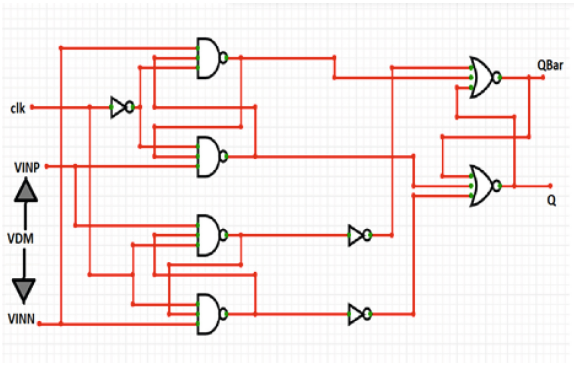

Fig. 4. Block Diagram of Proposed RR-DVC with not operation of AND3- based stages.

Table 1. Truth Table of Proposed Architecture

Clk	$Vinp$	$S1$	$S2$	$R1$	$R2$	Q	$Qbar$
0	x	0	0	0	0	Memory	Memory
1	>vinn	1	x	0	0	1	0
1	>vinn	x	1	0	0	1	0
1	<vinn	0	0	1	x	1	0
1	<vinn	0	0	x	1	1	0

The next proposed architecture is also similar to the existing RR-DVC. Here not operation of AND3 and not operation of OR3-based stages from the existing architecture are replaced with the NOR based stages and these outputs are combined using Set-Reset Latch as shown in the Fig. 5. Set-Reset Latch, a Bistable Multivibrator used to combine the NOR based stages. The Results of the Set-Reset bistable multivibrator are Q and Qbar and the inputs are the outputs of the not operation of OR3-based stages (Table 1).

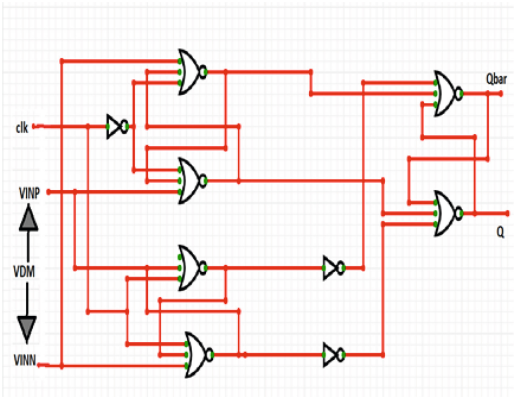

Fig. 5. Block Diagram of Proposed RR-DVC with not operation of OR3-based stages.

The cadence virtuoso tool with 90nm technology was used to develop completely synthesizable dynamic voltage comparators with not operation of AND3-based input stages (NAND-DVC) and completely synthesizable dynamic voltage comparators with not operation of OR3-based stages. The crucial elements of analog-to-digital converters can operate across a wide span of supply voltage values, primarily influenced by the sensor's maximum input voltage.
The sensor input used to determine the step size changes determines the reference voltage. The circuit's high speed operating in the 1GHz band makes it appropriate for flash ADC. The supply voltage ranges from 0.6 to 1.2 V. If the supply voltage falls, the driving capacity drops.

The driving power of the circuit is also impacted by the leakage current. As a result, the suggested design is tailored, and a digital standard cell-based module is made as part of the ADC integration process. When using a speed greater than 5GHz, several restrictions are observed. Power grows, yet at little sacrifice. This circuit is executed in its entirety with a very small footprint and under full synthesizability. When compared to CMOS, the switching speed of FinFET is faster. Therefore, by raising the Vgs of the PUN transistor gates, the common-mode input voltage is decreased (Table 2).

5 Results and Outputs

Existing RR-DVC produces power dissipation of 1.927×10-6W While the Rail to Rail Dynamic Voltage Comparator with NAND Based stages produces power dissipation of 19.08×10-12W and RR-DVC with NOR based stages produces a power dissipation of 1.796×10-6W. The NAND-based DVC is quite effective when compared to the NAND, NOR, and RR-DVC performance. The suggested NAND logic work base performs better (Fig. 6).

High output occurs when the voltage at the non-inverting input surpasses that at the inverting input. Conversely, low output is observed when the voltage

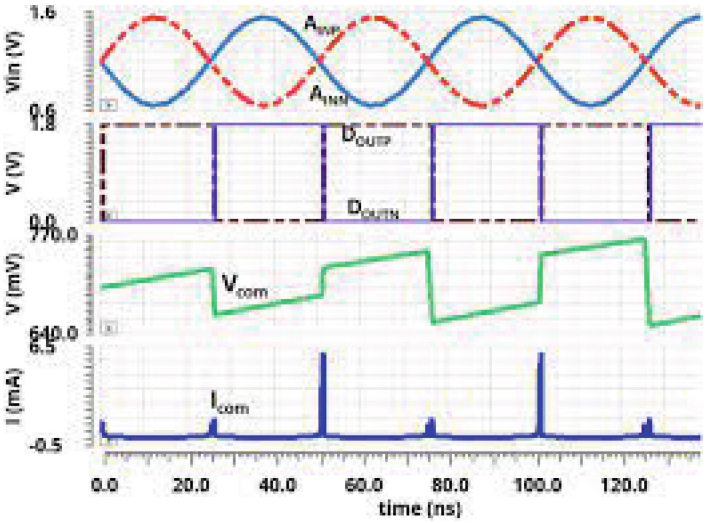

Fig. 6. Output of RR-DVC with NAND Based Stages

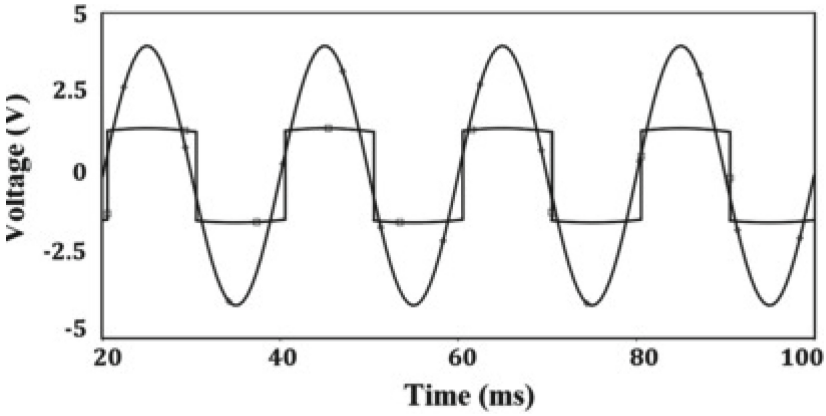

Fig. 7. Output of RR-DVC with NOR Based Stages

at the inverting input equals or exceeds that at the non-inverting input. Certain designs may feature a variable threshold voltage instead of a direct reference to VDD or VSS (Fig. 7).

Table 2. Comparative Analysis of three circuits

$ExistingRRDVC$	$ProposedRRDVC1$	$ProposedRRDVC2$
power $= 1.927 \times 10^{-6}$W	power $= 19.08 \times 10^{-12}$W	power $= 1.796 \times 10^{-6}$W
Delay $= 103$ ps	Delay $= 115$ ps	Delay $= 107$ ps
PDP $= 198.481 \times 10^{-18}$	PDP $= 1984.32 \times 10^{-24}$	PDP $= 192.172 \times 10^{-18}$
Dual SR latch is used.	Dual SR latch is used.	Dual SR latch is used.
Consumes more power	Consumes less power	Consumes same power as the existing one.
Both NAND and NOR based Stages are used.	Only NAND Based stage is used.	Only NOR Based stage is used.

6 Conclusion

Hence both existing and proposed Rail to Rail Dynamic Voltage Comparators are designed. Hence it is observed from the obtained graphs that, Rail to Rail Dynamic Voltage Comparator (i.e., proposed model) dissipates less power when compared to existing method. Hence Proposed RR-DVC gives around 80% lesser power when compared to Existing Rail to RR-DVC. In circuits with low amplitude signals, the design of the comparator becomes critically important. ADCs use comparators at the input step of the transformation process. To achieve faster operation and lower power consumption, data converters require efficient circuit designs.

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