Research on Data Security Acquisition System Based on Artificial Intelligence

Yingjian Kang(✉), Lei Ma, and Leiguang Liu

Telecommunication Engineering Institute, Beijing Polytechnic, Beijing, China
kangyingjian343@163.com

Abstract. The traditional acquisition system had low collection efficiency and poor acquisition accuracy. In order to solve the above problems, a new data security acquisition system was studied. Artificial intelligence technology was introduced to design the hardware and software parts of the system. The hardware part mainly designed the system A/D acquisition module, serial data acquisition module and parallel port communication module. The software part was divided into three steps: data screening, data analysis and data acquisition. By comparing with the traditional system, the actual working effect of the system was verified. The experimental results showed that the data security acquisition system based on artificial intelligence had higher collection efficiency and better precision. The system was worthy of recommendation.

Keywords: Artificial intelligence · Secure acquisition · Acquisition system · Data acquisition

1 Introduction

There are usually two explanations for data collection: one refers to terminal computer equipment such as inventory machines and handheld computers; the other refers to software for network data collection. The equipment of the data acquisition system refers to the process of automatically collecting information from analog and digital units to be tested such as sensors and other devices to be tested. The data acquisition system is a flexible [1], user-defined measurement system that combines computer-based measurement software and hardware products to collect content such as web pages and forums in batches. The system can directly save the collected data to a database or publish to the network. The original webpage can be automatically collected according to the rules set by the user, the content required in the format webpage can be obtained, and the data can be processed [2].

It mainly has the following characteristics: ① System with strong software and hardware support. All the hardware and software resources of the general-purpose microcomputer system can be used to support the system to work. ② With independent development capabilities [3]. ③ The application configuration of the software and hardware of the system is relatively small, and the cost of the system is relatively high. However, when the secondary development is performed, the software and hardware expansion capabilities are better. ④ The reliability of the operation in the industrial environment is poor, and the environment for placing is high [4]. ⑤ The system does

G. Gui and L. Yun (Eds.): ADHIP 2019, LNICST 301, pp. 112–119, 2019.
https://doi.org/10.1007/978-3-030-36402-1_12

not have the ability to develop independently. Therefore, the software and hardware development of the system must rely on development tools. ⑥ The software and hardware design and configuration scale of the system are all based on the principle of meeting the functional requirements of the data acquisition system. Therefore, the software and hardware applications of the system have a configuration ratio close to 1, and have the best cost performance. ⑦ The system is reliable and easy to use. The application runs in ROM without being destroyed by external interference, and the system immediately enters the user state after power-on [5].

2 Research on Hardware of Data Security Acquisition System Based on Artificial Intelligence

In the campus network performance data acquisition system, the acquisition system needs to transmit the analog parameters such as motor speed and current loop to the monitoring host on the one hand, and collect various parameters and image data of the lower computer on the other hand. At the same time, the monitoring host also sends various control signals to the lower computer. In order to balance various needs, the design combines analog and digital acquisition methods, which can realize 8-channel A/D sampling, 2-channel serial data acquisition and 2-channel parallel data acquisition. The block diagram of the system is shown in Fig. 1:

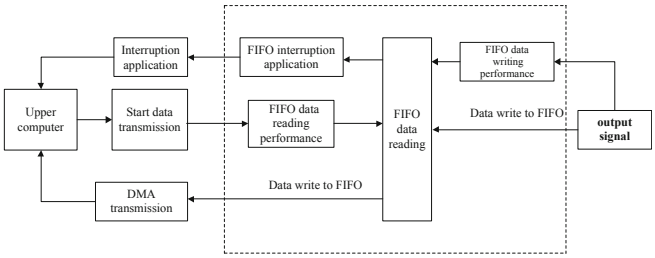

Fig. 1. Data security acquisition system hardware based on artificial intelligence

2.1 Acquisition Module Design

The acquisition system uses the digital signal processing chip TMS320F2812 as the control core, and the F2812 has a maximum operating frequency of 150 MHz. In addition to a wealth of internal memory resources, it also has a variety of peripheral resources such as ADC, SCI, SPI, etc. The design utilizes its ADC and SCI modules for analog signal and serial digital signal acquisition [6]. Data collection for parallel data is directly exchanged with the host without going through the DSP. Because the host and peripheral speed do not match, the dual-port RAM chip IDT70V24 is selected as the data cache. It is a high-speed, low-power dual-port RAM with a storage capacity of 8 k bytes. The logic control of the system is completed by CPLD chip XC95108. Its main functions are PCI local bus arbitration and address decoding. The implementation of the three acquisition modules is as follows:

(1) A/D acquisition module. The analog signal is sampled using the F2812's own digital-to-analog converter module ADC. The ADC has 16 analog input channels with two built-in S/H (sampler keeper), conversion accuracy of 12 bit, maximum conversion rate of 12.5 MSPS, and support for data input ranging from 0 to 3 V [7].
(2) Serial data acquisition module. F2812's SCI module has two serial communication interfaces, which can be configured to 65,536 different baud rates, with parity check mark, can work in half-duplex or full-duplex mode, can be set to interrupt or query mode [8]. In addition, SCI has two enhanced features: ① Both transmit and receive have separate FIFOs with a FIFO depth of 16 words and the trigger stage can be configured to any number within 16. This flexible setting is very convenient for practical use, because the data length collected by the lower computer is often not an integer multiple of 16, and the FIFO trigger level is set according to the data length, so that one frame of data can be transmitted and processed in time; ② The baud rate can be automatically detected, which is very suitable in the case of the unknown communication terminal baud rate or the need to replace the communication terminal.
(3) Parallel communication module. For signals with a large amount of data transmission such as image signals, it is necessary to use parallel port communication. The acquisition system provides two parallel ports, the data width is 8 bits, and the address width is 8 bits. They exchange data with the host through the dual port RAM.

2.2 Acquisition System Bus Design

The bus of the acquisition system is selected from the Compact PCI bus. The Compact PCI bus is fully compatible with the PCI standard, but as an open industrial computer standard, the Compact PCI bus is quite different from the PCI bus. It mainly reflects in:

① The Compact PCI bus has thermal switching capability that allows the entire system to replace damaged boards in the event of an uninterrupted power supply, which is critical for systems with high reliability requirements.
② The Compact PCI bus uses a European card (Eurocard) for better mechanical properties. The assembly technology of the European plug-in card is very mature. The plug-in card is inserted vertically into the chassis to facilitate ventilation and heat dissipation.
③ High-density pinhole bus connectors are completely airtight and offer higher shock resistance and reliability than desktop PCI slots.
④ The Compact PCI backplane accommodates up to eight cards and doubles the original PCI specification to better meet the needs of industrial systems.

2.3 Compact PCI Interface Design

At present, many PCI protocol chips also support hot swap, so that the original PCI bus-based hardware system can be easily ported to the CPCI framework without major

modifications in hardware and software. This design uses the PCI9054 from PLX, which complies with the PCI 2.2 specification and the CPCI 2.1 hot swap specification. For the hot swap specification of CPCI, PCI9054 provides the pin ENUM# and LEDon/LEDin. The activation of ENUM# indicates that the plug-in status of the card is about to change. The LEDon/LEDin pin is used to drive an external LED to indicate the current system software layer connection and disconnection. The PCI9054 also provides a hot swap control register HS_CSR to record board status and control status. The definition of HS_CSR is shown in Table 1:

Table 1. Hot swap control status register hs_csr.

Position	Explain
0	Retain
1	EMUM
2	Retain
3	EMUM
4	Retain
5	Retain
6	EMUM
7	Retain

When the board is inserted, HS_CSR [3] is set to 1, the blue light is lit, PCI9054 sets HS–_CSR [7] to 1, and the ENUM# signal is activated to cause an interrupt. The interrupt is cleared until the device driver is installed, HS_CSR [3] is set to 0, and the blue light is extinguished. When the board is unplugged, HS_CSR [6] is set to 1. The activation of the ENUM# signal causes an interrupt. After the host unloads the driver, HS_CSR [3] is set to 1. Lights up in blue, indicating that the board can be safely removed.

2.4 Hot Swap Power Management

The signals used for hot plug control in the CPCI specification are: BD_SEL#, HEALTHY, and PCI_RST#. The pins of the connector J1 of the CPCI bus are divided into a long pin, a medium long pin, and a short pin. The long pin is the power and ground signal, the long pin is the PCI bus signal, and the short pin is BD_SEL# and IDSEL. When the board is inserted, the power signal is first contacted, and the PCI bus signal is precharged to 1 V. This is to reduce the impact on the PCI bus signal during hot plugging. Then there is the PCI bus signal connection, and finally the BD_SEL# signal connection. BD_SEL# is effective to indicate that the board has been plugged in and can be powered on. The card removal process is just the opposite. HEALTHY# is a signal that reflects whether the board's power supply status is good.

The LTC1646 is a hot-swap power management IC from Linear for CPCI interfaces. The LTC1646 requires two external N-channel transistors as switches to control the supply of 3.3 V and 5 V power to the board. The OFF/ON# pin of the LTC1646 is

connected to BD_SEL#. When BD_SEL# is low, the transistor is turned on, and the 3.3 V and 5 V power supplies are powered up at a certain rate. PWRGD# is connected to HEALTHY#, which is low when the board power supply is within tolerance. PCI_RST# is connected to the RESETIN# pin of LTC1646. It is ORed with the HEALTHY signal to obtain the output signal RESETOUT#. This signal is connected to the RST# pin of PCI9054 as the reset signal of the CPCI board. The LTC1646 provides an output pin, PRECHARGE, which is connected to the bus signal of the PCI9054 to pre-charge the bus signal during board insertion and removal.

3 Research on Data Security Acquisition System Software Based on Artificial Intelligence

Modifications to hardware operating parameters are achieved by means of interrupts. Customize a 16-bit control register User_CSR with the upper 4 bits used as the command word and the lower 12 bits used as the control word. When the application writes data to User_CSR through the PCI bus, the CPLD sends an interrupt signal to the external interrupt pin XINT2 of F2812 through the decoding logic. The software workflow is shown in Fig. 2 below:

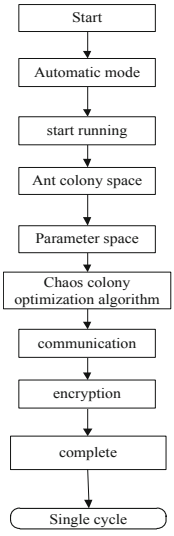

Fig. 2. Software workflow

After the F2812 responds to the interrupt, it reads the value of User_CSR, determines which parameter needs to be modified according to its command word, and then obtains a new parameter value according to its control word, and writes it to the corresponding register to complete the modification. Due to space limitations, the specific implementation method is explained by taking the modification of the SCIA setting as an example. User_CSR defines SCIA as follows (Table 2):

Table 2. Partial definition of User_CSR.

Bit15 ~ 12	11 ~ 0
Command word	Control word
0000	SCI
0001	SCIA
0010	SCIB

The hardware configuration that can be modified through this interface has the baud rate of the SCI, the trigger level of the transceiver FIFO, and the size of the dual-port RAM space occupied by each acquisition channel.

The software work-flow can be represented by the following calculation process:

$$X = \left(r^2 k_1 + r^4 k_2\right) + \left(r^2 + 2x^2\right)P \tag{1}$$

$$Y = \left(r^2 k_1 + r^4 k_2\right) + \left(r^2 + 2x^2\right)P \tag{2}$$

$$Z = \left(r^2 k_1 + r^4 k_2\right) + \left(r^2 + 2x^2\right)P \tag{3}$$

In the above formula, X, Y, and Z respectively represent the three-dimensional coordinates of the acquired data, r represents the acquisition coefficient, k_1 represents the parent band constant, k_2 represents the child constant, and P represents the detection constant.

4 Experimental Results

In order to test the actual working effect of the acquisition system designed in this paper, a comparative experiment was designed.

4.1 Experimental Parameters

The experimental parameters are shown in Table 3 below:

Table 3. Experimental parameters.

Project	Data
Working voltage	220 V
Working current	50 A
Work environment	UMA
Standard of execution	RE
Execute a command	TVA
Working frequency	30 MHz
Working hours	20 min

4.2 Experiment Procedure

Experiment according to the parameters set above, select the traditional acquisition system and the acquisition system of this paper to collect the data of the same computer, record the collection efficiency, and analyze the experimental results.

4.3 Experimental Results and Analysis

Collection efficiency experiment results (Fig. 3)

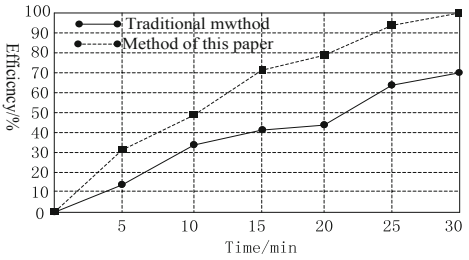

Fig. 3. Collection efficiency experiment results

Observing the above figure, when the working time is 5 min, the collection efficiency of the traditional system is 13%, and the collection efficiency of the system is 31%; When the working time is 10 min, the collection efficiency of the traditional system is 34%, and the collection efficiency of the system is 49%; When the working time is 15 min, the collection efficiency of the traditional system is 40%, and the collection efficiency of the system is 70%; When the working time is 20 min, the collection efficiency of the traditional system is 42%, and the collection efficiency of the system is 80%; When the working time is 25 min, the collection efficiency of the traditional system is 65%, and the collection efficiency of the system is 90%; When the working time is 30 min, the collection efficiency of the traditional system is 70%, and the collection efficiency of the system is 100%.

4.4 Experimental Results

According to the above experimental results, the following experimental conclusions are obtained: the artificial intelligence-based data acquisition system designer has the good ability, and process the data streams were obtained by sampling the analog signals, such as multiplication and accumulation summation operations. For example, there are two types of commonly used digital signal processing chips, one is a dedicated DSP chip, and the other is a general purpose DSP chip. The characteristics of the data acquisition system based on DSP digital signal microprocessor are as follows: high precision, good flexibility, high reliability, easy integration, time-division multiplexing, etc., but at the same time its price is high. (4) Based on hybrid computer acquisition system. This is a system structure that has developed rapidly in the field of computer

applications with the emergence of 8-bit single-chip microcomputers in recent years. It is connected by a general-purpose computer (PC) and a single-chip microcomputer through a standard bus (for example, RS-485 standard). The part of the MCU and its peripheral circuits is specially configured for the functions of data acquisition and other functions. The host computer undertakes the tasks of man-machine dialogue, large-capacity calculation, recording, printing and graphic display of the data acquisition system. The computer data acquisition system based on artificial intelligence technology has the following characteristics: ① It usually has self-development capability. ② The system configuration is flexible, and it is easy to form various large and medium-sized measurement and control systems. ③ The host can be separated from the site to form various local area network systems. ④ Make full use of the host resources, but it will not occupy the full CPU time of the host.

5 Conclusions

This design uses TMS320F2812 as the control core of the data acquisition system, which satisfies the real-time requirements of the system, saves peripheral resources and improves the cost performance of the system. Applying the Compact PCI bus to the acquisition system gives the system the ability to plug in and out, improving the reliability of the entire system and adapting to the needs of the industrial work environment. The innovation of this paper is to combine the advantages of Compact PCI bus and DSP chip, which greatly improves the reliability and real-time of the system. At the same time, it provides a good interface for application developers, which facilitates the modification of hardware working parameters and improves the flexibility of the system.

References

1. Hu, D., Dong, S.: Research and simulation of information data acquisition in remote experiment, simulation of computer simulation **34**(4), 186–189 (2017)
2. Li, M.: Research on rapid diagnosis of agricultural tractor engine fault based on artificial intelligence. Agric. Mechanization Res. **39**(11), 229–233 (2017)
3. Gao, J.: Artificial intelligence and artificial self healing drive chemical base quality safety. Jiangsu Saf. Prod. **15**(11), 13 (2017)
4. Zhang, H.: Design and implementation of artificial intelligent image detection system based on the Internet of Things. Comput. Meas. Contr. **25**(2), 15–18 (2017)
5. Zhou, R., Zhang, W.: Financial technology innovation risk and control analysis based on large data, artificial intelligence, block chain research. China Manage. Inf. **12**(19), 33–36 (2017)
6. He, X., Shi, W., Li, W., et al.: Based on large data large capacity power electronic system reliability research. China J. Electr. Eng. **37**(1), 209–220 (2017)
7. Yan, A.Q., Tian, J.: Non coal mine mountain intelligent control system design. Metal Mine **3**(2), 113–116 (2017)
8. Wang, X.: The practice of information security in the construction of mobile financial control system based on artificial intelligence **3**(11), 1000–1005 (2017)