A Comparative Study of Power Optimization Using Leakage Reduction Techniques

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Abstract. Designers have scaled down feature sizes, decreasing threshold voltage and allowing the integration of on a single chip, the functionality is becoming increasingly sophisticated. Due to the rapid improvement of semiconductor technology and the growing need for battery-powered portable electronics. To increase the number of devices in a concert, three critical factors are required: system speed, small space, and low power consumption. The entire power consumption of integrated devices is determined by leakage current dissipation in particular. In order to minimize power consumption, the leakage current must be lowered. This study article examines and analyses numerous leakage power reduction techniques, including SC-CMOS and Sleepy keeper. Inverter and Full adder reduction approaches are evaluated in terms of static and dynamic power. In this work, a new strategy for reducing leakage power in 90nm technology is suggested. The suggested approaches will be compared to other leakage reduction strategies that have been used in the past.

Keywords: Full adder · SC-CMOS · Sleepy Keeper · Leakage Power

1 Introduction

The increased use of power electronic devices that run on batteries, such as mobiles and other portable gadgets, may be driving the demand for power leakage mitigation. Leakage power is a serious issue in high-performance applications with low voltage and power. In the past, the overall power dissipation of CMOS devices was dominated by dynamic power. However, as technology continues to scale, leakage power is increasingly becoming a significant source of energy consumption. Many methods for reducing leakage power have been proposed in the past, including forced stack, sleepy stack, sleepy keeper, and SC-CMOS. The leakage power can be calculated by

$$P_{Leak} = V_{dd} * I_{leak}$$

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Many strategies for reducing leakage power have been offered in the past, however new methods for reducing leakage power with 90 nm technology have been proposed. The suggested approaches will be compared to other leakage reduction strategies that have been used in the past. Micro wind 3.1 in 90 nm CMOS technology at room temperature is used to replicate the outcome [1]. They devised a mechanism known as the self-controllable voltage level (SVL) approach, which decreases leakage current considerably. The dissipation of dynamic power is also decreased. We eliminate 93% of leakage current in the suggested approach by adopting a self-controllable voltage level technique in a 1-bit adder, and simulation is performed using a MICROWIND 3.1 and DSCH 2 with 90 nm technology [2]. They discovered that there is an optimal reverse body bias that reduces an IC's standby leakage power usage, which is unique to each technological generation. The total standby leakage power consumption (Psb) of the chip with a reverse body bias Vbs is given by [3]

$$P_{sb} = V_{dd}I_{dd} + (V_{dd} + V_{bs})I_{bp} + V_{bs} * I_{bn}$$

Using stacked sleep transistors, they showed a new way for minimizing static power in CMOS VLSI circuits without sacrificing power delay product requirements or circuit performance [4]. This review paper demonstrates a thorough understanding of the topic of low-power VLSI design. The necessity for the field, its history, its evolution, and its future prospects are all thoroughly examined. At the circuit level, a full assessment of existing leakage reduction techniques is offered. The key ideas of various leakage reduction methodologies are used to simulate a NAND3 gate at a 16 nm technology node for comparison [5]. In this research, a fresh investigation and analysis of several leakage power minimizing approaches has been given. Cadence virtuoso has created a leakage reduction approach, with the combination of stack with sleepy keeper approach. As a result, lowering the leakage power of dynamic logic gates is critical [6]. This paper presents several basic circuits in which power consumption is reduced using transistor size and MTCMOS approach independently, Then using a mix of the two ways, we'll build a circuit that uses less power overall than typical CMOS circuitry [7]. The goal of this study is to provide a leakage reduction strategy that will work for CMOS and fin field effect transistors (FinFET). The usage of electricity will always be a major issue for integrated circuit (IC) designers. Leakage electricity currently accounts for the majority of total power usage, which is a serious problem. The latency for both the new and existing approaches has been estimated, indicating that the suggested methodology is suitable for high-speed circuit applications. To test the performance of the proposed circuit, the authors used higher order gates. The suggested approach is suited for FinFET and deep-submicron CMOS technologies [8]. The components of leakage will be studied and analyzed in this study. A revolutionary enhanced leakage power reduction solution was also demonstrated by integrating Sleepy piled with the LECTOR approach. Two leakage control transistors are inserted between the pull up and pull down circuits. Each existing transistor will be replaced with two half-sized transistors to create the stack effect. It limits the amount of space available due to the requirement of additional transistors to keep the circuit state during sleep mode, using a CMOS switch to introduce a high resistance between the supply and ground. This method will give great leakage current reduction with no additional delay [9]. This research gives an in-depth look at leakage power reduction technologies and approaches, as well as an analysis and comparison. In addition, the benefits and drawbacks of various leakage power reduction solutions are discussed [10]. Weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling are some of the intrinsic leakage processes discussed in this study. The use of channel engineering techniques like retrograde wells and halo doping to reduce short-channel effects in CMOS devices for continuous scaling is explored. Finally, the research investigates several circuit approaches for reducing leakage power usage [11]. This work presents a detailed investigation and analysis of several leakage power mitigation approaches. The current research study and analysis are primarily concerned with circuit performance factors. According to the current literature, a VLSI circuit designer can only perform a sequential analytical approach efficiently if the leakage power minimization strategy is adequate for the application [12]. The purpose of this study is to look at a variety of leakage currents, including those with and without short channel effects. Leakage currents have been widely investigated in relation to a range of causes. Diverse methods for decreasing leakage have also been researched. The effect of leakage on a variety of short channel devices, including the junction less transistor, has been investigated and compared [13]. The DGPT and DGNT and DGNPT are three unique strategies for leakage power reduction that are suggested to be employed in low-power (LP) applications. Sleep transistors with sleep signals are placed between pull-up and pull-down networks to regulate leakage in the suggested ways to reduce leakage power [14]. An 8 × 8 multiplier is constructed in this work employing several leakage power reduction approaches such as MTCMOS, DUAL-Vt, and LECTOR. In 90 nm technology, all of the aforementioned processes are simulated using the Cadence virtuoso tool [15]. Multi-threshold CMOS, Super-Cutoff CMOS, Zigzag, Stack Effect, Input Vector Control, LECTOR, Sleepy Stack, Sleepy Keeper, VCLEARIT, GALEOR, Dual Sleep, Sleepy-Pass Gate, and Transistor Gating are among the leakage reduction approaches compared in this study. The workings, comparisons, and analyses of all of these approaches in various CMOS technologies are thoroughly explored in this study.

During the standby phase of operation, the leakage power is measured. The quantity of leakage in a given circuit is determined by the CMOS technology employed as well as the leakage reduction strategy utilized, it has been observed. This research provides a wide range of leakage power reduction outcomes in CMOS technologies spanning from 180 nm to 45 nm, which will be valuable for future research [16].

2 Design Used

2.1 Half Adder

In this we compared the inverter circuit with the three designs and also with proposed design. We used normal inverter as shown in the figure. We compared the static and dynamic power, delay and average power. This inverter circuit is used for all the designs and the output graphs are shown in the results section (Fig. 1 and Table 1).

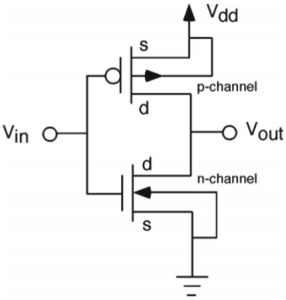

Fig. 1. Inverter Circuit

Table 1. Inverter Truth Table

Input	*output*
0	1
1	0

2.2 Full Adder

We compared the whole adder circuit to the three existing designs as well as the new design. As seen in the diagram, we used 16 complete transistors. The static and dynamic power, as well as the delay and average power, were compared.

Leakage Reduction Techniques Survey:

In today's integrated circuits, low power design is a must. I intend to cover the fundamental techniques of low-power design in this essay, regardless of the tools used. Battery backup time became increasingly crucial as firms began to load more and more functions and applications into battery-operated gadgets. Customers' power usage becomes an increasingly relevant criterion over time. As a result, all chip vendors are concentrating on reducing power usage. Efforts are being made to minimize both dynamic and static power usage. Companies began to lower the nominal voltages inside the semiconductor, but this, too, was restricted by technology. As a result, a variety of low-power design strategies began to be used during the Chip (Fig. 2 and Table 2).

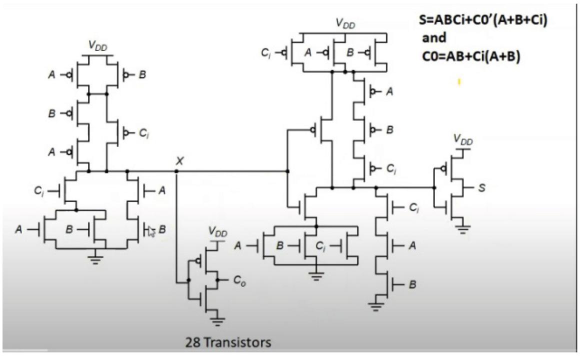

Fig. 2. 16 transistor Full adder Circuit

Design process in order to minimize both static and dynamic power usage. The following is a list of some of the most popular and widely used Low Power Design Techniques. 1. Clock Gating. 2. Power Gating. 3. Dynamic Voltage and Frequency Scaling. 4. RPG. 5. Save and Restore Power Gating.

Table 2. Full adder Circuit Truth Table

a	*b*	*c*	*Sum*	*carry*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.3 Multi Threshold CMOS (MTCMOS)

In MTCMOS, an SLEEP transistor is made by connecting the power supply and ground to high threshold devices in series with low threshold transistors (as shown in fig). Because there is a route between the supply and the ground in active mode, the sleep transistors are turned on, allowing regular functioning to continue. The sleep transistors are switched off in standby mode, which turns off the circuit's power source and establishes virtual supply and ground rails. Pull up and pull down networks employ low threshold voltage transistors. As sleep transistors, high threshold voltage transistors are employed (Figs. 3 and 4).

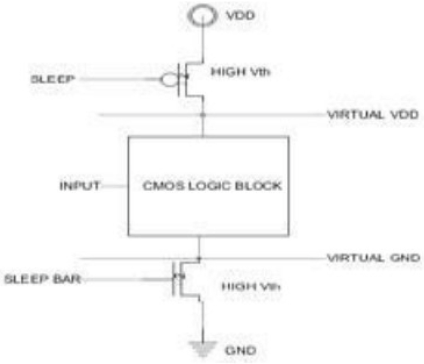

Fig. 3. MT-CMOS

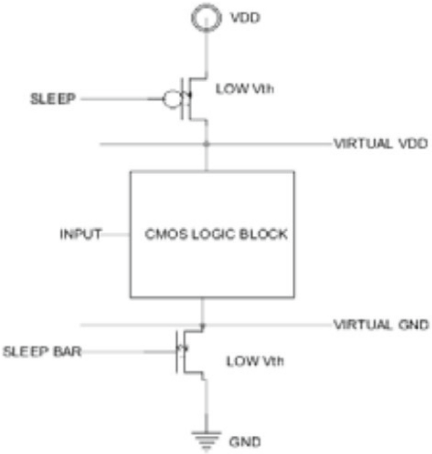

Fig. 4. SCCMOS

2.4 Super Cutoff CMOS (SCCMOS)

The super cut-off technique avoids multiple-threshold devices in a logic circuit. The super cut-off strategy reduces leakage current by using a single kind of threshold voltage device.

This technology is known as super cut-off CMOS when it is utilized for CMOS logic (SCCMOS). The purpose of this method is to avoid weak inversion current by placing the transistors in a super cut-off state during standby mode. For this, the charge pump circuit is employed at the transistor's input. The device enters a super cut-off state when the input voltage is less than the ground potential for NMOS devices or greater than the power supply voltage for PMOS devices. The charge pump circuit generates the required input signals and helps to prevent excessive leakage currents. When a charge pump circuit is included in a logic block, it generates unwanted parameter setting, resulting in a significant delay.

2.5 Sleepy Keeper Circuit

Between the draw up network and Vdd and the pull down network and GND, a paralleled connection of PMOS and NMOS transistors is established in this technology, with the NMOS transistor of the pull up sleep transistor coupled to the PMOS pull down sleep transistor. Because the GND-connected NMOS sleep transistor and the GND-connected PMOS transistor, which is connected to Vdd, is not turned on, the NMOS transistor will not efficiently pass Vdd. Keep the output value "1" in sleep mode and attach the NMOS to Vdd to fix this problem. A PMOS transistor is connected to the pull up NMOS transistor and GND is parallel to the NMOS sleep transistor to keep the output value equal to "0" in sleep mode. This technology efficiently reduces leakage power while preserving acceptable logic in a smaller circuit (Fig. 5).

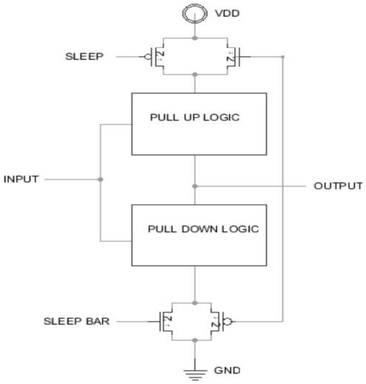

Fig. 5. Sleepy Keeper Circuit

3 Proposed Design

The MTCMOS approach has been tweaked for this application. The NMOS HVT sleep transistor is made as a stack of two transistors with twice the width of the original one in this design. When more than one OFF transistor is present in the route, the state is significantly less leaky than when only one OFF transistor is present. This improved method dramatically decreases leakage power when compared to the previous method.

This is built on dual threshold voltage transistors, where high voltage transistors serve as sleep transistors and low voltage transistors serve as logic blocks in CMOS (Fig. 6).

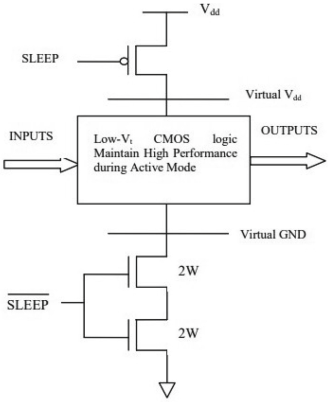

Fig. 6. Proposed Design Circuit

4 Simulation Results and Experimental Analysis

We did the comparative analysis for full adder and inverter for the three designs SC-CMOS, MTCMOS, sleepy Keeper and the proposed design.

4.1 Inverter Outputs

We have implemented the circuit in cadence tool as shown in below figures. Normal inverter circuit implementation. The static power graph for normal inverter is dynamic power graph (Figs. 7 and 8).

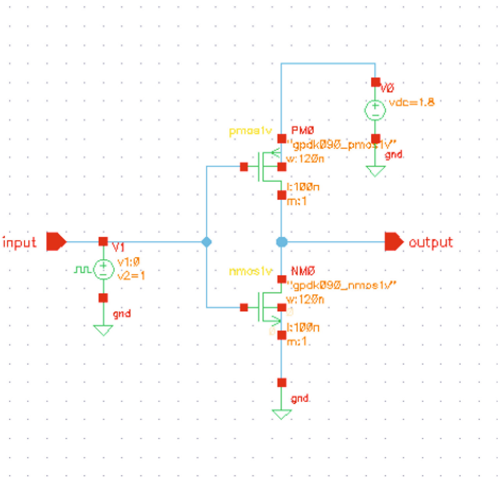

Fig. 7. Normal inverter Circuit

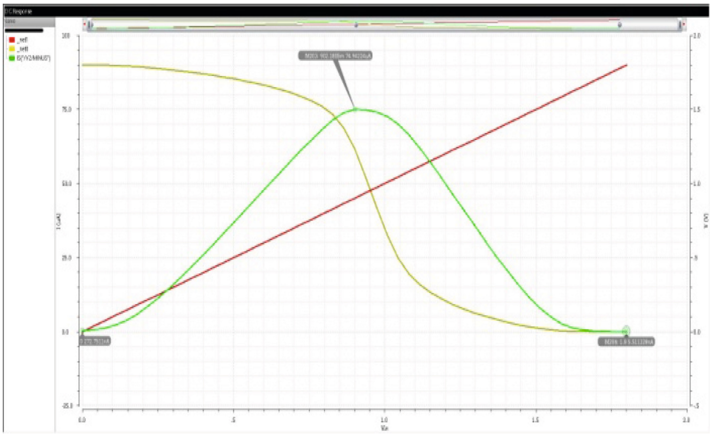

Fig. 8. Normal inverter Static Power graph

4.2 SC-CMOS Inverter

Super cut off inverter circuit implementation which consists of Low threshold transistors? (Fig. 9).

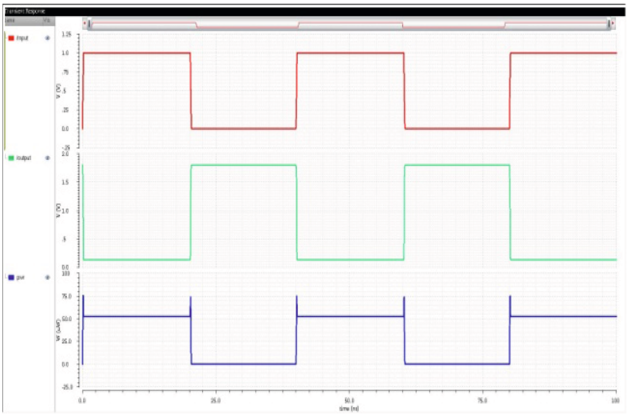

Fig. 9. Normal inverter Dynamic Power graph Circuit

The static power graph for SC-CMOS inverter is given below, implemented in cadence. Where the static power is calculated without changing inputs Dynamic power graph (Fig. 10).

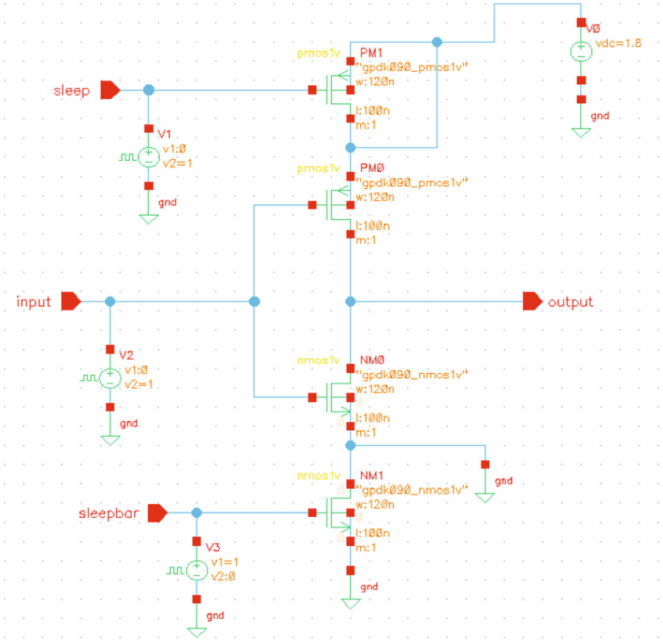

Fig. 10. SC-CMOS inverter Circuit

4.3 MT-CMOS Inverter

MT-CMOS inverter circuit implementation The static power graph for inverter is implemented in cadence as shown below dynamic power graph (Figs. 11, 12, 13, 14, 15, 16, 17 and 18).

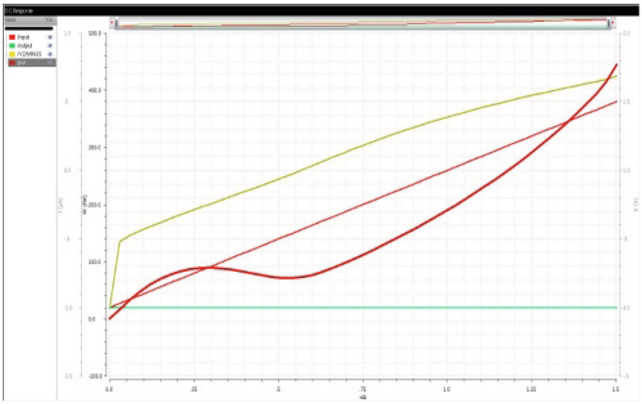

Fig. 11. SC-CMOS inverter Static Power graph

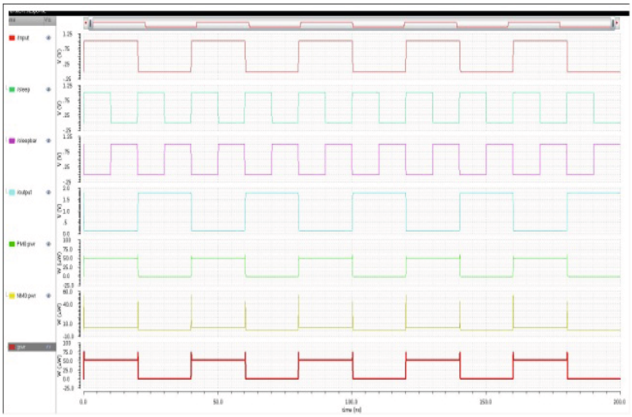

Fig. 12. SC-CMOS inverter Dynamic Power graph Circuit

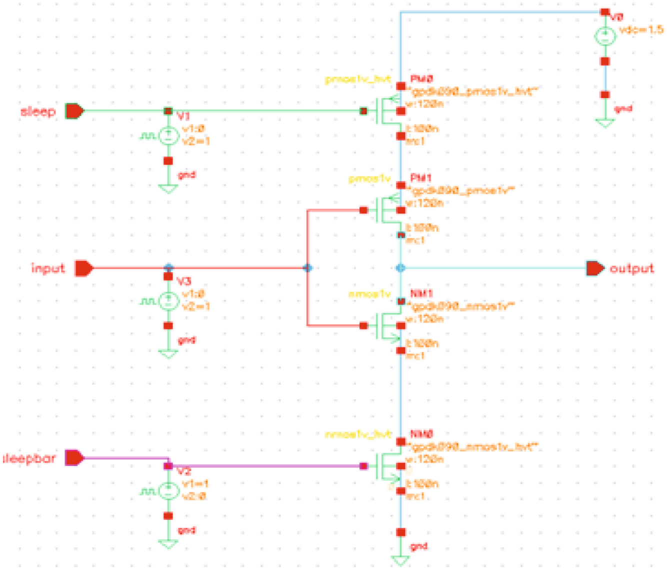

Fig. 13. MT-CMOS inverter Circuit

4.4 Proposed Inverter Circuit

Inverter circuit implementation the static power graph for proposed inverter is Dynamic power graph (Figs. 19 and 20).

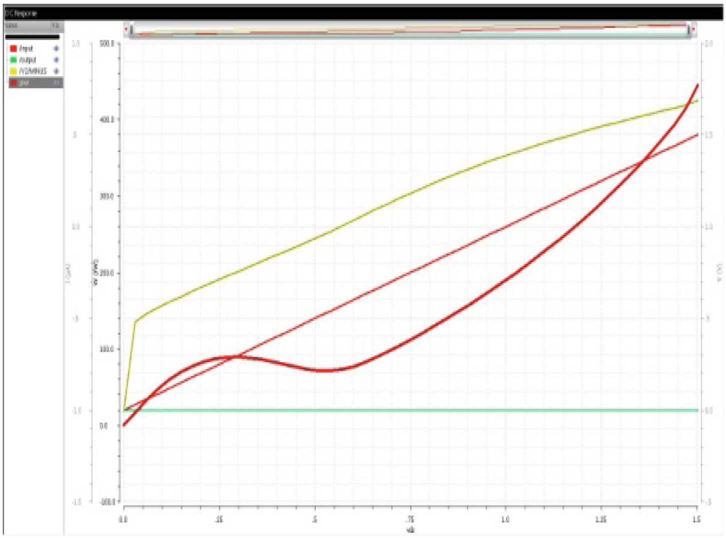

Fig. 14. MT-CMOS inverter Static Power graph

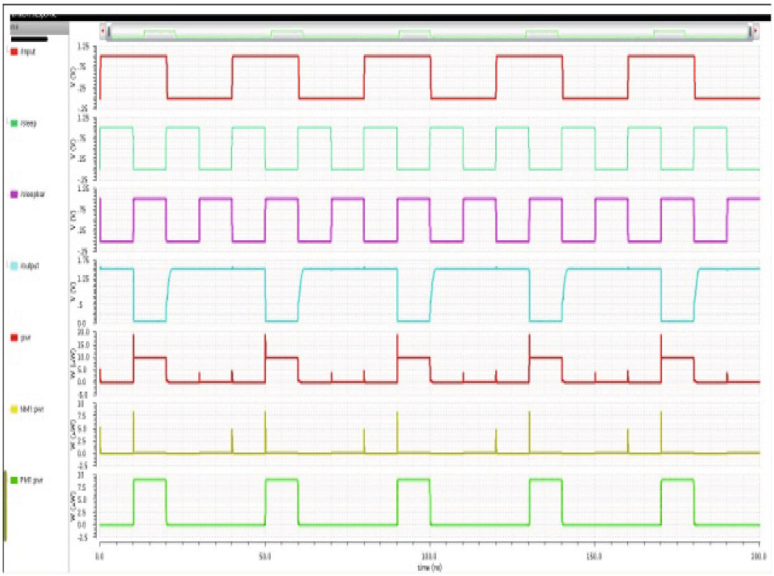

Fig. 15. MT-CMOS inverter Dynamic Power graph Circuit

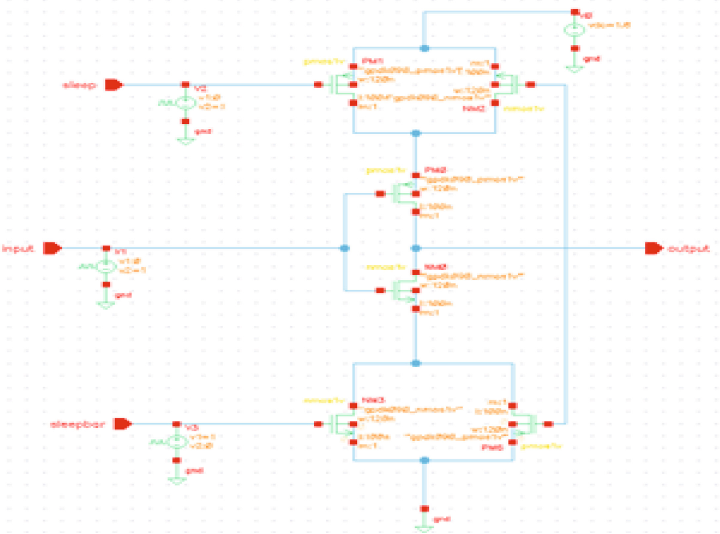

Fig. 16. Sleepy Keeper Inverter Circuit

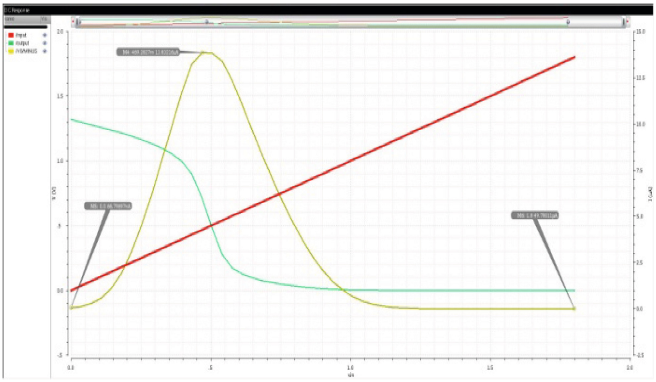

Fig. 17. Sleepy Keeper inverter Static Power graph

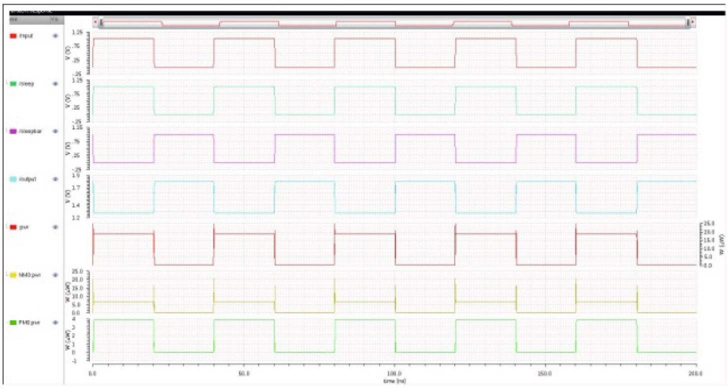

Fig. 18. Sleepy Keeper inverter Dynamic Power graph Circuit

Fig. 19. Proposed inverter Circuit

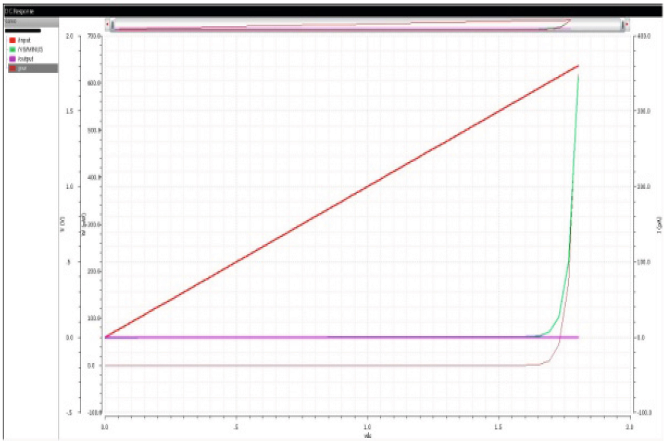

Fig. 20. Proposed inverter Static Power graph

4.5 Full Adder Outputs

Normal Full adder: In this we have implemented 16 transistor full adders for all the designs. Static power graph: In the absence of any design activity, static power, often known as “leakage,” is consumed. It’s closely linked to the current flowing through the transistor in its idle state, which is dictated by the transistor’s characteristics (Figs. 21 and 22).

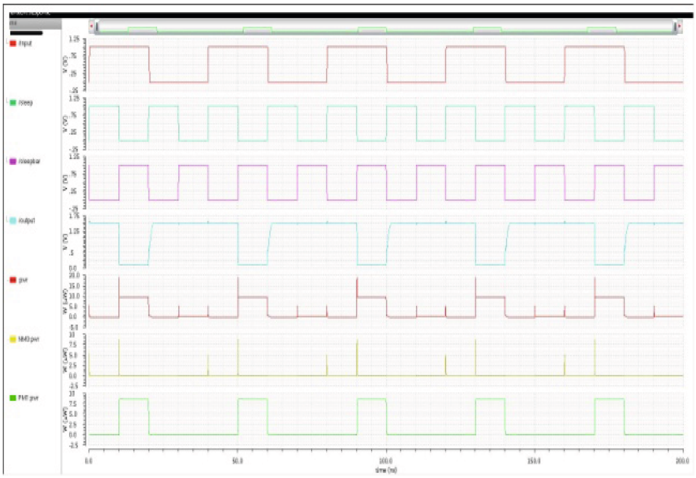

Fig. 21. Proposed inverter Dynamic Power graph Circuit

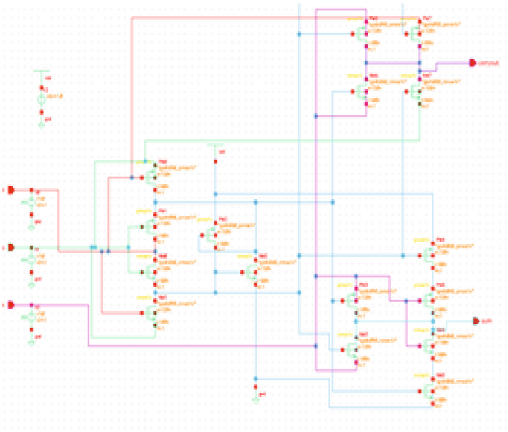

Fig. 22. Normal Full adder Circuit

Dynamic power graph: The majority of the power expended in circuits is dynamic power, which also contributes to peak power. It is determined by three factors: supply voltage, switching frequency, and output load. Short circuit power and switching power are the two fundamental components of dynamic power (Figs. 23 and 24).

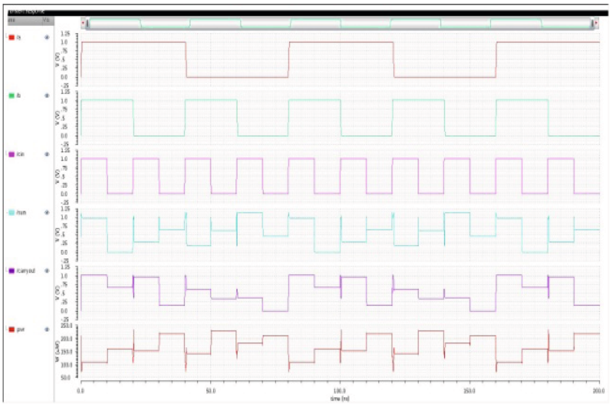

Fig. 23. Normal full adder Dynamic Power graph Circuit

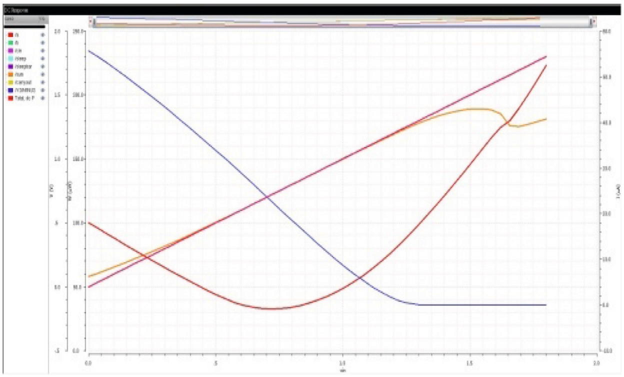

Fig. 24. SC-CMOS Full adder Static Power graph

4.6 SC-CMOS Full Adder

Static power graph and dynamic power graphs are presented (Figs. 25 and 26)

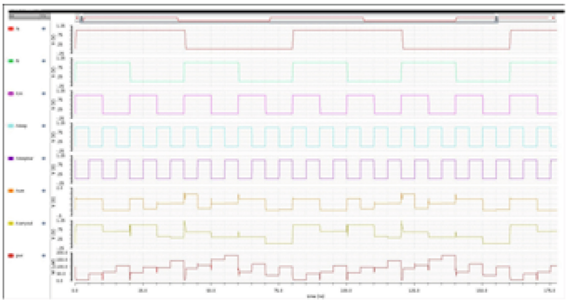

Fig. 25. SC-CMOS full adder Dynamic Power graph Circuit

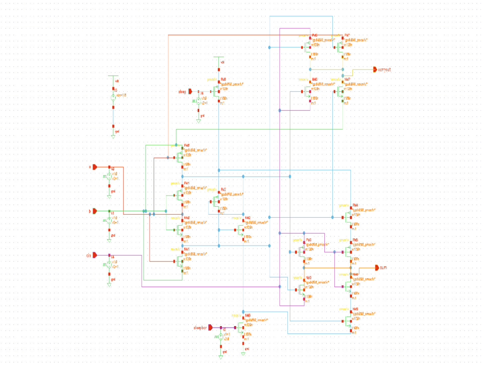

Fig. 26. SC-CMOS Full adder Circuit

4.7 Sleepy Keeper Full Adder

Static power graph and dynamic power graphs are presented (Figs. 27, 28 and 29)

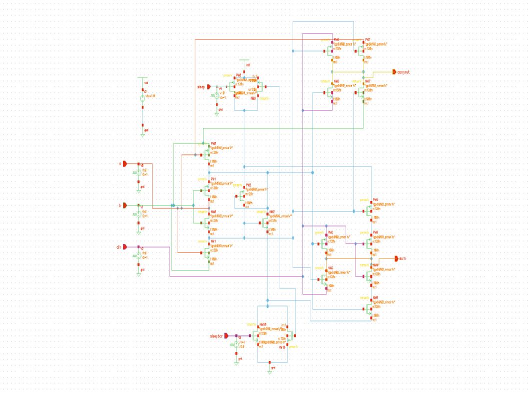

Fig. 27. Sleepy keeper full adder Circuit

On comparing all three techniques and proposed technique the static power and Dynamic power has been reduced. Comparison of delay, average power and static power for inverter (Table 3, Figs. 30, 31, 32 and Table 4).

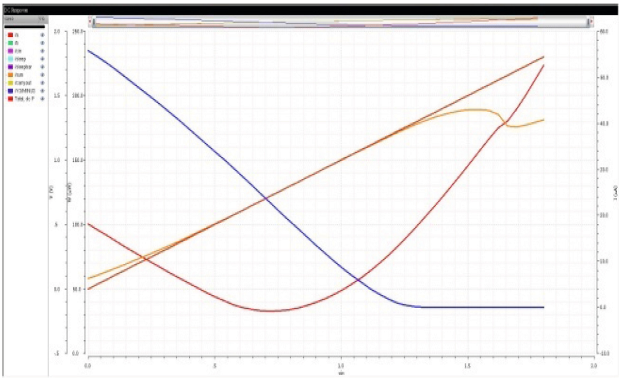

Fig. 28. Sleepy keeper Full adder Static Power graph

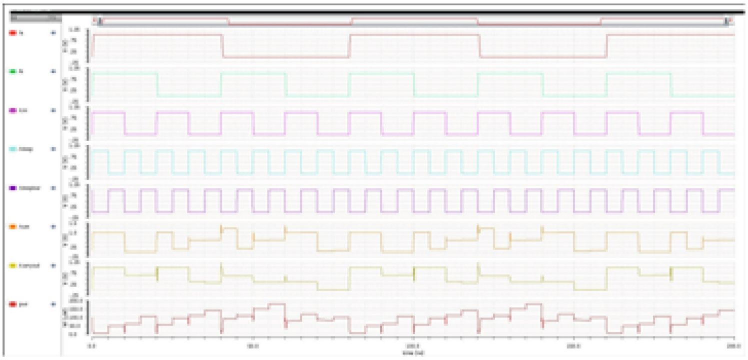

Fig. 29. Sleepy Keeper full adder Dynamic Power graph Circuit

Table 3. Comparison of delay, average power and static power for inverter

Design	Delay (pW)	Average power (mW)	Static Power (mW)
Normal	38.74	66.59	134.895
SC-CMOS	38.72	36.87	73.764
MT-CMOS	30.04	2.483	29.6 nW
Sleepy Keeper	60.05	11.01	24.894
Proposed	34.25	2.132	11.14 nW

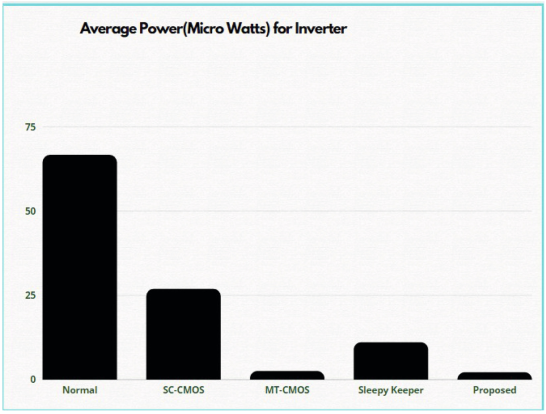

Fig. 30. Comparing Average power for inverter

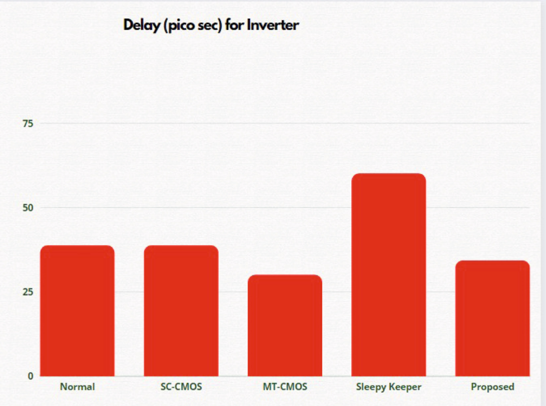

Fig. 31. Comparing Delay for inverter

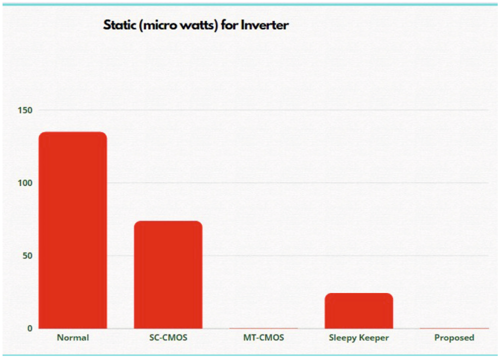

Fig. 32. Comparing Static for inverter

Table 4. Comparison of delay, average power and static power for inverter

Design	Average power (mW)	Static Power (mW)
Normal	165.7	183.2
SC-CMOS	90.36	85.88
MT-CMOS	60.24	56.84
Sleepy Keeper	92.3	80.91
proposed	45.19	50.19

5 Conclusion

In this project we have compared several leakage reduction techniques and came up with a new technique which is based on Dual threshold transistors. The average power for inverter (compared to proposed design) is reduced almost 96.7%. The static power is reduced around 99% for inverter. For full adder the average power is reduced by 70%. The static power is reduced by 72.6%.

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