Design of 8-bit 2 GHz Current-Steering DAC

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Abstract. In this paper, an 8-bit 2 GHz current steering DAC based on SMIC 55 nm CMOS process is designed. The design is mainly divided into two parts: analog part and digital part. The analog part contains a bandgap reference voltage source providing a small temperature coefficient reference voltage, a bias voltage generation circuit and a current source consisting of a cascode current mirror, while the digital part mainly contains an input register, a dual 4-bit thermometer decoder and a switch driver. After the digital signal is input, it is first synchronized by the clock drive register and uniformly input into the high and low thermometer decoders, and then the switch driver module translates the decoded signal into a high cross-point drive signal to ensure that the NMOS switches of the current source do not turn off simultaneously, ensuring the accuracy and stability of the output signal.

By improving the structure of the low-voltage cascode current mirror, the DAC obtains better output stability at low voltage. The overall simulation of DAC using EDA tool shows that the start-up time of DAC is less than 0.5 ns under the pre-simulation condition of 27 °C, and the DNL is 0.375 LSB and INL is 0.492 LSB at 2 GHz sampling frequency, which proves that DAC has good working ability at this frequency.

Keywords: Digital-to-analog (DAC) · CMOS · Current-steering

1 Introduction

1.1 Research Background and Significance

In recent years, with the development and improvement of Internet technology, more and more industries are gradually integrated with the Internet. In this process, DACs convert digital signals to analog signals. They are usually used as output channels of process control computer systems connected to actuators to automate production processes. In certain high-tech industries, the output response speed of precisely controlled processes has become an increasing concern. For real-time control and detection of rapidly changing signals, DACs require high conversion speeds. As a result, there is a growing need to design high-speed DACs.

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1.2 Current Status of Domestic and International Research

With the development of IC processes, CMOS has become the mainstream process for IC design today due to its advantages of high integration, low power consumption, good reliability, short design cycle and low price [1]. CMOS has become the dominant process in today's IC design with its advantages of high integration power, reliability, short design cycle time and low price. It plays an important role in the design of high performance data conversion circuits.

In foreign countries, the research of high-speed high-precision DAC is mainly conducted by independent companies and universities; in China, the relevant research is led by universities and research institutes, and a lot of human and material resources have also been invested. However, due to the influence of technology level, there is still a big gap between domestic DAC research and the world advanced level compared with the international level. Therefore, it has become an important task for domestic DAC research to strengthen technology development and innovation, and continuously improve DAC performance and application scope.

In this section, this paper will specifically introduce the current research status of DAC at home and abroad, in order to better understand the development status and future trends of DAC.

Status of Foreign Research

In the field of digital-to-analog converters, after years of development abroad, universities and some leading companies have taken the lead in the research of high-speed and high-precision DACs.

At present, foreign high-speed high-precision DAC has formed a complete industry chain, covering major applications. Among them, ADI, TI, MAXIM and other companies are most representative.

Unlike the products with practicality from foreign related companies, the academic community in foreign universities focuses more on the improvement of DAC performance by novel architectures.

Current Status of Domestic Research

Compared with foreign countries, the domestic IC industry started late and there is a big gap with the international advanced level so far. However, with the progress of domestic IC industry and with the strong support from the state, domestic research institutes, universities and enterprises have conducted a lot of research on DAC and achieved good research results.

Among them, the most representative one is the 6-bit 30 GSPS sampling frequency DAC developed by the Institute of Microelectronics, Chinese Academy of Sciences, which has made a breakthrough in the domestic DAC industry. Among them, the 6-bit segmented current-steering DAC core with a speed of 30 Gsps, integrated with three error correction circuits, 4–1 MUX high-speed circuit, delay deviation calibration circuit and 24-way high-speed serial data receiver, can achieve full-rate output at 30 Gsps sampling frequency, and the test results are shown in Fig. 1. Under the low input signal frequency, the SFDR reaches 44 dB, and the SFDR is greater than 28.5 dB for the whole Nyquist input range [2].

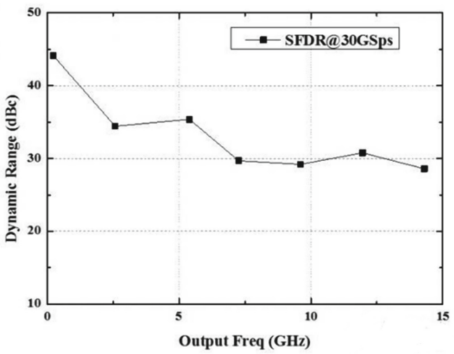

Fig. 1. SFDR schematic of the 6-bit 30 Gsps sampling frequency DAC developed by the Institute of Microelectronics, Chinese Academy of Sciences [2]

The design uses R-2R ladder network and high voltage folding cascode op amp as buffer output to ensure good monotonicity of DAC and improve radiation resistance [3].

Xi'an University of Electronic Science and Technology has designed a 6-bit high-speed segmented current rudder DAC, which is compatible with the input clock frequency range from 1 GHz to 33 GHz, while ensuring the synchronization of the clock signal, with strong driving capability and high-frequency anti-interference capability [4]. Chao Huang et al. proposed a new DAC component design scheme, which contains three parts: counter circuit, comparison circuit, and PWM wave rectification circuit. The counter generates a counting cycle in M-decimal mode, and then inputs the corresponding output state value to the multi-bit comparison circuit. The increasing data of the counter is constantly compared with the preset initial value in the multi-bit comparison circuit, and the multi-bit comparison circuit outputs high and low levels to form a PWM wave with corresponding duty cycle. The design has the advantages of low cost and simple structure, which can avoid the high cost of PWM wave output by microcontroller, and is a simple and effective new DAC design solution to meet the requirements of low frequency DAC [5]. It is a simple and effective new DAC design to meet the low frequency DAC requirements. The 24-bit DAC with 1 MSPS sampling frequency designed by University of Electronic Science and Technology is designed with multiple parallel DACs to increase the resolution of the converter, while pre-processing the input digital signal and using interleaved phase signals to suppress distortion [6]. Southeast University has optimized the structure of the bandgap voltage source to adapt to the low-voltage operating environment, and realized a 500 MHz sampling rate 14-bit DAC design under 1.1 V low-voltage power supply [7].

1.3 Research Content of This Paper

This paper focuses on DAC research, after reviewing the aforementioned large amount of domestic and international research literature, using current rudder structure, and after several trials using SMIC 55 nm process, finally successfully achieved a higher accuracy

conversion result of INL and DNL both less than 0.5 at 2 GHz clock frequency. The specific research content of this paper is as follows:

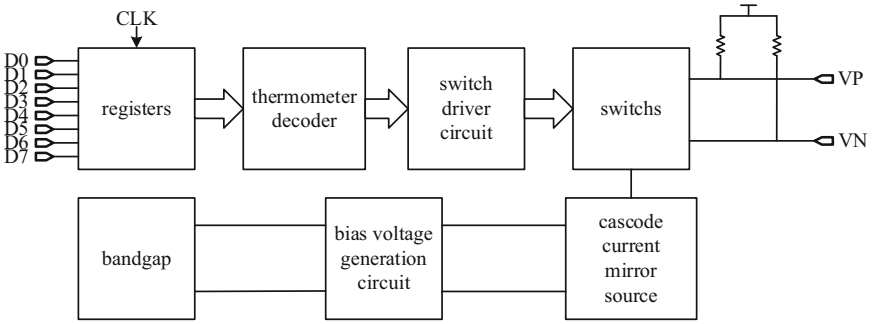

Fig. 2. 8-bit DAC overall structure design diagram

First, the DAC design is carried out. The design adopts a modular design approach, dividing the overall DAC circuit into two major parts: digital and analog. The analog part includes three major modules: bandgap voltage source, bias voltage generation circuit, cascode current mirror source and its switch. As shown in Fig. 2, the digital part includes registers, 4–15 thermometer decoder, and switch driver circuit. After the digital signal is input, it is uniformly input into the high and low 4–15 thermometer decoders through the clock drive register to ensure the synchronization of the signal. Meanwhile, the switch drive module translates the decoded signal into a high cross-point drive signal to ensure that the NMOS switches of the current source do not turn off at the same time to ensure the accuracy and stability of the output signal.

Then, pre-simulation was performed to verify that the actual performance of the design met the design objectives.

1.4 Overview of DAC

As shown in Fig. 3, after the digital signals $d_0 \sim d_{n-1}$ are input to the decoding circuit, the decoding circuit outputs the decoding result and controls the weighting network to output the corresponding voltage. Using the reference voltage source as the total output reference voltage, the output stage voltage output equation is shown in Eq. 1.1:

$$V_{out} = kV_{LSB}\left(2^{n-1}d_{n-1} + 2^{n-2}d_{n-2} + \cdots + 2^{0}d_{0}\right) \tag{1.1}$$

where k is the scaling factor that adjusts the voltage output range, V_{LSB} is used as the least significant bit of the analog output, which is superimposed as each significant bit of the digital code is turned on, noted as 1 LSB, for N-bit DACs with:

$$V_{LSB} = \frac{V_{REF}}{2^{N}} \tag{1.2}$$

where V_{REF} is the reference voltage.

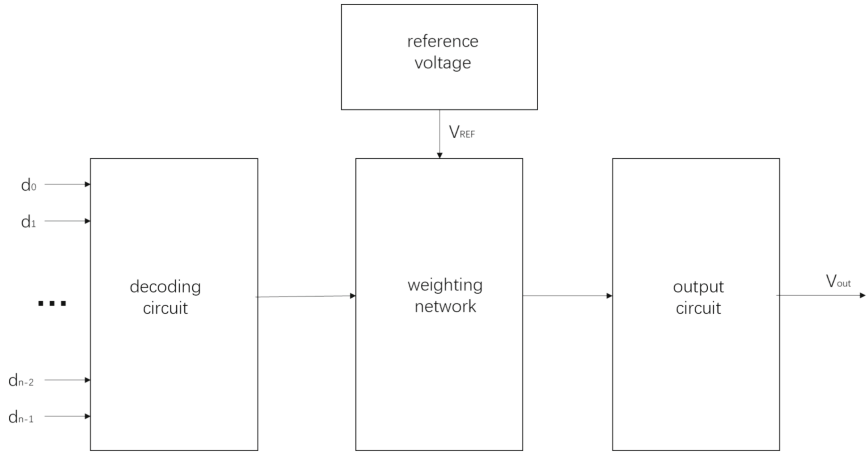

Fig.3. Digital-to-analog conversion schematic

1.5 Research Overview of This Paper

In this paper, the research is focused on DAC, and after reviewing the aforementioned domestic and international research literature, the current-steering structure is adopted, and after several experiments using SMIC 55 nm process, the conversion of INL and DNL at 2 GHz clock frequency is successfully achieved, which are both less than 0.5 LSB at 2 GHz clock frequency with high accuracy.

Firstly, the research on the principle and classification of DAC, performance parameters and the current status of DAC research at home and abroad is conducted, and the design objectives and overall design scheme are defined.

Then, the DAC design is carried out. This design adopts a modular design approach, dividing the overall DAC circuit into digital and analog components. The analog part includes bandgap voltage source, bias voltage generation circuit, cascode current source and its switch. The digital part consists of three modules: the memory, the 4–15 thermometer decoder, and the switch driver circuit. After the digital signal is input, it is uniformly input into the high and low 4–15 thermometer decoders through the clock-driven registers to ensure the synchronization of the signals, then the switch driver module translates the decoded signal into a high cross-point drive signal to ensure that the NMOS switch of the current source does not turn off at the same time to ensure the accuracy and stability of the output signal.

Finally, pre-simulation is performed to verify that the actual performance of the design meets the design objectives.

2 Bias Voltage Generation Circuit Design

The bandgap voltage source circuit can generate a reference voltage with an approximate zero temperature coefficient, but the current source array needs to be implemented by a current mirror structure, which requires the conversion of the reference voltage into

a reference current and then generating a bias voltage. Figure 4 shows the bias voltage generation circuit schematic. In the figure, Vref is the input port of the reference voltage, while Vcas and Vcs are the output ports of the bias voltage of the common gate tube and current source tube, respectively.

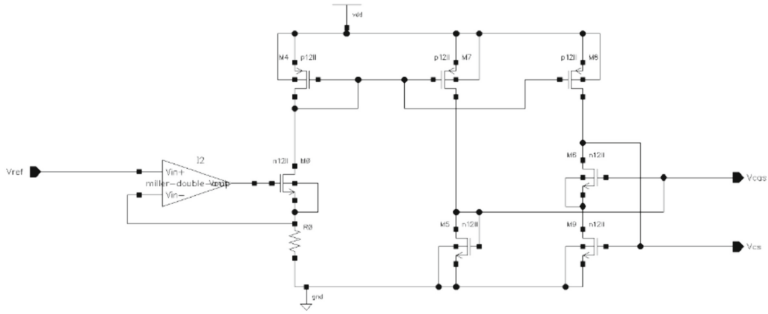

Fig. 4. Circuit diagram of bias voltage generation circuit

The main function of the current mirror bias circuit is to provide a bias voltage for the current source array by applying the input reference current. In order to obtain a high output impedance current source, a cascode current mirror structure is used for the bias circuit.

The right half of Fig. 4 forms the cascode bias voltage generation circuit. Since the supply voltage is low, only 1.2 V, a modified low-voltage cascode current mirror structure is used for the design [8]. The M4, M7 and M8 tubes are of the same size and together form the current mirror, which copies the reference current generated by the voltage-to-current circuit into the two branches. M6 and M9 tubes are of the same size as the current source and together with the current source tube form the cascode current mirror, where Vcas is the bias voltage of the common gate tube and Vcs is the bias voltage of the current source tube. The M5 tube has a smaller aspect ratio than the M6 and M9 tubes, which allows it to obtain a larger gate voltage, making the drain voltage of the M9 tube increase and making all MOS tubes work in the saturation region.

3 Overall Simulation of 8-bit 2 GHz Digital-To-Analog Converter

3.1 Static Performance Simulation

Under the condition of 27 °C, a clock signal with a period of 500 ps and a swing of 1.2 v is input at the clk end, and the $d_0 \sim d_7$ end of the input period of 1 ns, 2 ns, 4 ns, 8 ns, 16 ns, 32 ns, 64 ns, 128 ns in turn, simulate the change of the 8-bit digital signal from all 0 to all 1 at 2 GHz clock frequency with 1 GHz input, and the differential output results are shown in Fig. 5. The horizontal coordinate of the figure is the digital code growing with time, and the vertical coordinate is the differential output result

$$V_{out} = V_P - V_N \tag{3.1}$$

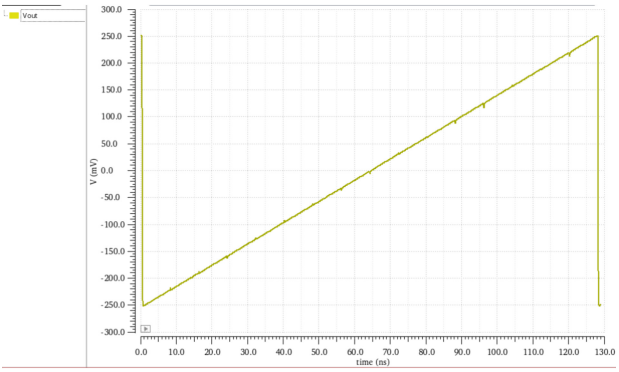

Fig. 5. Differential output results at 2 GHz clock frequency input

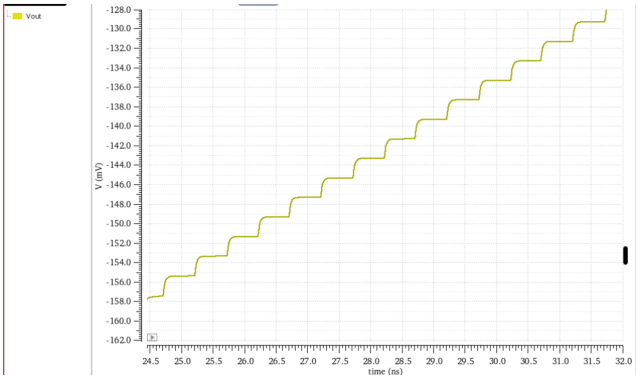

Fig. 6. Partial enlargement of differential output results at 2 GHz clock frequency input

As seen in Fig. 6, a continuous step waveform is visible after zooming in, and the output structure as a whole has a linear growth trend, which proves that the DAC can work properly under this simulation condition. At the same time, burr appears every 16 bits, which is caused by the lower bit falling time being larger than the higher bit rising time when feeding from the lower bit to the higher bit.

The voltage at that point is taken every 500 ps on the level step, and the INL and DNL of the DAC are calculated using Matlab tools, and the visible error simulation results are shown in Figs. 7 and 8.

It can be seen that the maximum value of INL is about 0.375 LSB and the maximum value of DNL is about 0.492 LSB, which are both less than 0.5 LSB and meet the design index. Among them, both INL and DNL extreme value points are located at 16-bit interval points, which are consistent with the previous burr points and are caused by the low and high bit feeds.

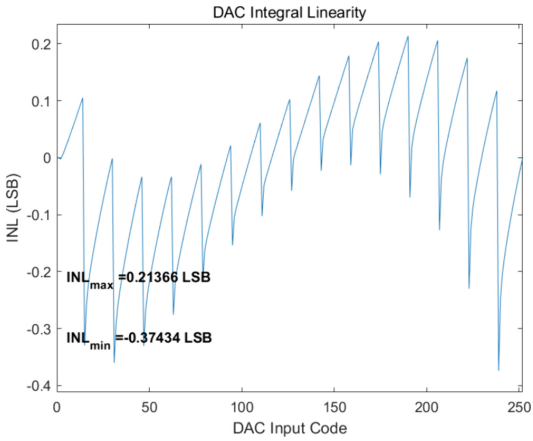

Fig. 7. INL simulation results at 2 GHz clock frequency input

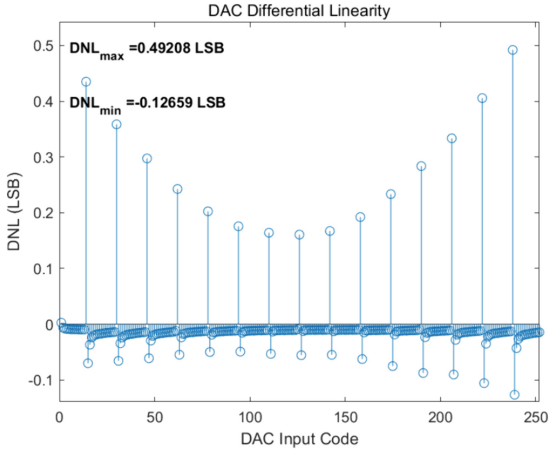

Fig. 8. DNL simulation results at 2 GHz clock frequency input

3.2 Dynamic Performance Simulation

Establishment Time

At the digital signal input of DAC $d_0 \sim d_7$ end is connected to the step signal generator at the same time and triggered uniformly at 5 ns, the analog input digital signals all switch from 0 to 1 change. Measure the time for the output analog signal to stabilize within the theoretical value of $\pm$ 0.5 LSB, and subtract 5 ns from this time to the establishment time of the DAC.

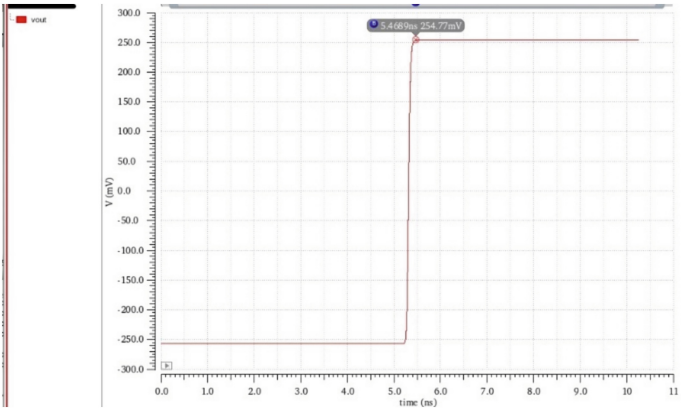

Fig. 9. DAC build time simulation result graph

As shown in Fig. 9, the simulation result of DAC build-up time is shown, whose vertical coordinate is the output voltage and horizontal coordinate is the simulation time. It can be seen that when the output analog signal is stable within the theoretical value of ±0.5 LSB, the time is 5.4689 ns, so the establishment time of DAC in this design is 0.4689 ns.

Considering the influence of establishment time on DAC, the output signal period should not be smaller than the establishment time, then the clock frequency should not be larger than 2 GHz, so 2 GHz is chosen as the final sampling frequency of this design.

Spurious-Free Dynamic Range

For dynamic performance simulation, the input signal is converted into the corresponding digital signal using an ideal ADC, and then input into the DAC in this design. The SFDR of the DAC in this design can be obtained by simulating and analyzing the DAC output mapping, and the relationship between the input signal frequency and clock frequency during simulation is as follows:

$$f_{in} = \frac{n}{N} f_{clk} \tag{3.2}$$

where f_{in} is the frequency of the input sine wave, f_{clk} is the clock frequency, N is the total number of bits and is taken as 256, and n is the number of output periods of the sine wave, which is generally less than half of N and is mutually prime with N. Simulations were performed at 27 °C using the TT process angle:

When f_{clk} is 2 GHz and n is taken as 3, the f_{in} approximation is taken as 10 MHz, its simulation output waveform is shown in Fig. 10, and the spectrum is shown in Fig. 11, which yields SFDR = 57.0447 dB.

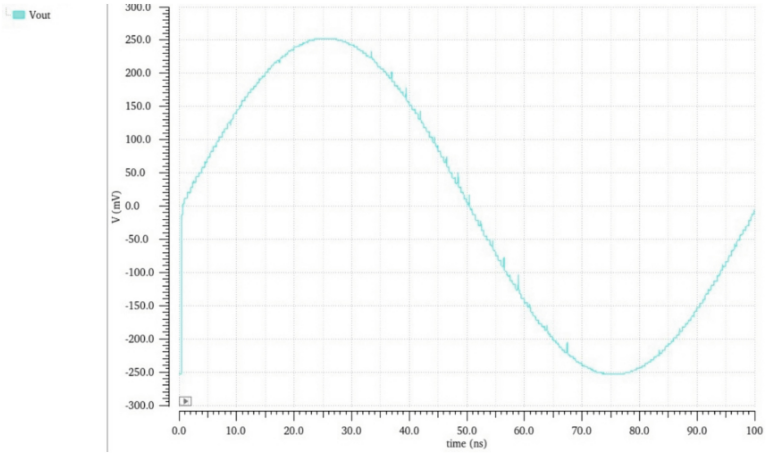

Fig. 10. Output waveform at 10 MHz input

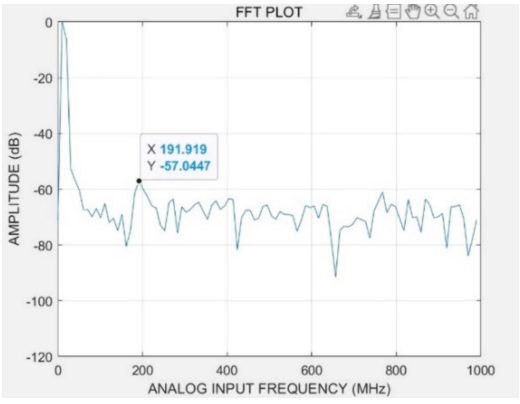

Fig. 11. Output spectrum at 10 MHz input

When f_{clk} is 2 GHz and n is taken as 115, the f_{in} approximation is taken as 900 MHz, the simulation output waveform is shown in Fig. 12 and the spectrum is shown in Fig. 13, which yields SFDR = 50.0262 dB.

It can be seen that the SFDR of the DAC near the Nyquist frequency is still 50.0262 dB, which meets the design specification.

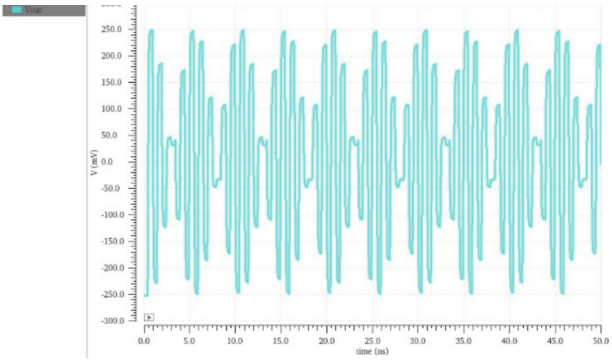

Fig. 12. Output waveform at 900 MHz input

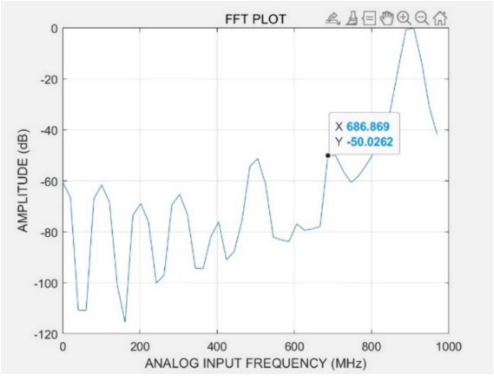

Fig. 13. Output spectrum plot at 900 MHz input

4 Summary

Based on a survey of the current status of DAC research at home and abroad and a discussion of the basic principles and structure of DACs, this paper designs a high-speed DAC that has a wide range of applications in various industries. After comprehensive testing of the performance of DACs designed under different processes, the SMIC55 nm process is selected as the design process, and an 8-bit segmented current rudder DAC is designed, which can operate normally at clock frequencies up to 2 GHz, with an INL of 0.375 LSB and a DNL of 0.492 LSB, both less than 0.5 LSB, meeting the design specifications. The experiment proves that the segmented row and column decoder thermometer decoder, high cross-point drive signal circuit, differential output switch, and low-voltage current mirror current source used in this DAC design effectively improve the circuit performance and achieve the design specifications.

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