Design of Intelligent Education Management Information System in Colleges and Universities from the Perspective of Big Data

Haiyan Zhao[1(✉)], Shiyuan Liu[1], Lin Xiao[1], Kun Liu[1], and Fuxia Liu[2]

[1] Beijing Union University, Beijing 100101, China
dwew562333@163.com
[2] Scientific Research Department, Hebei Open University, Shijiazhuang 050080, China

Abstract. There are many internal data types in the education management information system, which leads to the poor management effect of the intelligent education management information system in colleges and universities. Design an intelligent education management information system in Colleges and universities from the perspective of big data. The hardware part of the system focuses on the design of DSP module, FPGA module, analog-to-digital conversion module, A/D conversion module interface circuit and communication interface. In the system software part, the big data technology is used to divide and allocate data sets, so as to realize the design of intelligent education management information system in colleges and universities. Experimental results show that the proposed intelligent education management information system can effectively improve the accuracy and efficiency of resource mining, and has a good effect.

Keywords: Big data horizon · Education management information · Excavate · Transformation · Clustering · Match

1 Introduction

As one of the landmarks of the information age, big data is widely used in all aspects of society. Big data is a new thing gradually evolved with the rapid growth of massive data. It is different from traditional data. It has a huge volume, a wide variety of data, and the correlation between data is very complex, which has a great impact on business, education and culture [1]. The development of science and technology promotes the continuous progress of Internet technology. Big data is widely used in college teaching management information system.

Big data is essentially produced with the in-depth development of the Internet, and it is still in a blowout development. This is the era of massive information storage, and its real significance lies in the analysis and use of data. Through continuous mining, data can play a real role. In fact, the proposal of big data also brings development opportunities and new challenges to colleges and universities in the forefront of science and technology, which requires college education to actively comply with the development of the trend

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of the times. Therefore, taking advantage of the advantages brought by big data, we should constantly innovate college teaching management information system and build a new college education model. The hardware part of the college intelligent education management information system under the vision of big data focuses on the design of DSP module, FPGA module, analog-to-digital conversion module, A/D conversion module, interface circuit and communication interface. In the system software part, the big data technology is used to allocate data sets to achieve the design of the college intelligent education management information system.

2 System Hardware Framework

The hardware framework of the whole system is shown in Fig. 1:

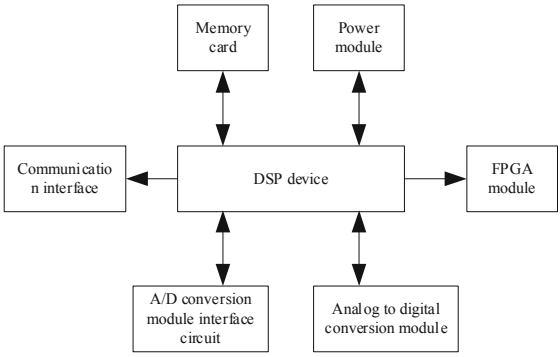

Fig. 1. System hardware framework

Among them, DSP device is a professional data processor, which can realize the high-speed processing of a large number of data and the operation of complex algorithms, and has won the favor of the majority of designers with its efficient performance. DSP is the core of data acquisition of the whole system. The data processing link of the system is mainly completed in DSP. DSP device has many optional IP core resources. The data output of the system is completed by the PCI bus interface of DSP device, and the data is sent to the back-end computer for further processing, storage and recording.

FPGA is the heart and bridge of the whole system. Because the working frequency and data bit width between the data acquisition module and the data processing module cannot be directly matched, and the FPGA device has the characteristics of flexible design and compatibility with a variety of interface levels, the transition and connection between the acquisition module and the processing module are realized through FPGA. In this paper, a data buffer FIFO is designed in FPGA device to realize the cache of system data and the transformation of data bit width and transmission frequency [2]. PLL in FPGA device is used to double the frequency of clock signal to provide clock signal for the system.

2.1 DSP Module Design

The system uses TigerSHARC Series High-Performance floating-point DSP: TS201 to complete baseband signal processing, so as to ensure high data transmission rate, large data exchange task and real-time transmission. TigerSHARC processor is the core of a software defined radio solution for baseband modem, and supports high-level language and operating system.

Following ADSP-TS101, ADI released new members of TigerSHARC in 2003: ADSP-TS201, ADSP-TS202 and ADSP-TS203. The operating frequency of its core has reached 600 MHz, and the on-chip memory has been increased to 24 Mbit. ADSP-TS201 is a static superscalar processor with high performance, which is specially optimized for large signal processing tasks and communication structure.

The main performances of ADSP-TS201 are as follows:

First, up to 600 MHz operation speed, 1.6 ns command cycle;

Second, 24 Mbit on-chip DRAM is divided into six 4 M bit blocks M0, M2, M4, M6, M8 and M10;

Third, dual operation module, each calculation block includes 1 ALU, 1 multiplier, 1 shifter [3], 1 register group and 1 communication logic operation unit;

Fourth, double integer ALU provides data addressing and pointer operation functions;

Fifth, integrated I/O interface, including 14 channel DMA controller, external port, 4 chain junctions, SDRAM controller, programmable flag pin, 2 timers and timer output pins, etc. for system connection;

Sixth, IEEE1149 1. Compatible JTAG port is used for online simulation;

Seventh, four groups of fully bidirectional chain intersections, each containing 4-bit independent input and 4-bit independent output [4], and using LVDS technology, the link throughput reaches 4G bytes;

Eighth, up to 8 TIGERSHARCDSPS can be seamlessly connected through the shared bus;

Ninth, there are four boot modes: EPROM boot, host boot, link boot, and no boot.

The main advantages of ADSP-TS201 are:

(1) Provide high-performance static superscalar DSP operation, specially optimized for communication and applications requiring multiple DSP processors;
(2) Excellent DSP algorithm and I/O performance;
(3) The DMA controller supports 14 DMA channels and can complete the high-speed transmission of overhead between on-chip memory, off-chip memory, memory mapping peripherals, chain junctions, host processors and other multiprocessors;
(4) Very flexible instruction set and DSP structure supporting high-level language are convenient for DSP programming;
(5) A scalable multiprocessor system requires only low communication overhead.

On this basis, the external memory interface is designed. Although ADSP-TS201 has 24 Mbit on-chip DRAM, it is not enough to use only on-chip memory because DSP undertakes heavy signal processing and data exchange tasks in the whole system. Therefore, in this hardware system, the external 128 Mbit SDRAM is used to expand

the storage space of DSP. In addition, a Flash is configured on the periphery of the DSP to guide the DSP loader after power on.

The mode of SDRAM access needs to be set through the register sdrcon. Meanwhile, in order to meet the timing requirements of SDRAM, ADSP-TS20xs allows the addressing of SDRAM to adopt pipeline mode, pipeline depth (definition of pipelining depth: delay between address valid period and data valid period) is set in register sdrcon. In addition, SDRAM configuration requirements of different manufacturers can be met by properly configuring sdrcon register of ADSP-TS201 processor. Before selecting appropriate storage devices, first understand the characteristics of SDRAM controller of DSP and SDRAM controller characteristics As shown in Table 1:

Table 1. SDRAM controller characteristics of TS201

Serial number	Controller parameters	Corresponding valid values
1	Operating voltage	3.3 V and 2.5 V
2	Maximum supported operating frequency	125 MHz
3	Maximum supported storage capacity	256 Mbytes
4	Number of SDRAM banks	2 or 4
5	CAS delay	Programmable: 1–3 SCLKS
6	Refresh rate	Programmable: 32–64 ms
7	BurstLength	Fullpageburst
8	Page size	Programmable: 256, 512 or 1024 words
9	Initialization sequence	MRS-> REF REF-> MRS

The above modules are used as the main controller of the system to improve the response speed of the system.

2.2 FPGA Module Design

FPGA module acts as the heart, commander and Bridge in the whole system. The clock signal and control signal of the whole system are provided by FPGA. In order to solve the mismatch between the working frequency and data bit width between A/D module and DSP module, the system realizes the connection and data transmission between them through FPGA [5].

FPGA, namely field programmable gate array, is a high-performance programmable logic device developed on the basis of complex programmable logic devices. FPGA devices are generally based on SRAM process, and some devices are based on Flash process or anti fuse process. FPGA devices have a very high degree of integration, with

device density ranging from tens of thousands of system gates to tens of millions of system gates. They are grouped into programmable I/O units, embedded block RAM, underlying embedded units, rich wiring resources, basic programmable logic units, special hard cores for cores, etc.

Compared with ASIC chip, FPGA chip has the advantages of short development cycle, low design cost, standard product test free, advanced development tools and real-time online detection. Therefore, FPGA devices are widely used in the original design of products. Traditional data acquisition systems are generally designed based on DSP structure. This system generally designs DSP peripheral interface circuit through small-scale digital devices. Such interface circuit occupies a large space and does not have scalability. FPGA device has the characteristics of programmability, good expansibility and high integration, which is very suitable for the application of DSP peripheral interface circuit. The system uses FPGA devices to realize the interface connection between DSP and A/D module, and undertakes the tasks of data preprocessing, caching and timing control in the system [6].

The CycloneII series chip Ep2C5 of Altera company is selected, which has 4608 logic units, 26 M4K random access memory modules, 13 embedded multipliers, 2 phase-locked loops and 158 user I/O interfaces. This series of chips are manufactured by low-K electrolyte process based on 90 nm. Therefore, the chip has good fast response and low power consumption performance. It is the lowest cost FPGA chip in the industry. CycloneII series chips have the following characteristics:

(1) High density structure. With 4608-68416 logic units. M4K embedded memory module; 1.1M embedded RAM; working frequency up to 260 MHz.
(2) Embedded multiplier. With 150 18 × 18 bit embedded multiplier (can be used as two separate 9 × 9); Operating frequency of 250 MHz; Optional input and output registers;
(3) Advanced I/O interface technology. Support various types of high-speed differential I/O interfaces, including LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL and differential SSTL; support single ended standard I/O interfaces of 2.5 V and 1.8 V; support PCI bus interface and PCI-E interface with 32-bit or 66 bit operating frequency of 33 MHz or 66 MHz; high-speed external memory interface, etc. [7];
(4) Flexible clock management circuit with 2–4 PLLs, 16 global clock networks;
(5) Multiple chip configuration modes, including active configuration, passive configuration and JTAG configuration;
(6) A variety of embedded IP cores. In order to optimize CycloneII devices, more than 40 IP cores are embedded, including NiosII embedded processor, PCI bus, fir compiler, DDRSDRAM controller, FFT/IFFT, etc.

On this basis, the peripheral circuit of FPGA is designed:

First, the configuration circuit. The CycloneII device is based on the SRAM structure. The configuration information of the chip is stored in the SRAM. Because the data in the SRAM is lost after power failure, the configuration information of the chip will be reloaded after each power on. FPGA chip has three configuration modes: active configuration mode, passive configuration mode and JTAG configuration mode. Active configuration mode: in as mode, the FPGA chip controls the configuration process, and

sends the control signal and synchronization signal to the configuration chip of EPCs series to complete the configuration operation. Passive configuration mode: in PS mode, the configuration process is controlled by an external processor or computer, and the configuration process is completed by enhanced configuration devices.

Second, clock circuit. FPGA chip is the heart of the system and provides clock signal for the system. The system provides 50 MHz clock source for FPGA chip, which is provided by the clock generation circuit in the figure below. After entering the FPGA module, the clock signal is divided and multiplied by the PLL, and then sent to the A/D acquisition conversion module and DSP data processing module respectively.

2.3 Design of Analog-to-Digital Conversion Module

The signal output by the sensor is generally analog signal. In the system with computer as the core, the analog signal output by the sensor must be converted into digital signal before it can be recognized and analyzed by digital electronic equipment. A/D chip is a special analog-to-digital converter and the primary link of data acquisition system. A/D converter is an extremely important key component of data acquisition system. The performance of a/D converter is directly related to the quality of the whole data acquisition system. The so-called A/D conversion is to convert the analog signal output by the sensor into digital signal for the identification and processing of digital circuit [8]. In the A/D converter, the amplitude of the input analog signal is continuous in time, but the output digital signal is discrete. Therefore, the sampling of the input signal can only be completed at some selected moments, and then the sampled value can be converted into digital electricity. The working process of A/D conversion is divided into four steps: sampling, holding, quantization and coding. Firstly, the analog signal is sampled. After sampling, the signal enters the hold state. Within the hold time, the sampled voltage is converted into digital quantity, and then encoded. Finally, the conversion results are output according to the fixed coding format, and then enter the next round of sampling.

In this study, a high-performance A/D converter AD9254 launched by American analog devices company is used. The sampling rate of this A/D converter is millions of samples per second and has a resolution of 14 bits. This A/D converter works at 70 MHz and has a spurious free dynamic range of 83 dB. At the same time, the power consumption is only 50% lower than that of similar products. Because AD9254 has high SFDR, low power consumption and small package size (7 mm × 7 mm 48 pin LFCSP) has many perfect performances. The device is very suitable for the application of high-speed acquisition system. The Sha of AD9254 operates in two modes: sampling mode and hold mode. When SHA is switched to the sampling mode, the signal source must be able to complete the charging process of the sampling capacitor within half a cycle. The analog input of the AD9254 has no internal DC bias. When collecting AC signal, users need to set bias circuit externally. Generally, the bias voltage value should be set to 0.55 times of avdd. The common mode reference voltage of the circuit can be directly provided by the chip pin CML. At this time, the CML pin needs to be grounded through a 0.1 uF capacitor to realize decoupling. Power down mode: AD9254 has a low-power standby mode. When pdwn pin is connected to low level, AD9254 is in normal working mode; When pdwn pin is connected to high level, AD9254 is set to powerdown mode.

In this mode, the power consumed by the A/D converter is only 1.8 mW, and the output is in a high resistance state.

2.4 Interface Circuit Design of A/D Conversion Module

The analog signal input terminal of AD9254 has three configuration modes: transformer input. When the signal-to-noise ratio is very demanding, the transformer is usually used as the input driving circuit. When the frequency of the input signal is in the second Nyquist region or above, the performance of many amplifiers can not meet the signal-to-noise ratio requirements of AD9254. When selecting the transformer, it is necessary to consider the characteristics of the signal. Many RF Transformers will reach saturation at a frequency of several MHz [9]. When the signal energy exceeds this frequency range, it will cause coresaturation and signal distortion. The transformer chip of the system adopts ADT1-1WT+RF transformer of Mini-Circuits company. The power consumption of the transformer is 0.5 W, the DC current is 30 mA, the signal bandwidth is 0.4-800 MHz and the voltage ratio is 1:1. It has excellent performance in phase imbalance and amplitude imbalance transmission, and is very suitable for impedance matching and stable amplifier. The analog signal is input through the PRI pin of the transformer and then output in the form of differential signal from the two pins on the secondary side of the transformer. SEC_CT pin is used to provide A/D common mode voltage. A filter link is introduced between the pins of the secondary side of the transformer to obtain a stable output signal.

AD8138 differential drive. When the input signal frequency is in the second Nyquist region, in addition to using the transformer as the driving circuit, a special driving chip can also be selected as the differential driving circuit. The system selects AD8138 chip of ADI company, which is a special low distortion differential A/D converter driving chip. It can convert single ended signal into differential signal, realize balanced signal transmission, and help the A/D converter achieve the most perfect performance. The collected analog signal is input by NI+pin of AD8138, and the differential signal is output by +OUT and −OUT pins after passing through AD8138 chip, The common mode signal is provided by the Vocm pin. The output pin also introduces a filtering link to filter out clutter and obtain a stable output signal.

Differential double unbalanced transformer coupling drive. In those environments with very strict requirements for SFDR, using differential double unbalanced transformer coupling as input drive circuit is a good choice. In the data acquisition system studied in this paper, because the system does not have very strict requirements for SFDR, the first two driving modes are selected at the analog input of AD9254 chip, namely transformer driving mode and AD8138 driving mode.

For the clock input circuit, the high-speed A/D converter has very strict requirements for the quality of the sampling clock signal. Any noise or jitter in the clock signal will cause the output signal distortion of the A/D converter. Therefore, the clock circuit design is an important link in the high-speed circuit design, which needs the designer to pay enough attention.

The clock input structure of AD9254 is very flexible, including CMOS, LVDS, LVPECL and sinusoidal signal. However, no matter which clock signal is selected, jitter is still the most important indicator of clock source. A/D chip needs a low jitter clock

signal source to provide clock signal. Without a low jitter clock source, a low voltage differential signal can be AC coupled to provide a clock signal for the AD9254. A/D951x clock driver series chips have the performance of providing low jitter clock. The system selects ad9515 chip with more functions and better performance. The clock signal is provided by the FPGA module. After filtering by AD9515, it provides a stable clock signal for AD9254.

2.5 Communication Interface Design

Considering that the final data source and data terminal of the whole system are PC, it is necessary to design the communication interface between the hardware platform and PC. In addition, in order to complete the data exchange between DSP and FPGA, it is also necessary to establish the corresponding communication interface between them. In the system, the network controller selects the 10/100M adaptive fast Ethernet control processor based on asynchronous ISA bus of DAVICOM company model DM9000E, and synthesizes MAC, PHY and MMU. DM9000E is a fully integrated, low-cost, single fast Ethernet control chip with 16 K high-capacity FIFO, 4-channel multi-functional GPIO, full duplex operation and other functions. The physical layer supports Ethernet interface protocol. Because data is sometimes received in burst form, DM9000E also integrates a receiving buffer, so that when data is received, it can put the data into the buffer, and then the data link layer can directly take the data from the buffer. The link layer usually includes the device driver in the operating system and the corresponding network interface card in the computer. They process the physical interface detail data with the cable together, and its buffer can be used to temporarily store the frames to be sent or received.

The serial port chip used in this system is ST16C550, which is one of the most stable and reliable UART chips launched by EXAR company, and can provide serial/parallel and parallel/serial conversion functions of data. The synchronization function of serial data stream is realized by adding start and end bits to the transmission data to form data bytes.

Ensure data integrity by attaching parity bits to data bytes. The receiver checks the parity bit to determine whether there is a transmission error. It will be very complex to realize these functions with ordinary circuits, especially when the circuit is integrated on a single chip. ST16C550 adopts 0.6 mm CMOS process to meet the requirements of low power consumption, high speed and high integration. ST16C550 is equipped with 16 byte transceiver FIFO memory to communicate with high-speed memory. Under the external clock of 24 MHz, the transmission rate of ST16C550 can reach 1.5 Mbps. Other features of ST16C550 can be obtained through internal registers. Optional receive FIFO trigger points, optional TX and RX baud rates are some features of ST16C550.

3 Software Design of Education Management Information System from the Perspective of Big Data

In the system software part, big data technology is mainly used for education information management, and the specific contents are as follows.

3.1 Data Set Division

Parallel association rule mining algorithm is to divide the data set into each data block, and then scan each data block for association rule mining. In parallel association rule mining algorithm, different partition methods will greatly affect the mining efficiency of the algorithm. The most effective data set partition method must make a frequent item set in the data set be a frequent item set in only one or few data blocks. Therefore, data clustering technology can be used to cluster the transactions in the whole data set, and each cluster can divide the whole data set into each data block. Common clustering methods generally need to scan the whole data set for many times. When the data set contains a large number of transactions and the computational cost of clustering is too high, the parallel association rule mining algorithm will no longer have advantages. Therefore, it is very important to find a better and faster data set partition method. There is often a classification hierarchy relationship between various items in the data set. When the average transaction length of the data set is quite different from the number of items, the classification hierarchy relationship is used to cluster the transactions in the data set. The calculation is as follows:

$$\frac{|T - I_i|}{|T|} \leq \alpha \tag{1}$$

In formula (1), T represents the task to be divided, I_i represents the data block, and α represents the specified parameters. Based on the above calculation, it can be ensured that a transaction will not be divided into multiple data blocks.

3.2 Data Set Allocation

In this part, for the distribution of education management information, the data distribution process is set in the program design stage. When executing the program, the pre arranged distribution method is used to distribute the data to each node for calculation. In the environment with light network load and machine load, static data distribution can effectively deal with the problem of load balance.

Dynamic data allocation [10], the data allocation process is carried out dynamically during the calculation process. The master node does not allocate all data at one time. When a slave node completes the calculation and transmits the results to the master node, the master node redistributes the remaining data until all data are processed [11]. For cloud computing environment, static data distribution is prone to load imbalance, but it is easy to design coarse-grained parallel programs to reduce the traffic in the computing process; Dynamic data allocation is easier to achieve load balancing and facilitate the use of high-performance machines in the cloud environment for computing, but the corresponding parallel programs are difficult to design and usually require some additional overhead. For example, in order to understand the computing speed of each node, increase the traffic to determine the next data allocation. Based on the above analysis, this study uses the following methods to allocate data sets:

$$\alpha_j = \frac{W_j}{W} \tag{2}$$

In formula (2), α_j represents the proportion of data set allocation on node j, and W_j represents the weight of the overall processing capacity of the node executing the Map task in the cluster system. Based on the above calculation, the resource allocation is realized to realize the allocation of the education management information system.

4 Experimental Comparison

In order to verify the application effect of the system, taking a school as an example, this paper analyzes the application effect of the previous system and the proposed system. The hardware tool used is an ordinary PC, which is basically configured as Intel(R) Core(TM)2 Duo CPU P8600 2.4 GHz and 32 G memory. The Quist synthetic data generator of IBM is used to generate the experimental data of association rule mining objects. The main experimental results are as follows.

The comparison results between the correct mining quantity of the previous system and the correct mining quantity after the application of the system of this study are shown in Table 2:

Table 2. Number of correct information mining

Experiment serial number/piece	Item quantity/piece	Correct excavation quantity of the designed system/piece	Correct excavation quantity of previous system/piece
1	100	100	98
2	100	100	95
3	120	119	110
4	130	129	120
5	120	120	110
6	150	148	135
7	150	150	140
8	160	160	150
9	170	168	160
10	180	178	170

Based on Table 2, it can be found that the system studied can mine relevant information more accurately. However, in the previous system, there are less correct mining data and low accuracy.

The comparison results of teaching resource mining time between the information management system of this study and the previous management information system are shown in Fig. 2:

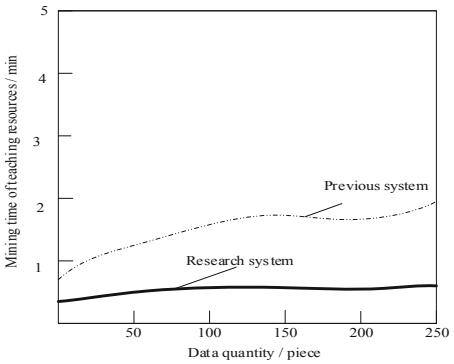

Fig. 2. Comparison of teaching resource mining expenses under different data volumes

The comparison results of student information mining expenses of the two systems under different data volumes are shown in Fig. 3:

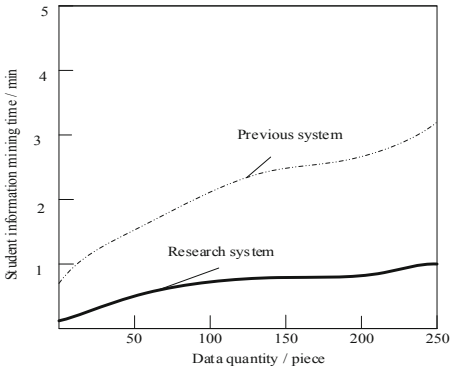

Fig. 3. Comparison of student information mining expenses under different data volumes

The comparison results of teacher information mining overhead time of the two systems under different data volumes are shown in Fig. 4:

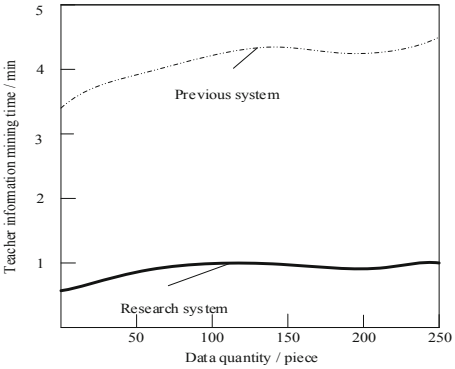

Fig. 4. Comparison of teacher information mining expenses under different data volumes

Based on Fig. 4, the proposed intelligent education management information system is less affected by the amount of data and can ensure a faster information mining speed. In the past, the system used in the school spent more time on teaching resource mining, which was greatly affected by the amount of data.

To sum up, the designed intelligent education management information system of colleges and universities from the perspective of big data can mine relevant information more accurately and is less affected by the amount of data, which can ensure faster information mining speed and better performance.

5 Conclusion

Based on the above process, the research of University intelligent education management information system from the perspective of big data is completed, and the effectiveness of the system is verified by experiments. The innovation point of the system is to design DSP module, FPGA module, ANALOG-to-digital conversion module, A/D conversion module interface circuit and communication interface in the hardware part. In the software part of the system, the big data technology is used to divide and allocate data sets to achieve the design of intelligent education management information system in colleges and universities. The proposed university intelligent education management information system can effectively improve the accuracy and efficiency of resource mining, and has a good effect. However, the research time is limited, and the proposed system still has shortcomings. In the follow-up research, the system will be further optimized.

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