Energy-Efficient DAC Scheme Based on Unit Capacitor Switching for SAR ADCs

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Abstract. With the development of Internet of Things (IoTs), the number of sensor nodes is growing rapidly. These sensors are usually passive or supplied by batteries and are usually a mixed-signal circuit. Analog to digital converter (ADC) is a core element in the sensor, and the power consumption of occupies a considerable part of the whole sensor. SAR ADC is a good candidate for the sensor due to its good energy-efficiency, medium resolution and speed. As the key part of SAR ADC, digital-to-analog converter (DAC) dominates the power consumption of the SAR ADC when dynamic comparator is employed. In order to improve the energy efficiency of the DAC, this paper proposes energy-efficient DAC scheme based on unit capacitor switching. By employing a capacitor-splitting structure and introducing a third voltage reference V_q equal to a quarter of the voltage reference V_{ref}, the unit capacitor can be employed to generate the last bit, which in turn reduces the DAC area. Simulation results show that the proposed scheme reduces the switching energy by 99.03% and the DAC area by 87.5% compared to the conventional SAR ADC structure, which achieves good energy-efficiency and area-efficiency.

Keywords: SAR ADC · DAC switching scheme · Energy-efficiency · Unit capacitor switching · Area-efficiency

1 Introduction

With the development of Internet of Things (IoTs), sensors are wildly deployed in order to meet requirements of information acquisition. In order to extend the life of sensors, the power consumption is very stringent, especially for implantable, portable and wearable devices. As the key component of these sensors, analog-to-digital converter (ADC) consumes a large amount power of the sensors. Compared to flash ADC, sigma-delta ADC and pipeline ADC, successive approximation register (SAR) features low power, medium speed, low complexity and medium resolution, and is a good candidate for those low power applications.

In SAR ADC, capacitive DAC (CDAC) dominates the power consumption and the area of the SAR ADC, and the power consumption and the area of DAC increase with the resolution of ADC. In recent years, various DAC scheme have been developed to improve

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the performance of the DAC [1–9]. In [1], by using a set and down method, the switching energy is reduced by 81.26% compared to the conventional structure. In [2], the V_{cm}-based scheme reduces the switching energy by 87.54% compared with the conventional scheme. Although schemes in [1, 2] greatly improve the energy-efficiency, the DAC area is still too large, which occupies a large die area. In order to improve the energy efficiency and reduce the DAC area, schemes in [3–8] proposes different methods to improve the performances. Compared with the conventional schemes, the low frequency dependence switching scheme in [3], the tri-level scheme in [4], the Vcm-based monotonic switching scheme in [5], the switching scheme in [6], the scheme with high accuracy in [7], the scheme in [8] and the low common-mode voltage variation scheme in [9] reduce the switching energy by 95.34%, 96.89%, 97.66%, 98.84%, 98.44%, 98.84% and 98.45%, respectively. And these schemes in [3–8] all achieve an area reduction of 75% compared to the conventional scheme. In order to further reduce the DAC area, a V_{aq}-based tri-level switching scheme is developed [10], and the DAC area is only 12.5% of the conventional scheme, which reduces the DAC area by half compared with schemes in [3–9]. However, the switching energy is only comparable to the tri-level scheme in [4]. In order to further improve the energy efficiency and reduce the DAC area, this paper proposes a DAC scheme based on unit capacitor switching, which improves the energy efficiency by 99.03% and reduces the DAC area by 87.5% compared to the conventional scheme.

2 Proposed DAC Switching Scheme

The proposed architecture for a 10-bit SAR ADC is shown in Fig. 1. The SAR ADC is mainly divided into three parts: SAR logic, DAC and comparator. Here, a capacitor-splitting DAC structure is adopted as in [7], and the most significant bit (MSB) capacitor is divided into small LSB parts, which is the same as the least significant bit (LSB) capacitors. The DAC consists of four sub-arrays, i.e. two MSB sub-arrays and two LSB sub-arrays. Different from other schemes in [2–9], the proposed architecture introduces a new reference voltage V_q, which is a quarter of the reference voltage V_{ref}.

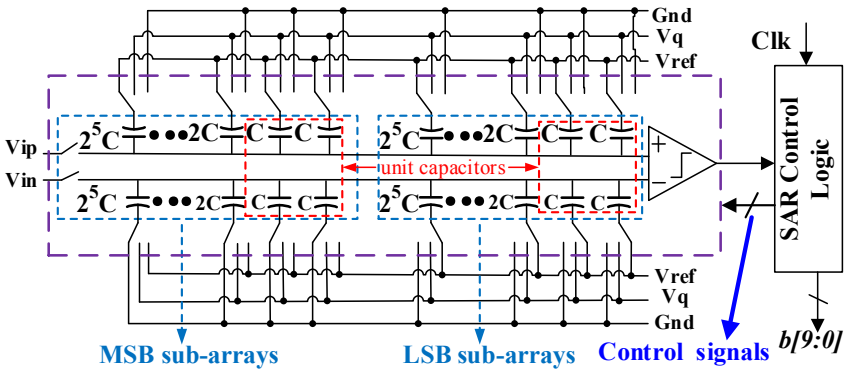

Fig. 1. Proposed SAR ADC structure

2.1 Switching Procedure of the Proposed Scheme

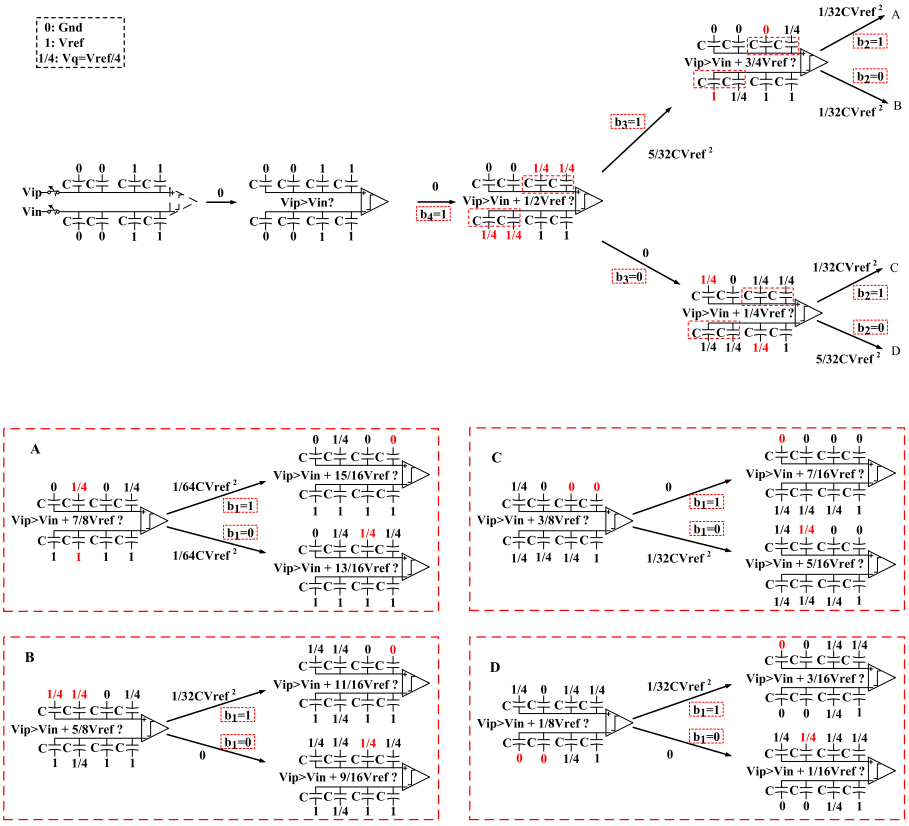

Fig. 2. The DAC switching procedure for a 5-bit SAR ADC model

The complete DAC switching procedure is explained using a 5-bit ADC in Fig. 2. As the conversion is symmetric, only the case for $V_{ip} > V_{in}$ is shown here. The sampling is conducted by connecting the inputs to the top plates of the DAC while the sequences of the bottom plates on both sides are set to [0, 0, 1, 1]. The MSB (b_4) is obtained with no energy consumption due to the top-sampling technique. When the MSB is acquired, the sequence of higher voltage potential side is set to [0, 0, 1/4, 1/4] and the sequence on the other side changes to [1/4, 1/4, 1, 1]. No energy is consumed for this operation and the MSB-1 (b_3) can be obtained after the comparison. During the MSB-2 (b_2) cycle, if MSB-1 (b_3) equals to logic '1', the corresponding capacitor of the LSB array with higher voltage potential changes from '1/4' to '0' and the counterpart of the LSB array with lower voltage potential changes from '1/4' to '1'; otherwise, the corresponding capacitor of the LSB array with higher voltage potential changes from '1' to '1/4' and the counterpart of the LSB array with lower voltage potential changes from '0' to '1/4'. This operation can be applied to the generations of MSB-2 to LSB-2 for an N-bit ADC.

The last two bits (LSB-1 and LSB) are obtained by reusing unit capacitors. The capacitors connection change depends on the comparison results of MSB, LSB-3 and LSB-2, which is shown clearly in Table 1. In order to clearly explain the LSB-1 and LSB generation, unit capacitors are divided into unit capacitors and dummy capacitors as Fig. 3 shows. And C_{d_DACPM}, C_{u_DACPM}, C_{d_DACPL}, C_{u_DACPL}, C_{d_DACNM}, C_{u_DACNM}, C_{d_DACNL} and C_{u_DACNL} in Table 1 represent the dummy capacitor in MSB sub-array of P-side, the unit capacitor in MSB sub-array of P-side, the dummy capacitor in LSB sub-array of P-side, the unit capacitor in LSB sub-array of P-side, the dummy capacitor in MSB sub-array of N-side, the unit capacitor in MSB sub-array of N-side, the dummy capacitor in LSB sub-array of N-side and the unit capacitor in LSB sub-array of N-side, respectively.

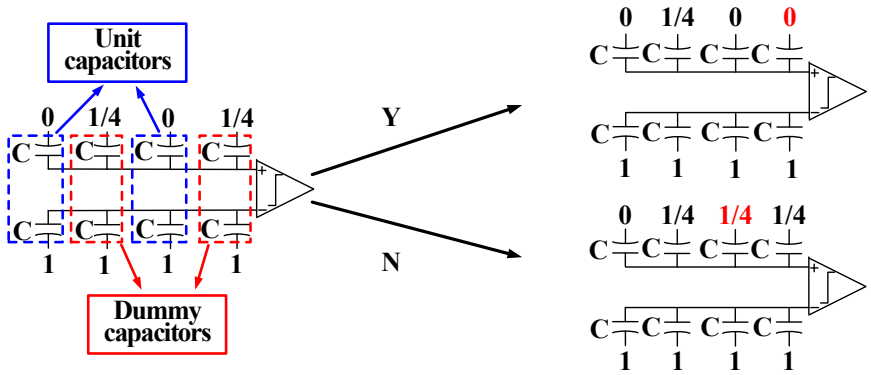

Fig. 3. Illustration of the unit capacitor switching scheme

Case 1: If MSB = 1, LSB-3 = 1 and LSB-2 = 1, for LSB-1 cycle, the dummy capacitor of the MSB-array with the higher voltage potential changes from '0' to '1/4', and the dummy capacitor of the MSB-array with the lower voltage potential changes from '1/4' to '1', this operation achieves an absolute voltage change $1/8V_{ref}$. After the comparison, the LSB-1 is obtained. If LSB-1 = 1, the dummy capacitor of the LSB-array with the higher voltage potential changes from '1/4' to '0'; otherwise, the unit capacitor of the LSB-array with the higher voltage potential changes from '0' to '1/4'. After the DAC settles, the LSB can be obtained after the comparator finished the comparison.

Case 2: If MSB = 1, LSB-3 = 1 and LSB-2 = 0, for LSB-1 cycle, the dummy capacitor and the unit capacitor of the MSB-array with the lower voltage potential both change from '0' to '1/4', and an absolute voltage change $1/8V_{ref}$ can be obtained. The capacitor connection change to obtain the LSB is just the same as Case 1.

Case 3: If MSB = 1, LSB-3 = 0 and LSB-2 = 1, for LSB-1 cycle, the dummy capacitor and the unit capacitor of the MSB-array with the higher voltage potential both change from '1/4' to '0'. For the LSB cycle, if LSB-1 = 1, the unit capacitor of the MSB-array with the higher voltage potential is reconnected from '1/4' to '0'; otherwise, the dummy

capacitor of the MSB-array with the lower voltage potential is reconnected from '0' to '1/4'.

Case 4: If MSB = 1, LSB-3 = 0 and LSB-2 = 0, for LSB-1 cycle, the dummy capacitor and the unit capacitor of the MSB-array with the higher voltage potential both change from '1/4' to '0'. For the LSB cycle, if LSB-1 = 1, the unit capacitor of the MSB-array with the higher voltage potential is reconnected from '1/4' to '0'; otherwise, the dummy capacitor of the MSB-array with the lower voltage potential is reconnected from '0' to '1/4'.

Table 1. Capacitor operations of the last two bits

	MSB = 1 LSB-3 = 1 LSB-2 = 1	MSB = 1 LSB-3 = 1 LSB-2 = 0	MSB = 1 LSB-3 = 0 LSB-2 = 1	MSB = 1 LSB-3 = 0 LSB-2 = 0
LSB-1 cycle	C_{d_DACPM}: 0 to 1/4 C_{d_DACNM}: 1/4 to 1	C_{u_DACPM}: 0 to 1/4 C_{d_DACPM}: 0 to 1/4	C_{u_DACPL}: 1/4 to 0 C_{d_DAPL}: 1/4 to 0	C_{u_DACPM}: 1/4 to 0 C_{d_DACPM}: 1/4 to 0
LSB cycle	LSB-1 = 1, C_{d_DACPL}: 1/4 to 0; LSB-1 = 0, C_{u_DACPL}: 0 to 1/4	LSB-1 = 1, C_{d_DACPL}: 1/4 to 0; LSB-1 = 0, C_{u_DACPL}: 0 to 1/4	LSB-1 = 1, C_{d_DACPM}: 1/4 to 0; LSB-1 = 0, C_{u_DACPM}: 0 to 1/4	LSB-1 = 1, C_{d_DACPM}: 1/4 to 0; LSB-1 = 0, C_{u_DACPM}: 0 to 1/4

2.2 The Impact of the Accuracy of V_q

As Sect. 2.1 described, the MSB is acquired after the sampling and no capacitor connection change is performed. Thus, the generation of the MSB has no relationship with the third reference voltage V_q. During the phase of the MSB-1, all capacitors of the LSB sub-array with higher voltage potential changes from '1' to '1/4' and those of the MSB sub-array with lower voltage potential changes from '0' to '1/4'. Supposing the variation of V_q is ΔV and MSB is '1', then during the phase of the MSB-1, the following equations can be obtained

$$V_{DACP}(MSB1) = V_{ip} - \frac{1}{2}[V_{ref} - (V_q + \Delta V)] \tag{1}$$

$$V_{DACN}(MSB1) = V_{in} - \frac{1}{2}(V_q + \Delta V) \tag{2}$$

$$V_{DAC}(MSB1) = V_{ip} - V_{ip} - \frac{1}{2}V_{ref} \tag{3}$$

where V_{DACP}(MSB1), V_{DACN}(MSB1) and V_{DAC}(MSB1) are the voltage of positive-side DAC array, the voltage of negative DAC array and the differential voltage of the DAC, respectively. From Eq. (3), it can be seen that the variation of V_q has no impact on the DAC voltage. The generation of MSB-2 to LSB-2 is similar to MSB-1, where the operations are complementary, which means the inaccurate transition of one side is compensated by the other side. Thus, the variation of V_q does not affect the transitions. However, the generation of the last two-bits only involves capacitor(s) of one side, thus the inaccurate transition due to the variation of V_q can not be compensated. Fortunately, the voltage changes of the last two-bit are small, the effect of V_q is minimized.

3 Simulation Results

3.1 Switching Energy

In order to evaluate the switching scheme of the proposed scheme, behavioral models of SAR ADC with the proposed DAC switching scheme and other published schemes are built using Matlab. During simulations, a 10-bit SAR ADC is employed, and the negative value of the switching energy was treated as zero in calculation as in [6]. The reset energy can be eliminated by the technique in [11], and it is not considered in the simulation. Figure 4 illustrates the switching energy versus the digital code of different schemes. Table 2 summarizes the main performances of different DAC switching schemes. The switching energy and the unit capacitor number of the proposed unit capacitor switching based scheme are 13.24 CV_{ref}^2 and 256, which improves the energy efficiency by 99.03% and reduces the DAC area by 87.5% compared to the conventional one. Compared to other schemes, the proposed scheme is the most energy-efficient one and the DAC area is the smallest one.

3.2 Linearity

As analysis in Sect. 3.1, the switching energy is related to the value of the unit capacitor. The unit capacitor should be as small as possible when considering the switching energy. However, due to the process variation, the practical value of a capacitor usually deviates from its nominal value, and the capacitor mismatch limits the smallest value of the unit capacitor adopted in the design procedure. Assume that the unit capacitor follows a Gaussian distribution with a mean value of C_u and a standard deviation of σ_u. Each capacitor in the binary-weighted capacitor array is consisted of the unit capacitor connected in parallel.

In order to evaluate the linearity of the switching scheme, Monte Carlo simulations are carried out using Matlab. During simulations, the unit capacitor is regarded as a Gaussian random variable with standard deviation of 1% ($\sigma_u/C_u = 0.01$). Figure 5 shows simulation results of DNL (Differential-Non-linearity) and INL (Integral-Nonlinearity) of 500 Monte Carlo runs of a 10-bit DAC with the proposed switching scheme. The root-mean-square (RMS) values of DNL and INL are 0.259LSB and 0.242LSB, respectively. As the first comparison cycle is mismatch free, the worst DNL occurs at $1/4V_{FS}$ and $3/4V_{FS}$, where V_{FS} stands for full scale signal.

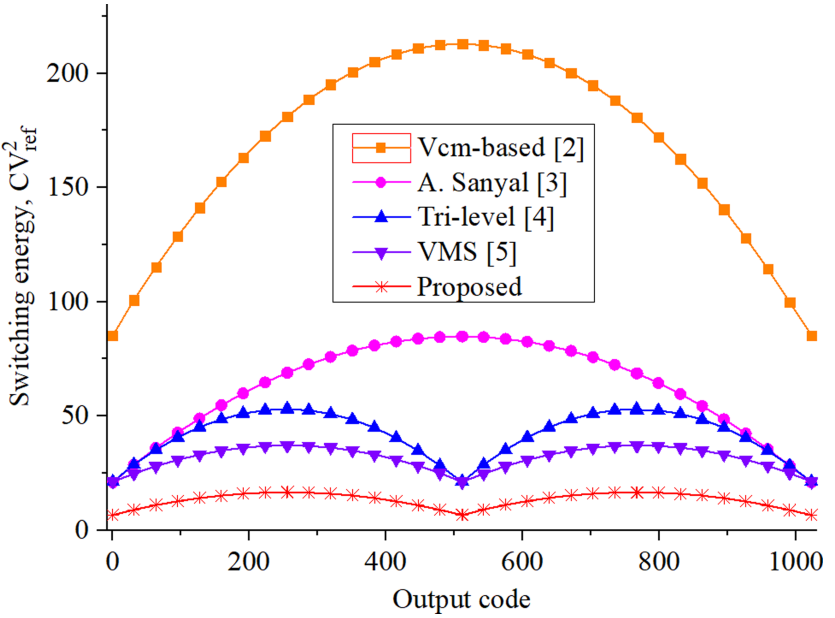

Fig. 4. Output code against switching energy

Table 2. Performance comparisons of different schemes for 10-bit SAR ADC

Switching scheme	Switching energy (CV_{ref}^2)	Energy savings	Total unit capacitor number	Area reduction
Conventional	1363.3	Ref.	2048	Ref.
Monotonic [1]	255.5	81.26%	1024	50%
V_{cm}-based [2]	170.17	87.54%	1024	50%
A. Sanyal [3]	63.56	95.34%	512	75%
Tri-level [4]	42.42	96.89%	512	75%
VMS [5]	31.88	97.66%	512	75%
Tong [6]	15.88	98.84%	512	75%
Xie [7]	21.2	98.44%	512	75%
Zhu [9]	15.88	98.84%	512	75%
Zhao [10]	48.03	96.48%	256	87.5%
This work	13.24	99.03%	256	87.5%

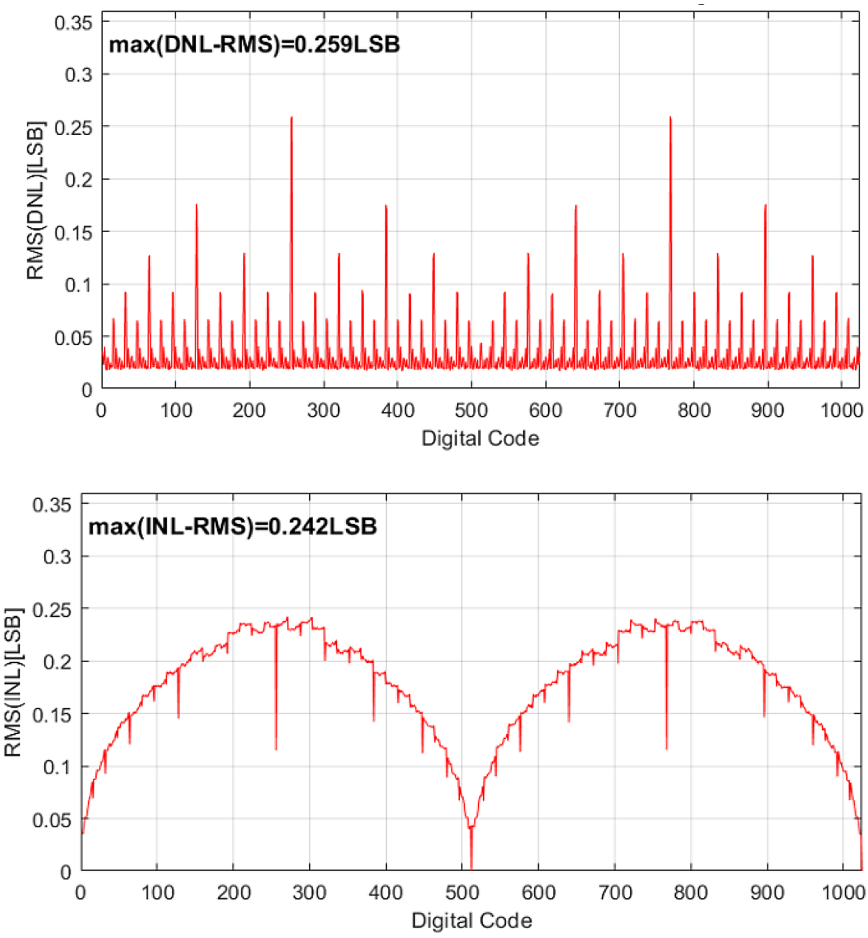

Fig. 5. The standard deviation of DNL and INL of the proposed scheme

4 Conclusion

This paper presents a low energy and small DAC area switching scheme for SAR ADC. By employing a capacitor splitting structure and introducing a third reference voltage V_q equals to 1/4 V_{ref}, the proposed DAC scheme can reuse the unit capacitors to reduce switching energy and the DAC area. Compared to the conventional structure, the proposed structure reduces the switching energy by 99.03% and the DAC area by 87.5%, which achieves both energy efficiency and area reduction.

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References

1. Liu, C.C., Chang, S.J., Huang, G.Y., Lin, Y.Z.: A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. IEEE J. Solid-State Circuits **45**(4), 731–740 (2010)
2. Zhu, Y., et al.: A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. IEEE J. Solid-State Circuits **45**(6), 1111–1121 (2010)
3. Sanyal, A., Sun, N.: An energy-efficient low frequency dependence switching technique for SAR ADCs. IEEE Trans. Circuits Syst. II Express Briefs **61**(5), 294–298 (2014)
4. Yuan, C., Lam, Y.: Low-energy and area-efficient tri-level switching scheme for SAR ADC. Electron. Lett. **48**(9), 482–483 (2012)
5. Zhu, Z., Xiao, Y., Song, X.: Vcm-based monotonic capacitor switching scheme for SAR ADC. Electron. Lett. **49**(5), 327–329 (2013)
6. Tong, X., Zhang, Y.: 98.8% switching energy reduction in SAR ADC for bioelectronics application. Electron. Lett. **51**(14), 1052–1054 (2015)
7. Xie, L., Su, J., Wang, Y., Liu, J., Wen, G.: Switching scheme with 98.4% switching energy reduction and high accuracy for SAR ADCs. Analog Integr. Circuits Signal Process. **90**(3), 681–686 (2016)
8. Zhu, Z., Liang, Y.: A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18μm CMOS for medical implant devices. IEEE Trans. Circuits Syst. I Regul. Papers **62**(9), 2167–2176 (2015)
9. Li, J., Li, X., Huang, L., Wu, J.: An energy-efficient switching scheme with low common-mode voltage variation and no-capacitor-splitting DAC for SAR ADC. Analog Integr. Circuits Signal Process. **104**(1), 93–101 (2020)
10. Zhao, J., Mei, N., Zhang, Z., Meng, L.: Vaq-based tri-level switching scheme for SAR ADC. Electron. Lett. **54**(2), 66–68 (2018)
11. Xie, L., Nie, W., Yang, X., Zhou, M.: A group reset method for energy-efficient SAR ADC switching schemes. Analog Integr. Circuits Signal Process. **96**(1), 183–187 (2018)