Effective Low Leakage 6T and 8T SRAM Using CMOS 90 nm Technology

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Abstract. This study addresses the escalating demand for low-power electronic devices by emphasizing the development of Static Random Access Memory (SRAM) cells with minimized leakage current. The research prioritizes key metrics such as leakage current, read/write stability, access time, and power consumption. To effectively reduce leakage current, reverse-biased FinFETs are employed as efficient switches, creating barriers that impede current flow during idle states. Additionally, power gating techniques selectively disable specific SRAM sub-blocks during inactivity, further reducing static power consumption. This innovative approach, utilizing CMOS 90 nm technology, demonstrates the significance of minimizing leakage current in SRAM cells. The proposed low-leakage 6T and 8T SRAM cells offer a promising solution, contributing to enhanced energy efficiency and performance in memory design. Overall, this research makes notable strides in advancing low-power electronic systems.

Keywords: Leakage currents · CMOS 90 nm · Low Power · Energy Efficiency · Memory design

1 Introduction

Semiconductor and memory design have evolved with Moore's Law, doubling transistor counts every 18 to 24 months. Despite challenges, Static Random-Access Memory (SRAM) remains crucial. Introducing the 8T SRAM cell emphasizes optimal transistor sizing for improved read and write operations, paving the way for energy-efficient solutions amid semiconductor advancements. Cell leakage power involves assessing its contribution to total power dissipation and its significance in determining the overall energy consumption of the memory system. Leakage current entails understanding its direct impact on standby power consumption and energy efficiency in SRAM cells.

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2 The Proposed Algorithm

2.1 Motivation

This research addresses leakage current challenges in CMOS 90 nm SRAM cells by employing innovative techniques like reverse-biased FinFETs and power gating. The aim is to enhance energy efficiency without sacrificing performance, impacting mobile computing, IoT, and energy-conscious electronic systems positively.

2.2 6T SRAM Design

The 6T SRAM cell, composed of six transistors, relies on proper transistor sizing for effective read and write operations. However, switching can briefly cause shortcircuits, resulting in static power loss. SRAM cell design aims to minimize these effects to ensure efficient operations and reduce unnecessary power consumption (Fig. 1).

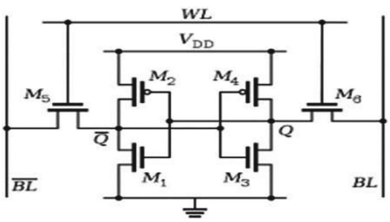

Fig. 1. 6T SRAM design

2.3 8T SRAM Design

The 8T SRAM cell, akin to the 6T version, employs two cross-coupled inverters and two access transistors regulated by a word line. Proper transistor sizing is crucial for efficient read and write operations. SRAM design, including the 8T variant, focuses on minimizing short-circuits during switching to optimize operations and reduce unnecessary power consumption (Fig. 2).

2.4 M-Array Design

Designing a memory array with 90 nm CMOS technology involves selecting cell types, individual cell design, and array organization within semiconductor process constraints. Peripheral circuitry for data access is incorporated, and layout design with simulation ensures performance and adherence to fabrication rules. Post-fabrication testing ensures functionality before integration into larger systems for data storage or other applications, necessitating expertise in semiconductor design to meet specified requirements (Fig. 3).

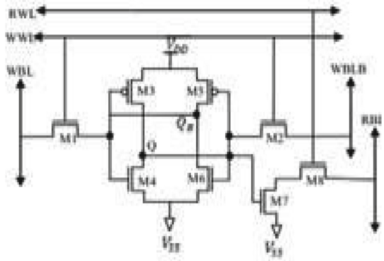

Fig. 2. 8T SRAM design

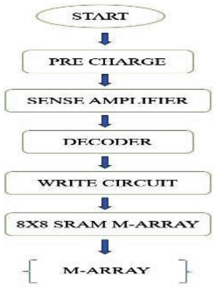

Fig. 3. Execution flow of the M-ARRAY design

3 Design of M-Array Circuit

Creating an 8×8 multiply array with 90 nm CMOS technology involves defining design specifications, considering data rate, precision, power consumption, and area constraints. Choosing an architectural design, like parallel or serial, is crucial for supporting 64 simultaneous multiplication operations. The multiplier cell, designed for speed, accuracy, and power efficiency, is at the core, utilizing CMOS logic gates for effective multiplication in the array.

3.1 Precharge Design

The memory array precharge phase sets voltage levels for bit lines and word lines, ensuring reliable data access. Efficient design minimizes power consumption and improves performance by synchronizing timing and reducing contention and noise during read/write operations (Fig. 4).

3.2 Sense Amplifier

In memory array design, the sense amplifier detects and amplifies weak signals from memory cells for accurate data retrieval during reads, minimizing latency and power consumption. Efficient design enhances overall memory system performance by comparing and amplifying bit line voltages while addressing issues like capacitive loading and loss (Fig. 5).

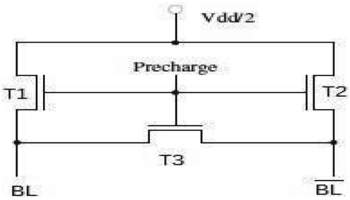

Fig. 4. PRECHARGE Circuit

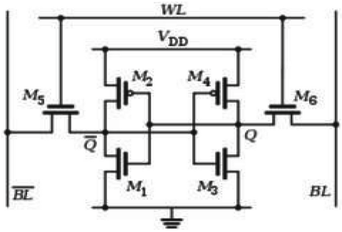

Fig. 5. SENSE AMPLIFIER Circuit

3.3 Decoder

In memory array design, the decoder phase translates controller addresses into control signals for selecting rows or columns for read/write operations. A row decoder activates word lines, facilitating data access, while a column decoder selects bit lines. Precision and speed in decoding ensure accurate memory cell selection, influencing system performance (Table 1).

Table 1. Truth table

$A2$	$A1$	$A0$	$D7$	$D6$	$D5$	$D4$	$D3$	$D2$	$D1$	$D0$
0	0	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	0	1	1	1	1
1	1	0	1	1	0	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1

3.4 Write Circuit

In memory array design, the "write" phase involves applying voltage levels to store data, with the memory controller supplying data bits and address while engaging write drivers and access transistors for signal regulation and connection, emphasizing precision for data integrity and reliability.

3.5 M-Array Circuit Design

Memory array control circuits manage read/write operations in various memory types like SRAM, DRAM, and Flash, encompassing functions such as address decoding, operation control, timing generation, and sense amplifiers with data latches, ensuring precise coordination and reliable performance for efficient data access and storage (Fig. 6).

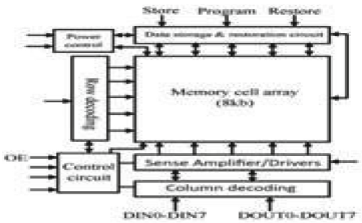

Fig. 6. M ARRAY Circuit

4 Simulation Results

Modern integrated circuits prioritize power efficiency, strategically managing transistor sizes and circuitry to optimize the 8T SRAM cell's performance for contemporary electronic systems with minimal power impact.

4.1 Schematic Diagrams and Simulations

See Figs. 7, 8, 9, 10, 11, 12, and 13.

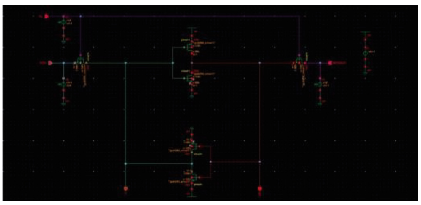

Fig. 7. 6T SRAM Circuit Schematc

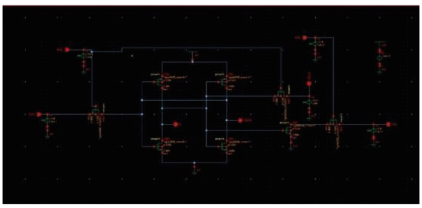

Fig. 8. 8T SRAM Circuit Schematic

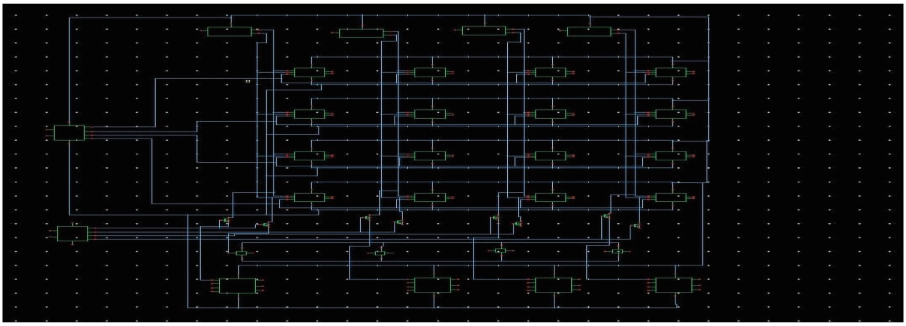

Fig. 9. M ARRAY Schematic

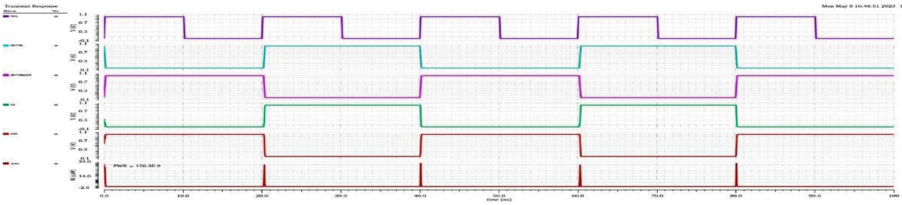

Fig. 10. Waveforms of 6T SRAM

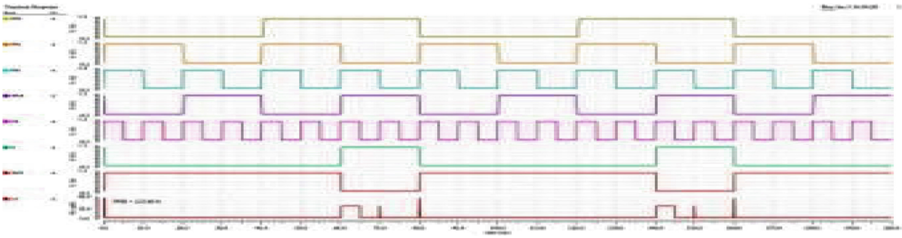

Fig. 11. Waveforms of 8T SRAM

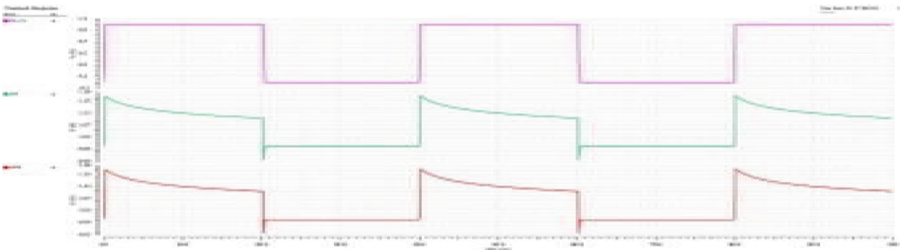

Fig. 12. Waveforms of Precharge

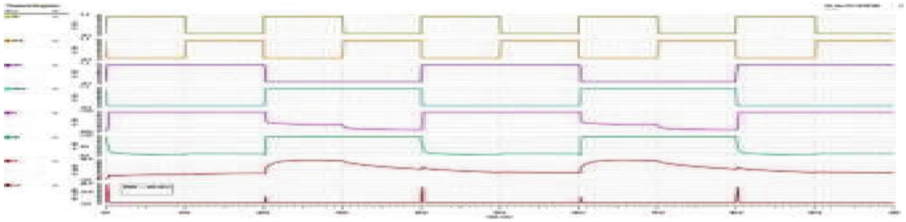

Fig. 13. Waveforms of Sense Amplifier

4.2 Performance Analysis

The passage compares an 8×8 SRAM memory array for moderate needs with a traditional CMOS 6T SRAM cell, highlighting trade-offs in speed, power, and area efficiency based on application-specific requirements (Fig. 14, Tables 2, 3 and 4).

Table 2. Comparative analysis

Aspect	Old Model	Proposed Model
Delay (ns)	10	8
Area (mm^2)	100	50
Power (mW)	10	5

Table 3. Components circuit and outputs

Circuit Component	Output Time (s)
6T SRAM	150.3×10^{-9}
8T SRAM	2.516×10^{-9}
Sense Amplifier	120.1×10^{-9}
Decoder	527.7×10^{-9}

Table 4. Comparison between 8 × 8 SRAM array and traditional

Aspect	8 × 8 SRAM Array	Traditional CMOS
Size	Larger	Smaller
Speed/Access Time	Slower	Faster
Power Consumption	Higher	Lower
Stability/Noise Immunity	Stable	Stable
Integration and Architecture	Complex	Simple
Application	Versatile	Specialized
Design Complexity	Intricate	Basic
Performance-Size Trade-off	Balanced	Efficient

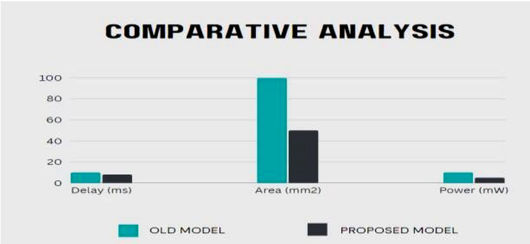

Fig. 14. Comparitive Analysis

5 Conclusion

In conclusion, this research effectively reduces leakage current in 6T and 8T SRAM cells using CMOS 90 nm technology, employing innovative design strategies like reverse-biased FinFETs and power gating. Simulations show superior energy efficiency without compromising performance, demonstrating the potential of CMOS 90 nm for low-power memory solutions and providing valuable insights for future semiconductor processes.

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