# Mitigation of Low-Frequency Oscillations by Tuning Single-Phase Phase-Locked Loop Circuits

Dayane M. Lessa, Michel P. Tcheou, Cleiton M. Freitas(✉), and Luís Fernando C. Monteiro

Rio de Janeiro State University, Rio de Janeiro, RJ 20550-900, Brazil
{cleiton.freitas,mtcheou,lmonteiro}@uerj.br

**Abstract.** Phase-Locked Loop (PLL) circuits have contributed to modernising electrical grids in different segments, such as distributed generation, identification and characterisation of phenomena related to power quality, localisation of faults, among others. This justifies the undergone research aiming at increasing their performance under certain conditions. Taking the example of the single-phase PLLs, researchers have worked out ways to cope with the characteristic doubly-frequency oscillation, which can undermine the performance of the frequency and phase tracking and compromise the extraction of the fundamental component from the input signal. In this sense, the present article aims at analysing a single-phase PLL circuit providing a methodology to adjust the control gains and minimise low-frequency oscillation. As for the analysed PLL, simulations in the time domain were carried out for modified versions of the well-known E-PLL, SOGI-PLL, and APF-PLL, all of them comprising notch filters and to cope with the doubly-frequency oscillation.

**Keywords:** Phase-Locked Loop · Orthogonal signal generators · Tuning methodology · Low-frequency oscillations

## 1 Introduction

Phase-Locked Loop (PLL) circuits are essential for instrumentation and control circuits that are required to be synchronised to the power grid. In fact, the use of PLL contributed to the modernisation of electrical networks in different segments, such as distributed generation, identification and characterisation of phenomena related to power quality, fault-finding on the power grid, among others [1].

When the PLL is applied in low-voltage or weak grids, the tracking of frequency and phase could be compromised by power quality issues, such as presence of unbalanced and harmonic components in the voltages and currents analysed [2,3]. These components may lead the PLL to present oscillating components in the tracked frequency, which could undermine the performance of


J. L. Afonso et al. (Eds.): SESC 2020, LNICST 375, pp. 132–151, 2021.
https://doi.org/10.1007/978-3-030-73585-2_9

PLL-dependent systems, e.g. grid-tied converters. Despite the fact that power quality plays an important role in the PLL performance, there are other issues which could not be neglected. For instance, in single-phase applications the general PLL presents a frequency oscillation at twice the frequency of the grid and it propagates inward, distorting internal signals, and compromising performance of the synchronisation circuit. An alternative to mitigate the problem is the use of an auxiliary signal in quadrature with the fundamental component of the input signal [4,5]. Then for an input signal composed only of the fundamental component, the single-phase PLL in steady-state has a similar behaviour to the three-phase PLL, eliminating the second-order harmonic component when the PLL is in a steady-state condition. Thus, such a harmonic component appears only when transients occur.

Another problem related to PLL is due to the difficulty in tuning the PLL controller gains. The analysis of non-linear models is still quite complex, and the problems related to them are still far from being solved, due to the complexity of the analysis of the mathematical model through second order differential equations [6]. Due to the analysis of transfer functions, the control theory used in most PLLs is strictly based on the linear control theory. In this case, a predefined model in the time domain is linearized for small-signals variations. One example of this approach is found in [6], where a method of analysing and simulating PLLs using linearisation is proposed.

The present work proposes an approach for tuning a single-phase PLL circuit, which is robust not only to variations in small signals, but also to variations in large signals. The methodology was explored in three different single-phase PLLs based on quadrature signal generators (QSG-PLLs) [7]: Enhanced Phase Locked Loop (E-PLL) [8–11], Second-Order Generalized Integrator (SOGI) PLL [12,13], and All-Pass filter PLL (APF-PLL) [14]. All the considered PLL structures were combined with a digital notch filter to mitigate second-order oscillations caused by distorted input signals [9,15].

Concerning the analysis presented in this article, it was considered a threshold of 100 ms, corresponding to 6 cycles of the fundamental component, for the settling time. In other words, any set of control parameters that lead to longer convergence time was disregarded. It was also disregarded the settings in which the output signals presented THD over 2%. It is important to highlight that there must be specific applications where these thresholds are prohibitive, but here it is used for simplicity.

## 2 Dynamic Models of the PLLs

This section presents the three different PLLs considered in the paper and also provides some discussion about their dynamic models. It is important to mention that, differently from the classical structures of the presented PLLs, this research considered the use of an adaptative notch filter to cope with the doubly-frequency components that may appear in the inner signals. The notch filter corresponds to a band-stop filter with a narrow band, that is, a high value for the quality factor.

The quality factor is the ratio between the resonant frequency and bandstop bandwidth. Thereby, the higher is the quality factor, the narrower is the bandstop range, and more accurately a specific frequency component is removed from the signal.

Figure 1 presents the frequency response of a second-order notch filter, whose transfer function is represented by (1), and the resonant frequency of the filter is represented by $\omega_n$ [16]. The quality factor was set as $Q = 1$, $Q = 5$, $Q = 10$ and $Q = 35$ and the component frequency to be attenuated was set 120 Hz. As can be seen, although the stopband is narrower for higher Q values, the attenuation at the resonant frequency increases with the reduction of the quality factor. Due to this factor, it was chosen to work with the quality factor $Q = 1$.

$$H_n = \left( \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \right) \tag{1}$$

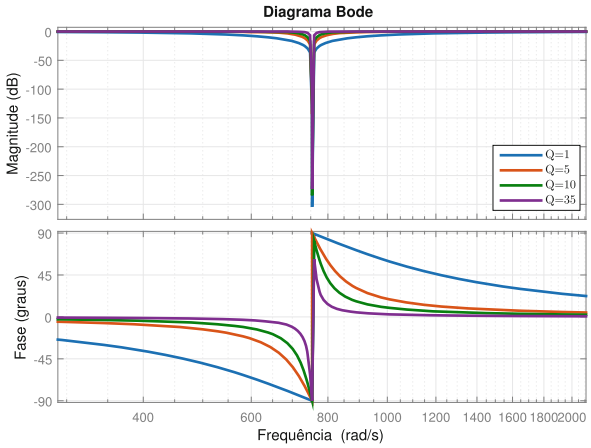



**Fig. 1.** Frequency response of the second-order notch filter

In order to attenuate the second harmonic component, a second order notch filter was designed and used in all PLLs models presented in this work. This filter attenuates second harmonic oscillations in the output signal, reducing the ripple in the PLL internal signals, and also improving the PLL convergence time.

For the mathematical description presented in this section form this point on, it is important to point out that it is neglected the possible effects caused by the notch filters. Such an assumption was considered once they were designed to filter out only the second harmonic component, without reflecting at the DC and fundamental components. Generally, the notch filter is used for attenuating a specific harmonic component present in the input signal and produces less phase lags.

### 2.1 E-PLL Dynamic Model

The Enhanced Phase Locked-Loop (E-PLL), proposed by Karimi [8–11], consists of two control loops. The first one aims to extract the frequency and phase-angle of the input signal, while the second loop obtains the signal amplitude. Figure 2 shows the E-PLL block diagram, including the notch filter in the control loop to track the phase-angle of the input signal.

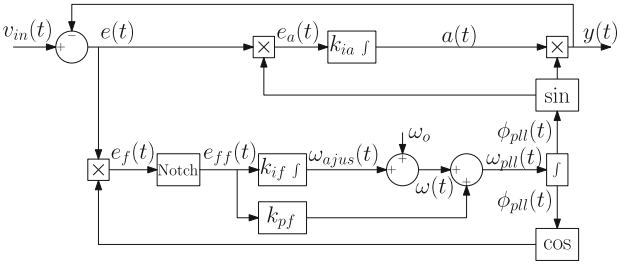



**Fig. 2.** E-PLL Diagram with a notch filter in the phase-loop

The amplitude control loop acts on the amplitude error, represented by $e_a(t)$, using an integral controller with gain $k_{ia}$. On the other hand, the phase-loop acts on the phase error, $e_f(t)$, using a PI controller with proportional and integral gains equal to $k_{pf}$ and $k_{if}$. The parameter $\omega_o$ can be understood as an initial condition, being used to reduce the PLL convergence time. Finally, the E-PLL output signal, $y(t)$, represents the fundamental component (amplitude, phase and frequency) of the input signal $v_{in}(t)$. It is important to highlight that the mentioned gains influence the dynamic of both control loops, since there is no decoupling between them.

One must note that although both control loops run simultaneously, the control loop of the frequency and phase-angle reaches the steady-state condition before the amplitude control loop. This is due to the fact that the frequency and phase-angle control-loop is able to reach the steady-state condition regardless of the amplitude signal. This feature is exploited in sequence.

Assuming that $\omega_1$ is the fundamental frequency of the input signal, and $\phi_{pll}$ is the PLL estimated phase, the input and output-signals, respectively, are given by:

$$v_{in}(t) = V_{in}\sin(\omega_1 t); \tag{2}$$

$$y(t) \;=\; a(t)\sin\Big(\phi_{pll}(t)\Big). \tag{3}$$

The phase-loop error signal, $e_f(t)$, corresponds to the difference between the E-PLL input and output-signals, when this difference is multiplied by the term $cos(\phi_{pll})$. Thus, $e_f(t)$ was decomposed into three components as follows:

$$e_f(t) = \frac{V_{in}}{2}\left[\sin\left(\omega_1 t - \phi_{pll}(t)\right) + \sin\left(\omega_1 t + \phi_{pll}(t)\right)\right] - \frac{a(t)}{2}\sin\left(2\phi_{pll}(t)\right). \quad (4)$$

Assuming that $\omega_1$ and $\phi_{pll}$ are always positive, one may see that $e_f(t)$ presents an average component when $\omega_{pll} = \omega_1$, but $\phi_{pll}(t) \neq \omega_1 t$. Other aspect that must be considered corresponds to the fact that the notch filter attenuates only the second-harmonic component. Thus, even with oscillating components at $e_{ff}(t)$, it is possible to assume that an steady-state condition is achieved when the average components at $e_{ff}(t)$ and $e_f(t)$ decreases to zero, i.e., the input and output-signals are synchronised.

After the convergence process of the phase loop, $\phi_{pll}$ tends to $\omega_1 t$ and the term $\sin(\omega_1 t - \phi_{pll})$ in (4) tends to disappear. Also in this situation, the term $\sin(\omega_1 t + \phi_{pll})$ tends to $\sin(2\omega_1 t)$ and (4) becomes:

$$e_f(t) = \frac{1}{2}\Big[V_{in} - a(t)\Big]\sin(2\omega_1 t). \quad (5)$$

On the other hand, the amplitude control loop is dynamically modified while the average of signal $e_a(t)$ is different from zero. Expanding this control loop, $e_a(t)$ is given by:

$$e_a(t) = \frac{a(t)}{2}\left[1 - \cos\left(2\phi_{pll}(t)\right)\right] - \frac{V_{in}}{2}\left[\cos\left(\omega_1 t - \phi_{pll}(t)\right) - \cos\left(\omega_1 t + \phi_{pll}(t)\right)\right]. \quad (6)$$

An average component appears more evident at $e_a(t)$ when $\phi_{pll}$ is equal to $\omega_1 t$. Indeed, when such condition is reached, $e_a(t)$ is reduced to:

$$e_a(t) = \frac{1}{2}\Big[a(t) - V_{in}\Big]; \quad (7)$$

which means that the amplitude control loop is not at the steady-state condition when $\omega_{pll}$ is equal to $\omega_1$. Such condition is only reached when $a(t)$ becomes equal to $V_{in}$. Furthermore, back to the frequency and phase-angle control-loop, note that an oscillating component still remains at $e_f(t)$ while $a(t)$ is different from $V_{in}$, as shown in (5). Thus, such analysis reinforces the assumption of considering an overall steady-state condition to the E-PLL only after the amplitude control loop reaches such condition.

### 2.2 SOGI-PLL Dynamic Model

The Second Order Generalized Integrator (SOGI) structure integrated into the PLL circuit results in the synchronising circuit known as SOGI-PLL, as shown in Fig. 3. Observe that the SOGI-PLL corresponds to the conventional q-PLL [17], gathered with an auxiliary loop to generate the control signals $v_\alpha(t)$ and $v_\beta(t)$.

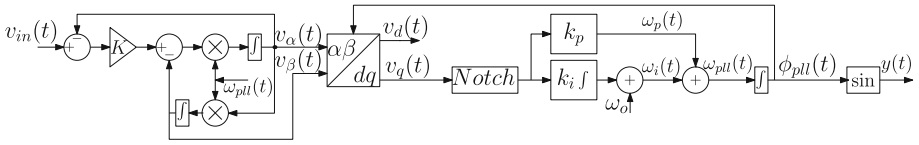



**Fig. 3.** SOGI-PLL Diagram with a notch filter in the phase-loop

The input signal is represented by $v_{in}(t)$ as indicated in (2), and with $v_\alpha(t)$ and $v_\beta(t)$ can be arranged as follows:

$$\frac{dv_\alpha(t)}{dt} + K\omega_{pll}(t)v_\alpha(t) = \omega_{pll}(t)\Big[Kv_{in}(t) - v_\beta(t)\Big]; \tag{8}$$

$$\frac{dv_\beta(t)}{dt} = \omega_{pll}(t)v_\alpha(t). \tag{9}$$

In sequence, the control signal $v_q(t)$ is given by:

$$v_q(t) = v_\alpha(t)\cos\Big(\phi(t)\Big) - v_\beta(t)\sin\Big(\phi(t)\Big). \tag{10}$$

When the average component of $v_q(t)$ becomes equal to zero, the steady-state condition is reached. Thus, such condition occurs with $\omega_{pll}(t)$ synchronised with $\omega_1$ and, moreover, the transient components of $v_\alpha(t)$ must be extinguished. Both dynamics occur simultaneously due to the feedback loop.

Expanding the SOGI loop and assuming that $\omega_{pll}(t)$ is synchronised with $\omega_1 t$, i.e., $\omega_{pll}$ is equal to $\omega_1$, the relationship between $v_\alpha(t)$ and $v_{in}(t)$ is given by:

$$\frac{d^2v_\alpha(t)}{dt^2} + K\frac{dv_\alpha(t)}{dt} + \omega_1^2 v_\alpha(t) = K\omega_1 v_{in}(t). \tag{11}$$

Solving the second-order ordinary-equation, the steady-state solution of $v_\alpha(t)$ is $v_{in}(t) = V_{in}sin(\omega_1 t)$ with $v_\beta(t) = -V_{in}cos(\omega_1 t)$. The dynamics of $v_\alpha(t)$ and $v_\beta(t)$ as a function of the parameter $K$ was described in [18], where $K \geq 2$ leads to an over-damped response. A detailed dynamic analysis to establish some constraints for tuning $K$ was introduced by [13]. In this work, based on the aforementioned proposals combined with some preliminary results, it was considered a gain $K = 3$. Compared to E-PLL, SOGI-PLL has better immunity to distortions in the input signal, $v_{in}(t)$. This occurs due to integrators in SOGI

structure acting as low-pass filters. Thus, the $v_\alpha(t)$ and $v_\beta(t)$ signals have less harmonic distortion compared to that observed in $v_{in}(t)$. On the other hand, such feature may lead to worse dynamics in comparison to the one obtained with E-PLL. Thus a commitment must be established for tuning its internal parameters as proposed in this work.

### 2.3 APF-PLL Dynamic Model

The APF-PLL (All-Pass Filter PLL) presents a similar structure when compared to SOGI-PLL, as illustrated in Fig. 4, where the conventional q-PLL is gathered with the All-Pass filter that generates the auxiliary signal $v_\beta(t)$. One may note that $v_\alpha(t)$ corresponds to the input signal, $v_{in}(t)$, which one was omitted. Essentially, the SOGI loop was replaced by an All-Pass Filter (APF) tuned at $\omega_{pll}(t)$. When the steady-state condition is reached, $\phi_{pll}(t)$ is synchronised with $\omega_1 t$, and $v_\beta(t)$ is in quadrature with $v_\alpha(t)$ as expected. Remind that $\omega_1$ is the frequency of $v_{in}(t)$.

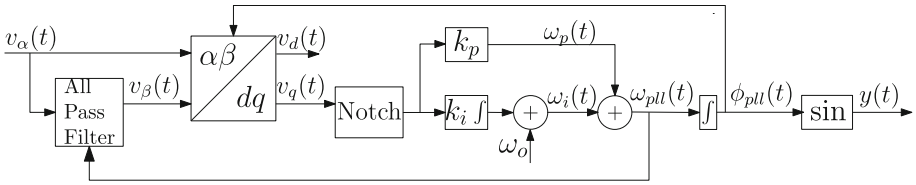



**Fig. 4.** Diagram blocks of APF-PLL including a nocth filter in the phase-loop

Figure 5 shows the All-Pass Filter diagram-blocks, where $\omega_{pll}$ is applied to determine $v_\beta(t)$ as a function of $v_\alpha(t)$, which leads to the following transfer function:

$$G_\beta(s) = \frac{v_\beta(s)}{v_\alpha(s)} = -\frac{s - \omega_{pll}}{s + \omega_{pll}}. \tag{12}$$

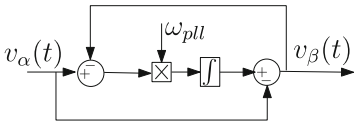



**Fig. 5.** Block diagrams of the All-Pass Filter

Expanding the block diagrams to obtain $v_\beta(s)$ as a function of $v_\alpha(s)$ and converting the expression of $v_\beta(s)$ to time-domain, $v_\beta(t)$ is given by:

$$v_\beta(t) = \frac{V_{in}}{\omega_1^2 + \omega_{pll}^2}\left[2\omega_1\omega_{pll}e^{-\omega_{pll}t} - \left(\omega_1^2 - \omega_{pll}^2\right)\sin(\omega_1 t) - 2\omega_1\omega_{pll}\cos(\omega_1 t)\right]. \quad (13)$$

When the average value of $\omega_{pll}(t)$ becomes equal to $\omega_1$, and neglecting its ripple, the function of $v_\beta(t)$ can be reduced as follows:

$$v_\beta(t) = V_{in}\left[e^{-\omega_1 t} - cos(\omega_1 t)\right]. \quad (14)$$

At steady-state $v_\beta(t)$ becomes equal to $-V_{in}cos(\omega t)$, i.e., $v_\beta(t)$ becomes a sinusoidal waveform lagged 90° by $v_\alpha(t)$ as expected. In sequence, the APF-PLL presents a phase-loop similar as the one introduced in SOGI-PLL, where the control signal $v_q(t)$ is equal to:

$$v_q(t) = \sin\left(\phi_{pll}(t)\right)V_{in}\left[\cos(\omega_1 t) - e^{-\omega_1 t}\right] + V_{in}\sin(\omega_1 t)\cos\left(\phi_{pll}(t)\right). \quad (15)$$

At steady-state, with $\omega_{pll}(t)$ equals to $\omega_1$ and the transient response of $v_\beta(t)$ extinguished, $v_q(t)$ is only comprised by an average component equal to zero. Thus, in comparison to the SOGI-PLL, the APF-PLL presents different dynamics to reach the steady-state condition. Based on the aforementioned conditions to be at steady-state, $\phi_{pll}(t)$ must be synchronised with $\omega_1 t$, as well as the transient response of $v_q(t)$ must be extinguished.

Based on the introduced PLL dynamics models, one may note that tuning the internal parameters of the PLLs through linear model approximations is unfeasible. Therefore, this paper presents an approach for tuning the internal parameters as described in sequence.

## 3 Proposed Approach for Tuning the Internal Parameters of the PLLs

In literature, one may see some proposals for tuning the internal parameters of the PLLs as, for instance, those introduced in [19–23]. Nonetheless, all of them were based on linear model approximations [24,25], which consists of predefined time-domain models valid for small signal variations. Thus, as highlighted in Sect. 2, due to the considerable assumptions and constraints, such models lead to limited-range solutions.

Therefore, it is proposed in this work an approach where the PLLs were submitted to a predefined set of parameters (internal gains). In sequence, data about the convergence speed of the internal loops and harmonic distortion of the output waveform were collected. The flowchart of Fig. 6 summarises the methodology for tuning the PLL control throughout this work [26]. The general idea was to conduct a series of tests considering different setting points (different values

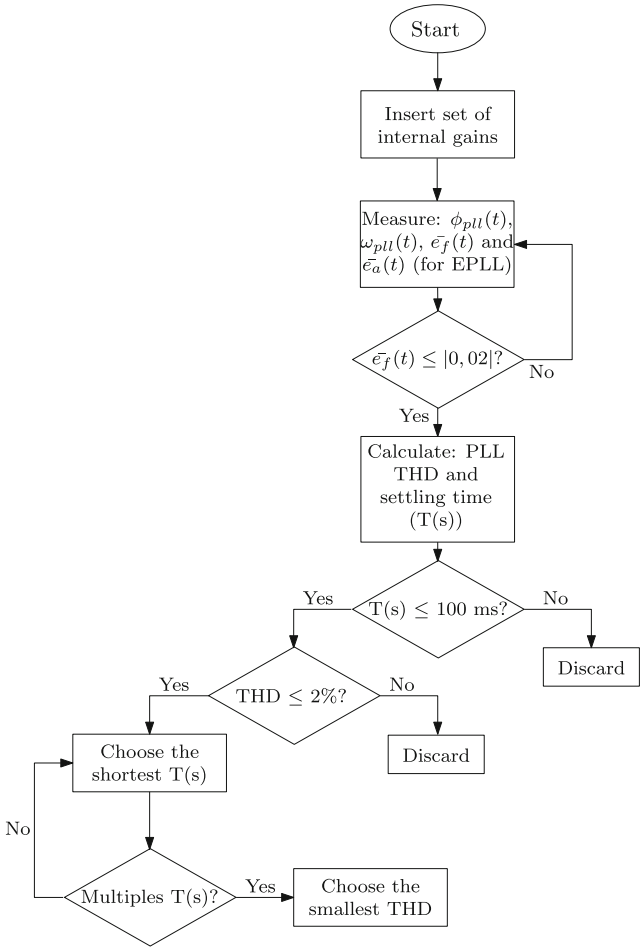



**Fig. 6.** Proposed method for tuning the internal parameters of the PLLs

for the control gains, $k_{pf}$, $k_{if}$ and $k_{ia}$) for the PLLs defined in Figs. 2, 3 and 4. During these tests, the effects caused by the control gains in some performance parameters were analysed and used to indicate the best combinations to comply with some constraints (later explained). As can be seen, two performance parameters were considered during this process: the settling time $T$ and the total harmonic distortion $THD$ of the output signal $y$.

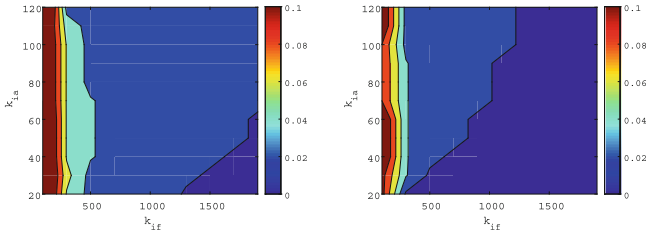
The settling time (convergence speed) was calculated as a function of the average component of the loop-errors. In the cases of the SOGI- and APF-PLLs, only the phase-loop error, $\overline{e_f}(t)$, was considered, whereas, for the E-PLL, it is also considered the average component of the amplitude-loop error, $\overline{e_a}(t)$. To compute the average components of these errors, it is considered a windowed moving average filter with a time span of (1/120) s, which corresponds

to, approximately, 8.33 ms. Such assumption was done once $v_q(t)$ is comprehended by a dc-component plus even-order harmonics ($2\omega$, $4\omega$, $6\omega$, ...), being $\omega$ the fundamental frequency. For determining the time instant where the PLL achieved steady-state condition, it was considered indicated in the flowchart by $|e_f(t)| \leq 0.02$. In other words, the settling time was counted from the beginning of the simulation until the phase error fades under 0.02. This threshold was empirically chosen by analysing the phase signal for different conditions. The THD of the output signal, on the other hand, was computed considering the PLLS in a steady-state condition. A boundary condition was established for reducing the number of results presented in the following sections. In this case, the control settings that led to settling time higher than 100ms and/or THD over 2% were simply discarded. Notice that, this boundary condition was randomly chosen, as this paper does no focus on any specific application. Nonetheless, depending on the application, these limits could be either relaxed or sharpened.

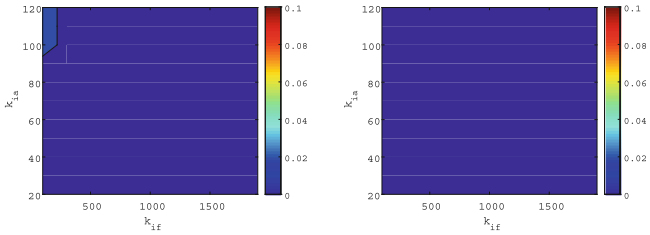
It is important to notice that, in a realistic scenario, where the voltage in a single-phase grid is usually distorted, particularly by the 3rd, 5th, and 7th harmonic components, the internal PLL signals necessarily present oscillating components even in a steady-state condition. These components tend to compromise the phase-tracking performance. For this reason, the tuning of the three PLLs was conducted considering a high-distorted input signal comprising fundamental 3rd, 5th, and 7th harmonic components.

### 3.1 E-PLL Tuning

In sequence, it is applied the proposed approach for tuning the internal gains of the E-PLL. One may note that E-PLL is composed of 2 internal loops (amplitude-loop and phase-loop), and, thus, it was extended the proposed method considering them both. Based on this, it has applied, firstly, to the phase-loop and, in sequence, to the amplitude-loop. The convergence speed of the E-PLL phase-loop is shown in Fig. 7. Basically, the set of gains were arranged with $k_{pf}$ constant and a range of different values for $k_{if}$ and $k_{ia}$, such that $0 < k_{if} < 2000$ and $20 < k_{ia} < 120$. One may note that the settling time is lower than 0.02 s for $k_{pf} = 34$ (Fig. 7(d)). Thus, it considered $k_{pf} = 34$ and it has done once more the proposed method looking to the settling time of the amplitude-loop. The acquired results are illustrated in Fig. 8. As expected, one may note a higher settling time to achieve the steady-state condition. Taking into consideration the $k_{pf}$ previously tuned through the phase-loop analysis, note that the acceptable results (settling time lower than 0.05s) are limited in $0 < k_{if} < 950$ and $118 < k_{ia} < 120$ (see Fig. 8(d)). In sequence, the THD of the output signals were calculated and, based on the obtained results, the E-PLL gains were defined as $k_{pf} = 34$, $k_{if} = 800$, $k_{ia} = 120$. Through them, the settling time of the amplitude-loop was equal to 49.9 ms with an output-signal THD of 1.68%.

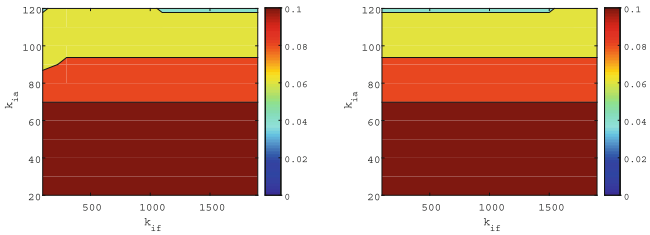



**(a)** Case 1: $k_{pf} = 4$ **(b)** Case 2: $k_{pf} = 14$

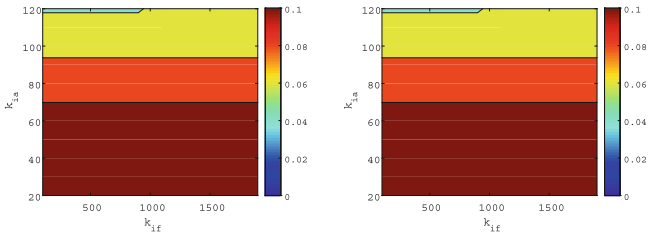



**(c)** Case 3: $k_{pf} = 24$ **(d)** Case 4: $k_{pf} = 34$

**Fig. 7.** Convergence speed of the E-PLL phase-loop




**(a)** Case 1: $k_{pf} = 4$ **(b)** Case 2: $k_{pf} = 14$



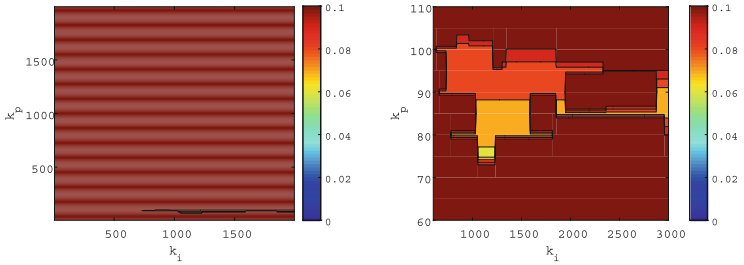

**(c)** Case 3: $k_{pf} = 24$ **(d)** Case 4: $k_{pf} = 34$

**Fig. 8.** Convergence speed of the E-PLL amplitude-loop

### 3.2 SOGI-PLL Tuning

For tuning the SOGI-PLL the procedure was done based on inspection of the PLL phase-loop performance, with the constraint that the output-signal THD must be lower than 2%. The set of the phase-loop gains was composed by a finite range of values. Initially, the integral and proportional gains of the phase-loop were limited to $5 < k_i < 2000$ and $5 < k_p < 2000$, with a step of 20 units. However, as shown in Fig. 9a, the contour region that delimits the shortest settling time in the model proved to be very narrow and a second graph was generated in order to obtain a better view of this band.

The new range of gains was set as $600 < k_i < 3000$ and $60 < k_p < 110$, with a fixed step of 5 units for both gains. Then the circuit was inspected again in order to generate a new and smaller database containing possible combinations of gains in order to verify their influence on the control circuit.



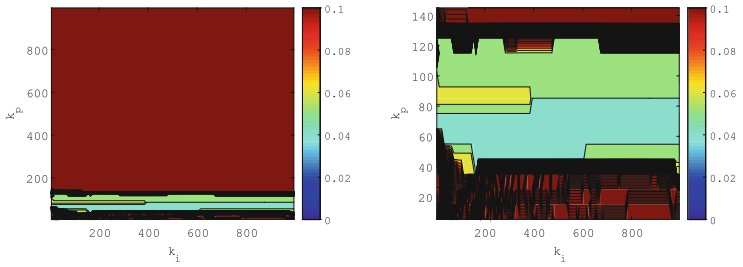

**(a)** Complete range **(b)** Zoomed graph

**Fig. 9.** Convergence speed of the SOGI-PLL phase-loop

For a better observation, a new region presenting the convergence speed in function of the phase-loop gains is shown in Fig. 9b, where it is possible to observe that yellow area covers the best and shortest synchronisation times of the circuit. Thus, in sequence, a new database was generated to identify those who presents an output-signal waveform with THD lower than 2%. Through inspection, it was found that the optimal gains for this particular analysis are referred to $k_i = 1225$ and $k_p = 75$. Through the selected gains, the SOGI-PLL with notch filter presented an convergence speed of 66.4 ms and a THD of 0.68%.

### 3.3 APF-PLL Tuning

In comparison to the SOGI-PLL, the same procedure was applied to the APF-PLL. Initially, informations of the settling time was collected with the set of gains in a range defined by $5 < k_p < 1000$ and $5 < k_i < 1000$. Each set was updated with a fixed step of 10 units. Based on the collected results, a contour graphic illustrated in Fig. 10b was generated. One may note that all of the results presented a settling time lower than 100 ms. Due to the lack of visibility of the




**(a)** Complete range **(b)** Zoomed graph

**Fig. 10.** Convergence speed of the APF-PLL phase-loop

initial contour region and aiming to a better observation of the region containing the shortest PLL convergence speed, a second graph was generated with a range limited for the gains, $5 < k_i < 1000$ and $5 < k_p < 150$. Through inspection, the chosen gains correspond to $k_p = 45$ and $k_i = 425$, reaching an accommodation time of 49.9 ms and a THD of 0.62%.

## 4 Simulations and Experimental Results

In this section it is presented the simulation and experimental results of the 3 PLLs, with the chosen gains through the proposed method. In all of the test cases, the input signal was given by:

$$v_{in}(t) = sin(\omega_1 t) + \frac{1}{3}sin(3\omega_1 t) + \frac{1}{5}sin(5\omega_1 t) + \frac{1}{7}sin(7\omega_1 t), \tag{16}$$

being $\omega_1$ 60 Hz fundamental frequency. Furthermore, it was only considered the transient when the PLLs were turned on.

The experimental results were obtained through a digital signal processor (DSP), with a internal clock of 150 MHz and sampling frequency of 40 kHz. The output signals were modulated through PWM (Pulse Width Modulation) technique. Small passive filters were used to attenuate the high-frequency component resulted from the switching frequency. On the other hand, the simulation results were obtained through Octave program.

### 4.1 Simulation and Experimental Results of the E-PLL

Figure 11a represents the phase-loop error before ($e_f(t)$) and after the notch filter ($e_{ff}(t)$). In addition, it is also illustrated the input and output signals. As expected, the notch filter did not compromised the phase-loop dynamics, reaching the steady-state condition in a time period lower than 2 cycles of the fundamental frequency. In sequence, Fig. 11b illustrates the amplitude-loop error ($e_a(t)$) together with the spectrum harmonic of the input and output signals.

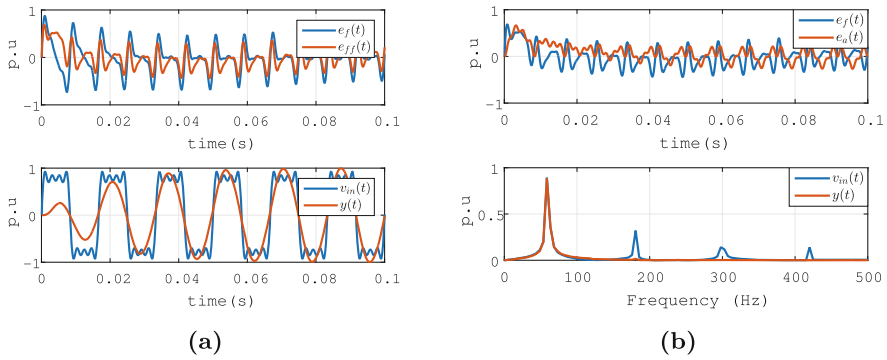



**Fig. 11.** E-PLL simulation results: (a) Phase-loop error with and without notch filter, including the input and output signals and (b) Amplitude-loop error with the harmonic spectrum of the input and output signals.

One may note that the amplitude-loop error reached its steady-state in a time period lower than 3 cycle periods.

Other aspect that should be highlighted is the notch filter performance, which one was designed to smooth an amount of the oscillating components in the phase-loop only. Thus, for keeping the THD of the output signal below 2%, both integrators contributed as low-pass filters, attenuating the oscillating components of $e_{ff}(t)$ and $e_a(t)$.

In sequence, the experimental results are illustrated in Fig. 12, evaluating the previous results obtained through simulations. As expected, the phase-loop, even with the notch filter, presents a faster dynamics in comparison to the amplitude-loop as shown in Fig. 12b. Moreover, from Fig. 12d, one may note that the output signal presents an small third harmonic component, with $e_a(t)$ having a stronger influence due to their oscillating components. Nevertheless, its THD is 2% below, which was previously defined.

### 4.2 Simulation and Experimental Results of the SOGI-PLL

In sequence, there are the simulation and experimental results of the SOGI-PLL. Initially, Fig. 13 presents the acquired results from simulation, where Fig. 13a shows the phase-loop error before ($v_q(t)$) and after ($v_{qf}(t)$) the notch filter with the input and output signals. The harmonic spectrum of the input and output signals are shown in Fig. 13b. One may note that, despite of $y(t)$ does not present the harmonic contents of $v_{in}(t)$, $y(t)$ still has an small $3^{rd}$ harmonic due to the residual oscillating components in $v_{qf}(t)$.

Figure 14 introduces the experimental results at steady-state. From Fig. 14b note that, in comparison to $v_{in}(t)$, $v_\alpha(t)$ and $v_\beta(t)$ present a lower harmonic distortion due to the SOGI-loop integrators. Furthermore, the harmonic content in $v_\beta(t)$ is even lower in comparison to $v_\alpha(t)$. It occurs due to the double integrator action to generate $v_\beta(t)$. Nonetheless, both signals still present har-

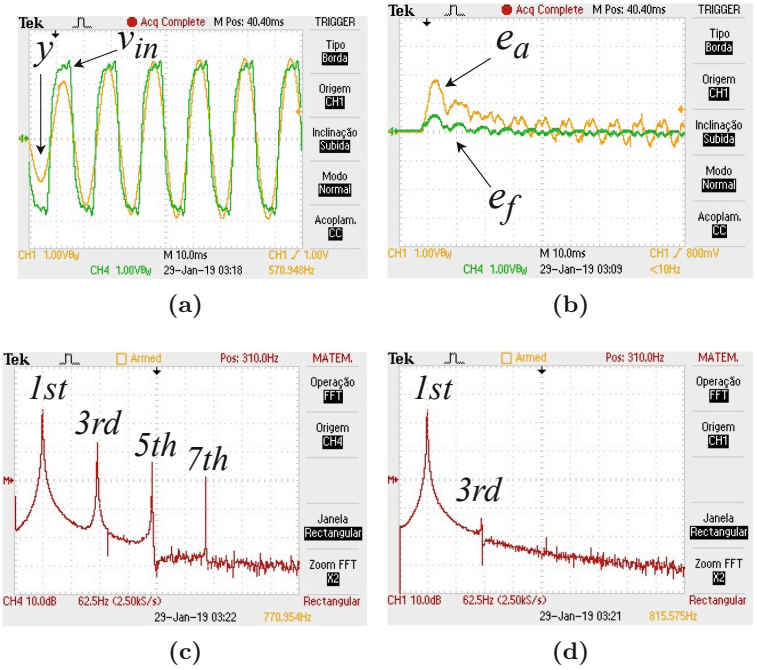



**Fig. 12.** E-PLL experimental results: (a) input and output signals, $v_{in}(t)$ and $y(t)$; (b) phase-loop error ($e_{ff}(t)$) and amplitude-loop error ($e_a(t)$); (c) FFT of the input $v_{in}(t)$, and; (d) FFT of the output signal $y(t)$.

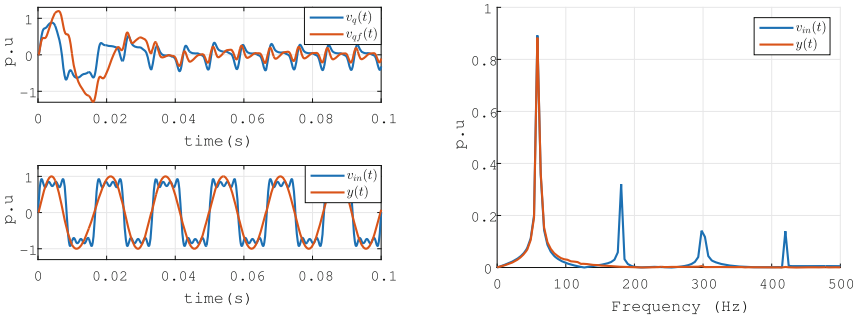



**Fig. 13.** SOGI-PLL simulation results: (a) Phase-loop error before ($v_q(t)$) and after ($v_{qf}(t)$) the notch filter; (b) Harmonic spectrum of the input and output signals.

monic distortion which reinforces the importance of the notch filter, combined with the integrator in the phase-loop, for reducing the oscillating-components propagation through the phase-loop for generating the output signal, $y(t)$.

In sequence, the harmonic spectrum of the input and output signals are shown in Fig. 14c and d, respectively. As aforementioned in this section, $y(t)$ still has an smaller $3^{rd}$ harmonic component, due to the oscillating components in the signal that corresponds to the phase-loop error ($v_{qf}(t)$). Nonetheless, $y(t)$ presents THD below than 1%, which is acceptable based on the initial constraints for tuning the internal parameters.

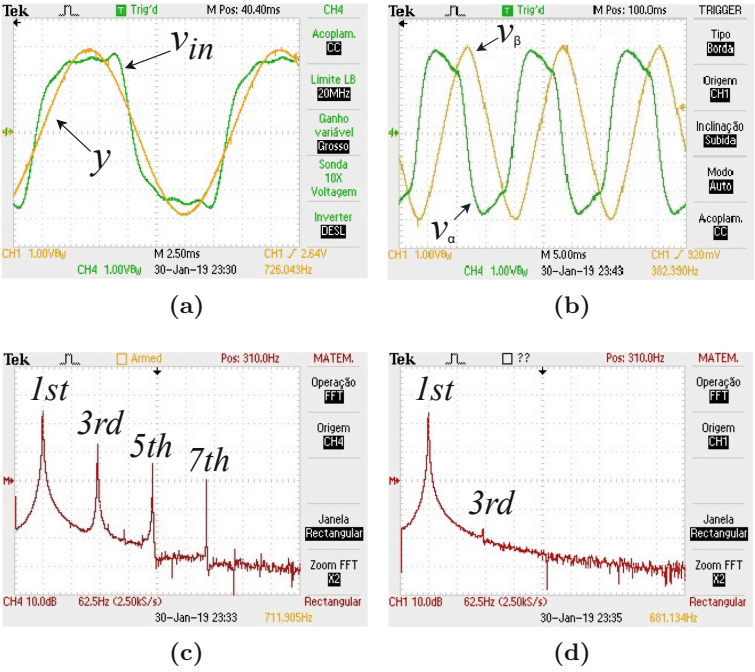



**Fig. 14.** SOGI-PLL experimental results: (a) input and output signals, $v_{in}(t)$ and $y(t)$; (b)quadrature auxiliary signals, $v_\alpha(t)$ and $v_\beta(t)$; (c) FFT of the input signal $v_{in}(t)$; and (d) FFT of the output signal $y(t)$.

### 4.3 Simulation and Experimental Results of the APF-PLL

Simulation results acquired from APF-PLL are shown in Fig. 15, where Fig. 15a presents the phase-loop error before ($v_{qf}(t)$) and after ($v_q(t)$) notch filter, with the input ($v_{in}(t)$) and output ($y(t)$) signals, whereas Fig. 15b illustrates the harmonic spectrum of $v_{in}(t)$ and $y(t)$. In comparison with SOGI-PLL, instead of having some differences for generating the auxiliary signals before the phase-loop, both PLLs presented a similar performance. It has occurred due to the proposed method for tuning the internal parameters of the loop-error, forcing both PLLs for presenting a similar performance to reach the steady-state condition with the output signal presenting THD below than 2%.

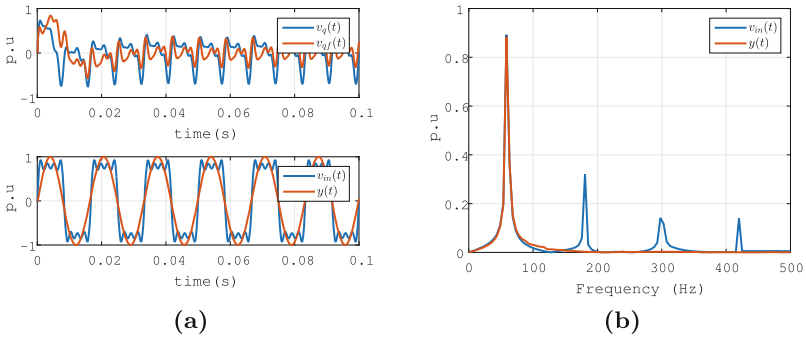



**Fig. 15.** APF simulation results: (a) Phase-loop error before ($v_q(t)$) and after ($v_{qf}(t)$) the notch filter; (b) Harmonic spectrum of the input and output signals.

In sequence the experimental results are shown in Fig. 16, with Fig. 16a presenting the input and output signals, whereas the phase-loop error before and after notch filter are illustrated in Fig. 16b. The harmonic spectrum of the input and output signals are shown in Fig. 16c and d, respectively.

It is important to comment that, instead of $y(t)$ having $3^{rd}$ and $5^{th}$ harmonic-components, its THD is still below than 1%. Furthermore, the steady-state condition was reached in a time period lower than 3 cycle periods (50 ms), and one may note the phase-loop error ($v_q(t)$) presenting the $2^{nd}$ harmonic component as the highest one, and the filtered signal ($v_{qf}(t)$) with a very small ripple.

**Table 1.** Summary of settling times and THD for the PLL models analysed

| PLL Model | EPLL | | | SOGI-PLL | | APF-PLL | |
|---|---|---|---|---|---|---|---|
| Filter | Notch | | | Notch | | Notch | |
| Parameter | $T_{phase}$ | $T_{amp}$ | THD(%) | $T_{phase}$ | THD(%) | $T_{phase}$ | THD(%) |
| Simulation | 41.6 ms | 49.9 ms | 1.687 | 66.4 ms | 0.6844 | 49.8 ms | 0.6934 |
| Experimental | 30 ms | 49.9 ms | 1.687 | 62 ms | 0.6844 | 50 ms | 0.6934 |

Table 1 summarises all PLLs models dynamics, showing that all PLLs with notch filter in the phase-loop reach the steady-state close to the third wave cycle, but with different harmonic distortion. While E-PLL and APF-PLL had similar dynamic in the settling time, SOGI-PLL and APF-PLL had better results regarding THD reaching a value below 1%, half of the proposed value. The E-PLL obtained a THD of 1.69%.

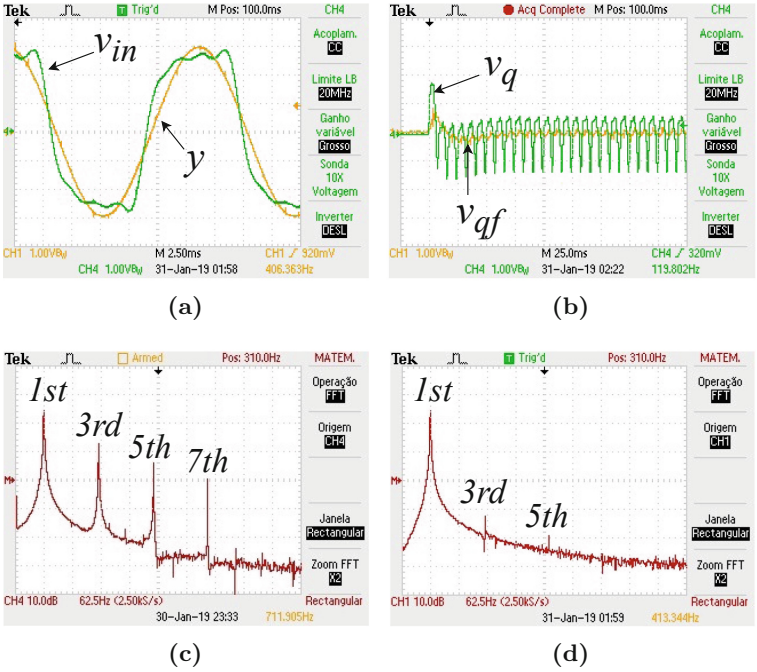



**Fig. 16.** APF-PLL experimental results: (a) input and output signals, $v_{in}(t)$ and $y(t)$; (b) phase-loop error before ($v_q(t)$) and after ($v_{qf}(t)$) notch filter; (c) FFT of the input signal $v_{in}(t)$; and (d) FFT of the output signal $y(t)$.

## 5 Conclusion

The present work proposes an approach for tuning single-phase PLLs to mitigate low-frequency oscillation. The proposed method was evaluated to three different PLLs, with all of them presenting orthogonal signal generators: E-PLL, SOGI-PLL, and APF-PLL.

Through simulation and experimental results one may note the capability of the proposed algorithm for tuning PLLs, even then presenting different dynamic behaviours. The employed notch filter was able to attenuate the oscillating component at $2\omega$ without compromising the dynamics of the PLLs for converging to a steady-state condition in a time period specified in the proposed method. Nonetheless, in this work, the coefficients of the notch filter were constant, such that its capability for attenuating the specified frequency could be compromised if frequency deviations were considered. In future works it is intended to exploiting this issue, replacing the constant coefficients with variable ones, in function of the phase-loop output. Furthermore, other transient events must be considered for evaluating the proposed method.

**Acknowledgement.** This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES) – Finance Code 001

## References

1. Sakamoto, S., Izumi, T., Yokoyama, T., Haneyoshi, T.: A new method for digital PLL control using estimated quadrature two phase frequency detection. In: Proceedings of the Power Conversion Conference-Osaka 2002 (Cat. No. 02TH8579). vol. 2, pp. 671–676 (2002). https://doi.org/10.1109/PCC.2002.997599
2. Arruda, L.N., Silva, S.M., Filho, B.J.C.: PLL structures for utility connected systems. In: Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No. 01CH37248), vol. 4, pp. 2655–2660 (2001). https://doi.org/10.1109/IAS.2001.955993
3. Modesto, R.A., da Silva, S.A.O.: Controladores srf aplicados em condicionadores ativos de potência em sistemas trifásicos a quatro-fios. UNOPAR Científica Ciências Exatas e Tecnológicas, **8**(1) (2009). https://revista.pgsskroton.com/index.php/exatas/article/view/609
4. Sepahvand, H., Saniei, M., Mortazavi, S.S., Golestan, S.: Performance improvement of single-phase PLLs under adverse grid conditions: an FIR filtering-based approach. Electric Power Syst. Res. **190**, 106829 (2021). https://doi.org/10.1016/j.epsr.2020.106829
5. Silva, S.M., Lopes, B.M., Filho, B.J.C., Campana, R.P., Bosventura, W.C.: Performance evaluation of PLL algorithms for single-phase grid-connected systems. In: Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting, vol. 4, pp. 2259–2263 (2004). https://doi.org/10.1109/IAS.2004.1348790
6. Abramovitch, D.: Phase-locked loops: a control centric tutorial. In: Proceedings of the 2002 American Control Conference (IEEE Cat. No. CH37301). vol. 1, pp. 1–15 (2002). https://doi.org/10.1109/ACC.2002.1024769
7. Golestan, S., Guerrero, J.M., Vasquez, J.C.: Single-phase PLLs: a review of recent advances. IEEE Trans. Power Electron. **32**(12), 9013–9030 (2017). https://doi.org/10.1109/TPEL.2017.2653861
8. Karimi-Ghartema, M.: Enhanced Phase-Locked Loop Structures for Power and Energy Applications, chap. 1–5. Wiley-IEEE Press (2014). https://doi.org/10.1002/9781118795187
9. Karimi-Ghartemani, M.: Linear and pseudolinear enhanced phased-locked loop (EPLL) structures. IEEE Trans. Ind. Electron. **61**(3), 1464–1474 (2014). https://doi.org/10.1109/TIE.2013.2261035
10. Karimi-Ghartemani, M., Khajehoddin, S.A., Jain, P.K., Bakhshai, A., Mojiri, M.: Addressing DC component in PLL and notch filter algorithms. IEEE Trans. Power Electron. **27**(1), 78–86 (2012). https://doi.org/10.1109/TPEL.2011.2158238
11. Karimi-Ghartemani, M., Khajehoddin, S.A., Jain, P.K., Bakhshai, A.: Derivation and design of in-loop filters in phase-locked loop systems. IEEE Trans. Instrum. Meas. **61**(4), 930–940 (2012). https://doi.org/10.1109/TIM.2011.2172999
12. Golestan, S., Monfared, M., Freijedo, F.D., Guerrero, J.M.: Dynamics assessment of advanced single-phase PLL structures. IEEE Trans. Ind. Electron. **60**(6), 2167–2177 (2013). https://doi.org/10.1109/TIE.2012.2193863
13. Xiao, F., Dong, L., Li, L., Liao, X.: A frequency-fixed SOGI-based PLL for single-phase grid-connected converters. IEEE Trans. Power Electron. **32**(3), 1713–1719 (2017). https://doi.org/10.1109/TPEL.2016.2606623

14. Thacker, T., Wang, R., Dong, D., Burgos, R., Wang, F., Boroyevich, D.: Phase-locked loops using state variable feedback for single-phase converter systems. In: 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pp. 864–870 (2009). https://doi.org/10.1109/APEC.2009.4802763
15. Hogan, D.J., Gonzalez-Espin, F.J., Hayes, J.G., Lightbody, G., Foley, R.: An adaptive digital-control scheme for improved active power filtering under distorted grid conditions. IEEE Trans. Ind. Electron. **65**(2), 988–999 (2018). https://doi.org/10.1109/TIE.2017.2726992
16. Sedra, A., Sedra, D., Smith, K., Smith, P.: Microelectronic circuits. Oxford Series in Electrical and Computer Engineering, pp. 678–696. Oxford University Press (1998). https://books.google.com.br/books?id=RcodQm6LaVEC
17. Rolim, L.G.B., da Costa, D.R., Aredes, M.: Analysis and software implementation of a robust synchronizing PLL circuit based on the pq theory. IEEE Trans. Ind. Electron. **53**(6), 1919–1926 (2006). https://doi.org/10.1109/TIE.2006.885483
18. Kulkarni, A., John, V.: A novel design method for SOGI-PLL for minimum settling time and low unit vector distortion. In: IECON 2013–39th Annual Conference of the IEEE Industrial Electronics Society, pp. 274–279 (2013). https://doi.org/10.1109/IECON.2013.6699148
19. Gardner, F.M.: Phaselock Techniques, 3rd edn, pp. 8–63. Wiley, Hoboken (2005). https://doi.org/10.1002/0471732699
20. Kroupa, V.F.: Phase Lock Loops and Frequency Synthesis, chap. 4. Wiley, Hoboken (2003). https://doi.org/10.1002/0470014105
21. Leonov, G., Kuznetsov, N., Seledzhi, S.: Nonlinear analysis and design of phase-locked loops. In: Rodić, A.D. (ed.) Automation and Control, chap. 7. IntechOpen, Rijeka (2009). https://doi.org/10.5772/7900
22. Lindsey, W.C., Simon, M.K.: Telecommunication Systems Engineering, chap. 2–3. Dover Books on Electrical Engineering, Dover Publications (1991). https://books.google.com.br/books?id=m2-tYwrNMPQC
23. Viterbi, A.J.: Principles of Coherent Communication, chap. 2–5. McGraw-Hill, New York (1966)
24. Encinas, J.: Phase Locked Loops, chap. 2-3. Microwave and RF Techniques and Applications. Springer, New York (2012)
25. Meyr, H., Popken, L., Mueller, H.: Synchronization failures in a chain of PLL synchronizers. IEEE Trans. Commun. **34**(5), 436–445 (1986). https://doi.org/10.1109/TCOM.1986.1096569
26. Lessa, D.M.: Uso combinado de filtros digitais com circuitos de sincronismo monofásico. Master's thesis, Universidade do Estado do Rio de Janeiro (2019). https://www.pel.uerj.br/bancodissertacoes/Dissertacao_Dayane_Lessa.pdf