Implementation of Non-stationary Channel Emulator Based on USRP

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Abstract. Inspired by the modular design of virtual instruments, a discrete non-stationary channel model and a flexible hardware architecture are proposed in this paper. On this basis, a universal channel emulator is implemented on universal software radio peripheral (USRP) platform. Moreover, we proposed a sum of linear frequency modulation (SoLFM) method to accurately generate non-stationary channel fading with continuous phase, i.e., Rayleigh fading, Rice fading, and log-normal fading channels. In addition, hardware measurement results demonstrate that the measured statistical properties are well consistent with the corresponding theoretical ones.

Keywords: USRP · Virtual instrument · Non-stationary channel fading · SoLFM

1 Introduction

Wireless communication systems have played an important role in many important fields, such as satellite communication, telemedicine and mobile communication. In order to ensure the security and reliability of wireless communication systems, measurement campaigns should be taken into account under realistic conditions [1–3]. However, field tests are expensive and unrepeatable, which means large-scale test scenarios are limited. Alternatively, the channel emulator can reproduce the real channel in the laboratory for fast prototyping and performance evaluation of wireless communication systems under different conditions, which greatly reduces the research and development costs and production cycle [4–7].

There are several commercial channel emulators available, such as Elektrobit Propsim C8 and Spirent SR5500, which are extremely bulky and expensive. Moreover, they are mainly designed for standard channel models and inflexible to customize different functionality. In [8], the authors describe an improved scheme for Rayleigh fading channels based on field programmable gate array (FPGA), which achieved an improvement in resource consumption. In [9], a hardware correlated Lognormal distributed sequence generator based on FPGA was proposed.

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However, the hardware architecture of above researches mainly focused on the specific algorithm verification, which is not suitable for channel emulation of all kinds of fading. In [10], researchers developed an emulator to assess the bit error rate (BER) performance of multi-hop, multi-carrier communication systems on Universal Software Radio Peripheral (USRP). It should be noted that software-defined radio (SDR) are suitable options which offer flexibility and low cost in prototyping.

To the best of our knowledge, traditional emulators are designed for wide-sense stationary (WSS) [11]. However, a large number of researches [12–15] proved that the real channel has non-stationary characteristics. Although the study on non-stationary channel was carried out in [16], the parameter update was only a simple segment. Thus, the phase of the fading is not a smooth transition between adjacent channel states, which generates a deviation in the doppler frequency. This paper aims to overcome the problem. The major contributions and novelties of this paper are summarized as follows:

1) Considering the abrupt phase change characteristic between adjacent channel states, a sum of linear frequency modulation (SoLFM) method is proposed to generate non-stationary channel fading with continuous phase.
2) Based on the modular design of virtual instruments, we can focus on architectural and algorithmic issues which are of great significance for design. A low complexity universal hardware architecture is proposed and validated.
3) With the idea of SDR, a channel emulator is designed and implemented to efficiently reproduce multipath fading such as Rayleigh fading, Rice fading, and Lognormal fading, and reproduce the characteristics of the propagation in the laboratory.

The rest of this paper is organized as follows. Section 2 describes the system model and the system architecture of the emulator. Section 3 gives the design of the Non-Stationary Channel Emulation. Hardware test and validation are presented in Sect. 4. Finally, conclusions are drawn in Sect. 5.

2 Channel Emulator Design

Affected by the reflection and scattering of obstacles in the complex wireless communication environment, the signal reaching the receiver is made up of multiple paths with different power and delay [17]. In the condition of no obstacles between the transceivers, the signal travels in a straight line, which is called line-of-sight (LoS) path, otherwise it is a non-line-of-sight (NLoS) path [18]. Considering that FPGA has the characteristics of discretization and fixed-point operation, we propose a model which the discrete channel impulse response (CIR) can be expressed as

$$\begin{aligned} h(l,\varsigma) = {} & c^{\mathrm{LoS}}(l)h^{\mathrm{LoS}}(l)\delta(\varsigma - \left|\tau^{\mathrm{LoS}}(l)\right|_{T_s}) \\ & + \sum_{k=1}^{K(t)} c_k^{\mathrm{NLoS}}(l)h_k^{\mathrm{NLoS}}(l)\delta(\varsigma - \left|\tau_k^{\mathrm{NLoS}}(l)\right|_{T_s}) \end{aligned} \tag{1}$$

where l is the label of the discrete sequence obtained by sampling the time domain signal, ς denotes the label of the discrete sequence obtained by sampling the delay domain signal, T_s represents the sampling period, $\left|\tau_k^{\mathrm{LoS}}(l)\right|_{T_s}$ and $\left|\tau_k^{\mathrm{NLoS}}(l)\right|_{T_s}$ denote the rounding delay results of the LoS and NLoS paths, respectively. To carry out the real-time calculation of the output signal sample stream, the channel emulator convolves the discrete-time input signal with the discrete CIR in (1) as follows:

$$\begin{aligned} y(l) = {} & c^{\mathrm{LoS}}(l)h^{\mathrm{LoS}}(l)x(l)\delta(\varsigma - \left|\tau^{\mathrm{LoS}}(l)\right|_{T_s}) \\ & + \sum_{k=1}^{K(t)} c_k^{\mathrm{NLoS}}(l)h_k^{\mathrm{NLoS}}(l)x(l)\delta(\varsigma - \left|\tau_k^{\mathrm{NLoS}}(l)\right|_{T_s}) \end{aligned} \tag{2}$$

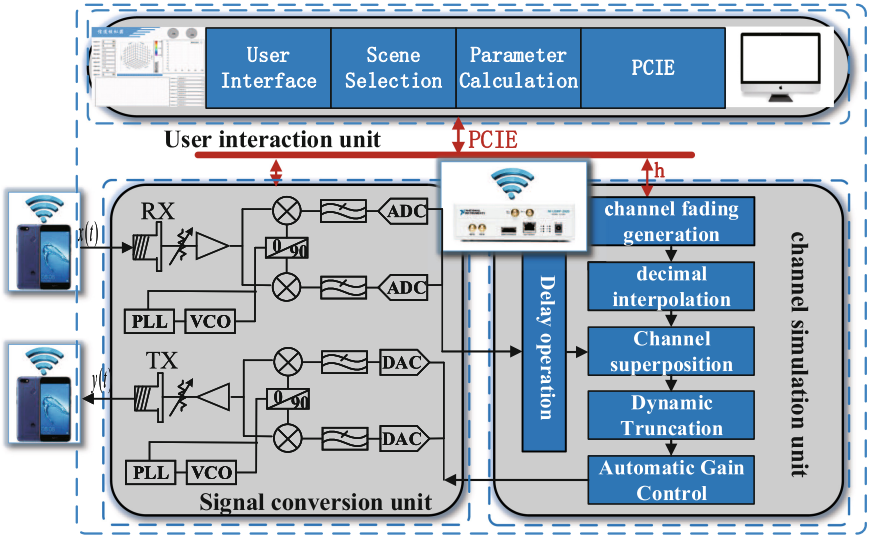

Fig. 1. Architecture of proposed channel emulator.

In order to accurately reproduce a wireless channel in a physical environment, this paper designs a flexible and reconfigurable channel emulator on the basis of (2). The emulator is designed by Labview FPGA module on the National Instrument USRP-Rio 2943R Software-Defined Radio platform which is equipped with a Xilinx Kintex-7 FPGA. As shown in Fig. 1 and Fig. 2, the channel emulator is made up of three units: user interaction unit, signal conversion unit and channel simulation unit. The user interaction unit provides a visual operation interface for users to configure associated parameters such as path delay, fading type, and spectrum shape. In the meanwhile, the RF input signals are down converted and sampled to digital complex baseband signals by the signal conversion unit. As the core part of the simulator, the channel simulation unit generates a non-stationary

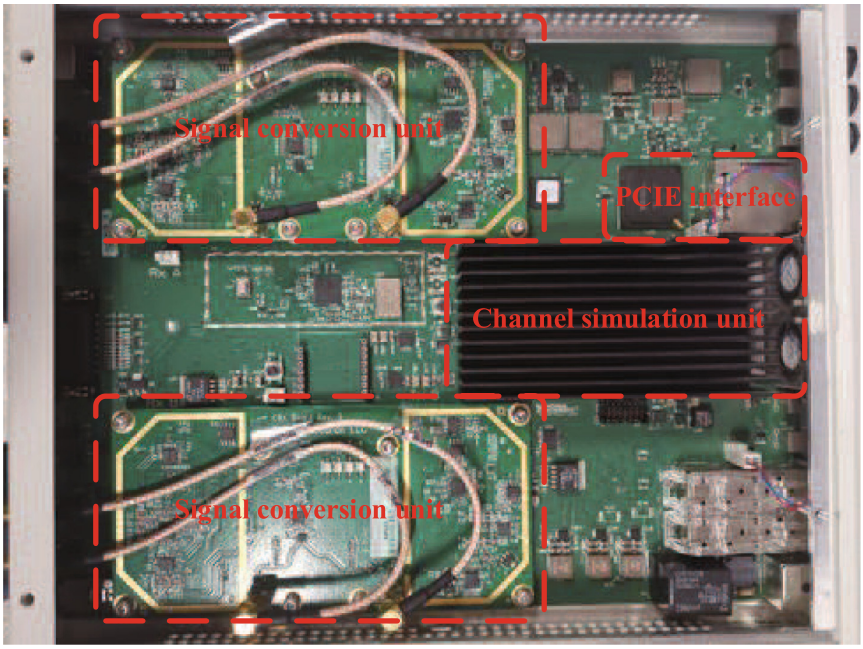

Fig. 2. Channel emulator hardware.

channel fading by SoLFM using the parameters above and combines it with the digital signals to produce a wireless environment. Moreover, the bit width of the output channel fading is 30 bits, which is a waste of hardware courses. To ensure a good tradeoff between the accuracy and resource consumption, it is truncated to 20 bits. However, the reduction of the bit width still results in the loss of amplitude and accuracy. In order to solve the negative impact of truncation, automatic gain control (AGC) module is added after truncation, which can effectively adjust the overall amplitude of the data to decrease the loss of accuracy.

3 Non-stationary Channel Fading Emulation

3.1 Principle of SoLFM Method

Traditional channel emulator often used sum of cisoids (SoC) method [19,20] to generate channel fading coefficients. The essence of the method is the sum of harmonics with different delays and power taking the place of the effects of direct radiation, scattering, reflection, and refraction during the wireless propagation,

$$\tilde{h}\left(t\right) = \lim_{N\to\infty} \sum_{n=1}^{N} e^{j(2\pi f_n t + \theta_n)} \tag{3}$$

where θ_n and f_n denote the initial phase and Doppler frequency of different branches. However, this method does not take into account the real-time changes of the channel parameters caused by the movement of the transceiver or scatterer. In other words, the channel does not meet the condition of wide sense stationary (WSS).

In order to solve this problem and reduce the complexity of hardware implementation, this article adopts the SoLFM method to generate non-stationary stochastic fading by upgrading $2\pi f_n(t)t$ to $2\pi \int_0^t f_n(\tau)\mathrm{d}\tau$.

$$\tilde{h}(t) = \sum_{n=1}^{N} \sqrt{\frac{1}{N}} e^{j\left(2\pi \int_0^t f_n(\tau)\mathrm{d}\tau + \theta_n\right)} \tag{4}$$

Meanwhile, due to the time-discrete characteristic of the hardware implementation, the model is further discretized as follows:

$$\tilde{h}(k) = \sum_{n=1}^{N} \sqrt{\frac{1}{N}} e^{j\left(2\pi \sum_{m=0}^{k} T_s f_n[m] + \theta_n\right)} \tag{5}$$

where m is the discrete time index, N is the number of sub-paths, T_s denotes the channel sampling period, $f_n[m]$ represents the discrete doppler frequency of sub-path, and θ_n is the random initial phase.

3.2 Hardware Implementation

The embedded Kintex-7 FPGA on the USRP Software-Defined Radio platform allows for the fast hardware implementation of the algorithm above. The hardware implementation with visual operations by Labview FPGA module include two key components. The embedded block RAM and ROM generate frequency control word and initial phase θ_n. Meanwhile, the look-up tables (LUT) combine the signals above to generate a time-varying fading with continuous phase based on the concept of direct digital synthesis (DDS). Instead of using existing Xilinx highly integrated intellectual property (IP), we design the prototype based on manual RTL-level design in HDL codes, which is tailored for our specific needs and costs less hardware sources.

As for implementation of the real-time delays in the tapped-delay line (TDL) Architecture, which is capable of performing the real-time convolution calculation by simple complex multiplication and additions, an embedded dual-port block RAM is adopted for parallel processing and real-time performance in Fig. 3. Limited to the sample rate of 100 MHz, the resolution of the delays is 10 ns, which satisfies the requirement of accuracy for most radio devices. Meanwhile, the maximum delay is decided by the depth of embedded block RAM available per path. Configuring the depth of 10000 can reach up to delay of 100 us, which is large enough for outdoor environment.

Just as depicted in formula (2), the path delay $\left|\tau_k^{\mathrm{LoS}}(l)\right|_{T_s}$ denotes delayed signal and $h_k^{\mathrm{NLoS}}(l)$ is realized by the non-stationary channel fading in the tapped-delay line architecture. Considering the fact that the sampling rate of the fading

is different from the delayed signal, they cannot perform multiplication operations directly. Consequently, a linear interpolator is needed before the TDL to raise the low sampling rate of the fading in real time to complete the hardware implement.

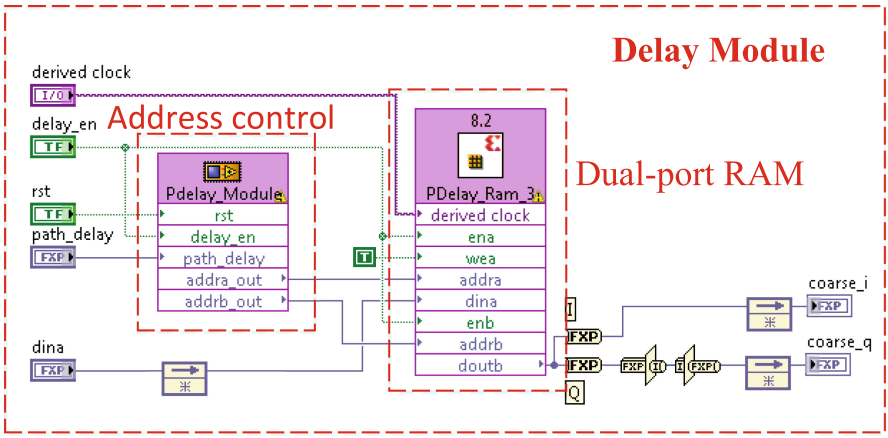

Fig. 3. Architecture of channel delay module.

Table 1. Resource consumption of FPGA.

Device Utilization	Used	Total	Percentage
Total Slices	17641	63550	27.8
Slice Registers	57792	508400	11.4
Slice LUTs	29657	254200	11.7
Block RAMs	133	795	16.7
DSP48s	302	1540	19.6

3.3 Resource Consumption

Following the above prototype design with the help of LabVIEW FPGA module, the whole channel emulator has been successfully implemented on the USRP Software-Defined Radio platform. It hosts an embedded Kintex-7 chip, which consists of about 508400 Slice Registers, 254200 Slice LUTs, 795 Block RAMs and 1540 DSP48. Taking one path for example, Table 1 summarizes the resource consumption after synthesis and implementation at 100 MHz using LabVIEW built-in local compiler. It can be seen from the table that DSP48s and Block

RAMs consume large amounts of resources, which occupy 19.6% and 16.7%, respectively. It mainly derived from the TDL, for multiplication and addition operations, and the channel delay for embedded block RAM. Considering the intrinsic consumption of the module, the embedded source is enough for 4 paths.

4 Measurements and Validations

In order to demonstrate the performance analysis and verify the effectiveness of the emulator intuitively, output waveform and amplitude distribution must be observed and calculated. Consequently, the testbed consists of a USRP as the channel emulator, a signal generator (Agilent E4438C) providing a 2 GHz carrier signal for testing, and an oscilloscope (Agilent N9340B) observing the measured waveform of channel emulator. Meanwhile, an industrial personal computer (IPC) running LabVIEW 2018 is connected to the USRP by the peripheral

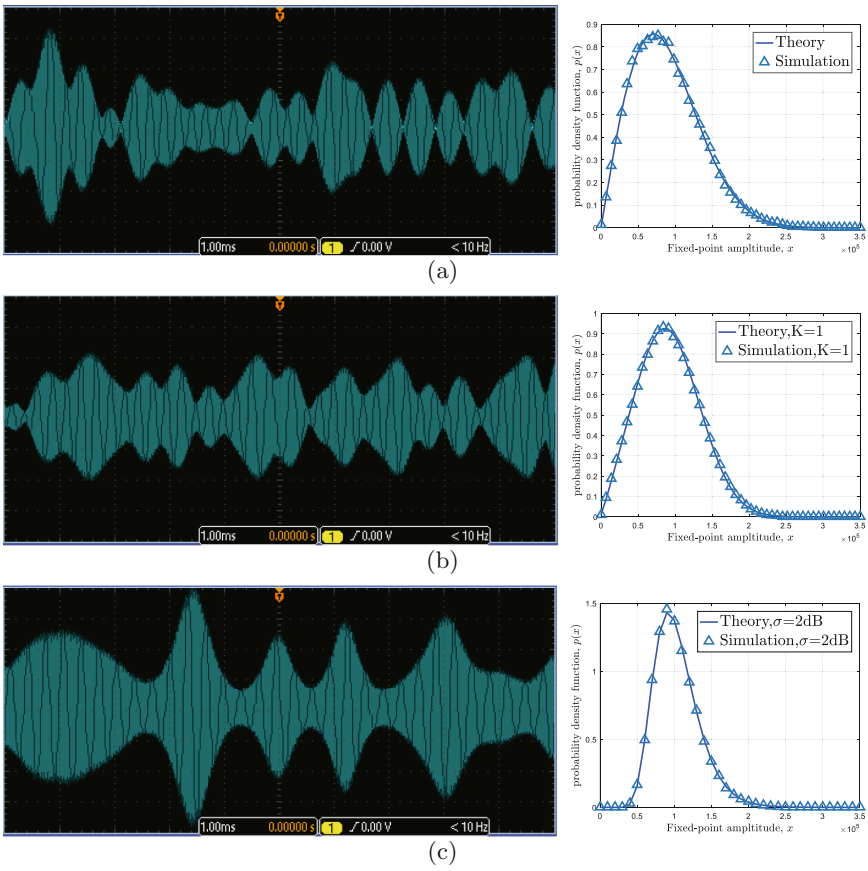

Fig. 4. Waveforms and PDFs of different channel fading (a) Rayleigh (b) Rice (c) Lognormal.

component interconnect express (PCIe) interface. At the beginning of the system, the host IPC downloads the compiled bitfiles into the FPGA and configures related channel parameters to be measured.

After the measurement, the output of waveform is shown in Fig. 4. Moreover, a large number of the measured waveform data are taken for statistical analysis of probability distribution function (PDF) by Matlab, which is shown in Fig. 4. It can be seen that the maximum distortion of the Rice distribution is 1.48% and the statistical Rician K-factor, K =1.02, is consistent with the input one, K = 1. The Rayleigh PDF deviation is 0.14 dB, and the maximum distortion of the lognormal distribution is 3.89%. In the meanwhile, the output of doppler power spectral density (DPSD) is shown in Fig. 5. The results show that the measured value is in good coincidence with the theoretical one and the emulator produces a physical channel which is similar to the natural one.

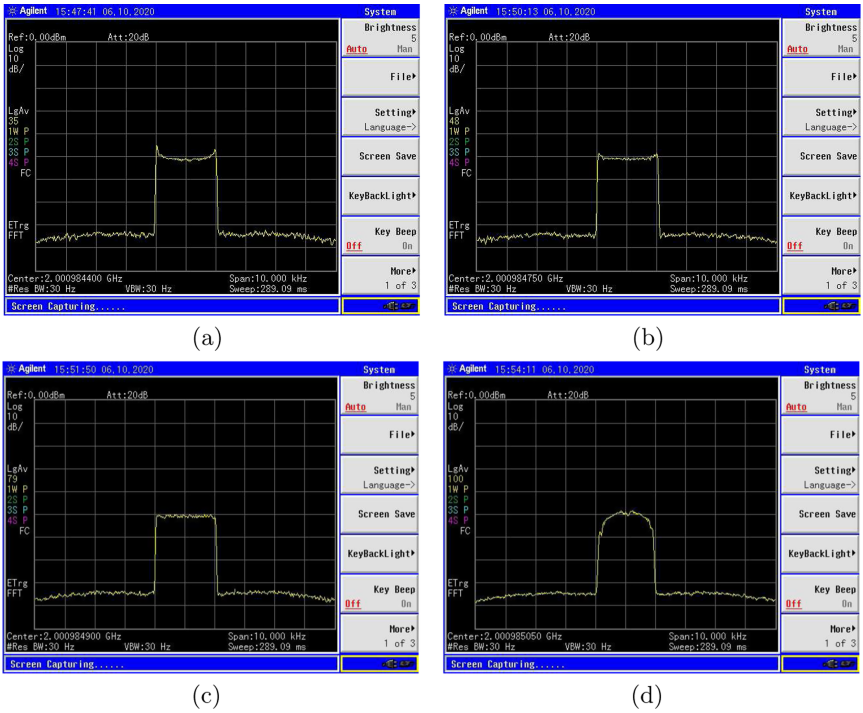

Fig. 5. Measured results of different DPSDs of (a) Jakes 6 dB (b) Jakes 3 dB (c) Flat (d) Round.

5 Conclusions

In this work, the design and prototypical implementation of a real-time channel emulator have been investigated based on the idea of virtual instrument

and the USRP-RIO hardware implementation platform of National Instruments Corporation. The design allows to generate time-varying channel fading with continuous phase, such as Rayleigh fading, Rice fading and Lognormal fading in laboratory. It solves the problem that the wireless communication system cannot be quickly tested, and greatly reduces the research and development cost. Furthermore, hardware measurement results have demonstrated that the measured PDF agrees well with the theoretical ones, which verifies the feasibility of proposed scheme and implementation.

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