Online Interactive Teaching System of Sanda Course Based on P2P Network

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Abstract. In order to improve the online teaching effect of sanda, this study designed an online interactive teaching system of sanda based on P2P network. The microcontroller is taken as the core of the hardware part of the system, and the processor, CPU sub-board and compatible motherboard are designed. After debugging, the normal transceiver of the hardware environment is realized. Then, on the basis of designing system function modules and database structure based on P2P network, the index function of the system is designed to complete the construction of system software environment. Experimental results show that the system improves the interactive efficiency, teaching performance and content collection accuracy, and effectively improves the teaching effect.

Keywords: P2P network · Sanda course · Online interactive teaching · Controller

1 Introduction

Network teaching has become an important way of education and teaching reform in Colleges and universities, and has been applied in various courses of education. Network teaching system is a virtual education and teaching environment based on P2P network on the Internet or campus network. Through this platform, the functions of teaching, communication, resource sharing and autonomous learning can be realized.

Most of the current network teaching assistance systems usually use B/S or C/S access mode. Among them, education and teaching resources are usually concentrated on the server side of the system, and each user's PC side cannot realize the exchange of learning resources. Although this method can meet the needs of the classroom, there are still problems in the following aspects: the first network, the single point of failure problem. Since the learning resources are provided on the server side, if there is a problem on the server side of the P2P network, the system cannot run; secondly, the cost is high. In order to better meet the needs of the system, it is necessary to construct various teaching services, and at the same time, with the increase of clients, higher requirements are placed on the server and data; third, the scalability is poor. When the number of users increases, the number of expensive servers needs to be increased to provide more stable services.

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P2P technology, as a kind of application technology of P2P network, was proposed in the 1990s of the last century. It mainly uses the nodes in the entire network to perform peer-to-peer computing, so that the space resources existing in the network can be fully mined. It has great advantages in fault tolerance, utilization and scalability. Therefore, in view of the above-mentioned problems, this paper proposes an online interactive teaching system for Sanda courses based on P2P network.

2 System Hardware Design

The hardware structure of the system is shown in Fig. 1.

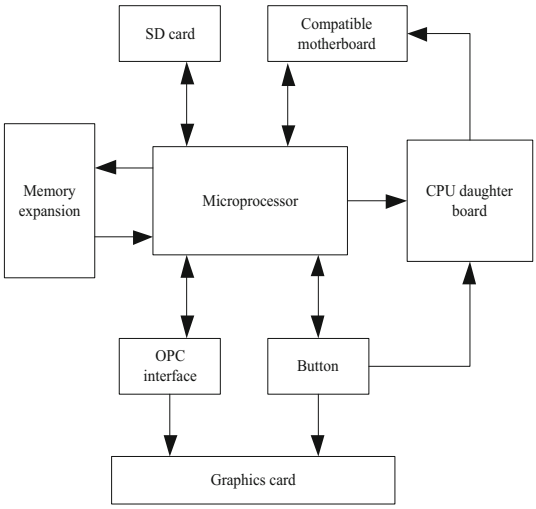

Fig. 1. System hardware structure

In this study, the microprocessor is taken as the core of the system hardware, as shown below.

2.1 Processor Design

The three embedded processors selected by this system are all ARM9 series processors. S3C2440 is a 32-bit RISC embedded processor based on ARM920T core produced by SAMSUNG Company [1], mainly for handheld devices and applications with high cost performance and low power consumption. The ARM920T core is composed of three parts: ARM9TDMI, storage pipeline unit MMU and cache. Among them, the MMU can manage virtual memory, and the cache consists of an independent 16 KB address and 16 KB data high-speed cache.

The ARM920T has two internal coprocessors: CP14 and CP15. Among them, CP14 is used for debugging control, and CP15 is used for storage system control and test

control. In order to reduce the system cost, the following components are integrated inside the S3C2440 chip:

1 LCD controller (independent DMA channel, supports STN and TFT) [2]; External memory controller (SDRAM controller and external chip controller); 4-channel UART; 4-channel DMA controller; 2-channel SPI; IIC bus interface; IIS audio interface and AC97 audio interface; SD/MMC interface; 2 USB host interfaces and 1 USB device interface; 8-channel 10-bit ADC; Touch screen interface; 4 timers with PWM function and an internal clock PLL; Watchdog counter; Camera interface.

On the clock side, the S3C2440 integrates an RTC with calendar function and a clock generator with PLL (MPLL and UPLL). The MPLL generates the master clock, which enables the processor to operate at a frequency of up to 400 MHz. This operating frequency enables the processor to easily run WinCE, Linux and other operating systems and perform more complex information processing [3].

In addition, the S3C2440 adopts an independent power supply method for each component on the chip:

(1) Core: When the main frequency is set to 300 MHz or below, use 1.2 V power supply;
(2) When the main frequency is set to 400 MHz, use 1.3 V to supply power.

The storage unit adopts 3.3 V independent power supply, 3.3 V can be used for general SDRAM, and 1.8/2.5 V can be used for mobile SDRAM. The memory controller of S3C2440 is used to provide control signals to the external memory. The memory controller has the following characteristics:

Support big-endian/little-endian modes (selected by software);
Address space: 1 GB in total, divided into 8 banks, each bank is 128 MB, S3C2440 uses 8 general chip select signals to select these banks;
The start address and size of Bank0 to Bank5 are fixed for ROM or SRAM;
Bank6 and Bank7 are used for ROM, SRAM or SDRAM, the start address and size of these two groups are programmable;
The access cycle of all Banks is programmable;
Supports self-refresh and low-power modes of SDRAM.

In addition, the S3C2440 adopts an independent power supply method for each component on the chip:

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(2) The storage unit adopts 3.3 V independent power supply, 3.3 V can be used for general SDRAM, and 1.8/2.5 V can be used for mobile SDRAM [4, 5].

2.2 CPU Daughter Board Design

The CPU daughter board mainly includes the following modules: ARM chip, power supply and crystal oscillator module, SDRAM module, NANDFlash module, daughter motherboard interface module.

The power supply and crystal oscillator module, on the daughter board, need to have two different voltages for the chip and each peripheral to use. 3V3 voltage, that is, 3.3 V voltage, the memory module of the system needs 3V3 voltage; 1V2 voltage, that is, 1.2 V voltage, the voltage used by the three ARM chips. Because there is only one input voltage from the motherboard to the daughter board, that is, the 3.3 V power supply voltage, a level conversion circuit should be designed in the hardware design for 3V3 to 1V2. The crystal oscillator circuit is an indispensable part of the embedded hardware circuit. The ARM chip obtains the main clock by multiplying the frequency of the external crystal oscillator. According to the requirements of the ARM chip S3C2440, this design provides two crystal oscillators with different frequencies, 16.9344 MHz and 32.768 MHz, for the ARM chip, which are respectively used in normal working mode and sleep mode [6].

SDRAM module, the memory controller of S3C2440 is used to provide control signals to the external memory. The memory controller has the following characteristics:

Support big-endian/little-endian modes (selected by software);
Address space: 1 GB in total, divided into 8 banks, each bank is 128 MB, S3C2440 uses nGCS [0–7]8 general chip select signals to select these banks;
The start address and size of Bank0 to Bank5 are fixed for ROM or SRAM;
Bank6 and Bank7 are used for ROM, SRAM or SDRAM, the start address and size of these two groups are programmable;
The access cycle of all Banks is programmable;
Supports self-refresh and low-power modes of SDRAM.

2.3 Compatible Motherboard Design

The compatible motherboard mainly includes: power supply and reset module and peripheral interface module. The main principle of compatible motherboard design is to ensure compatibility with the three CPU daughter boards [7]. Next, we mainly introduce the core modules on the compatible motherboard.

The structure block diagram of compatible motherboard is shown in Fig. 2.

On the mother board of the power supply and reset module, two different sizes of voltage are set for the chip and each peripheral. The input voltage from the outside to the embedded platform is 5 V, and the voltage from the USB interface and LCD interface is 5 V. The voltage of the peripheral circuit is 3.3 V. Because the external input voltage is fixed, a level conversion circuit should also be designed in the hardware design.

The reset circuit is an essential part of the embedded hardware circuit. The reset circuit in this design can be used for power-on reset or reset by manual button. At the same time, because the network interface chip CS8900A requires high-level reset, a 74HC14 inverter is added to invert the negative pulse of the system reset signal to obtain a positive pulse reset signal.

Ethernet interface module. The three ARM chips do not have an integrated Ethernet controller, so in this design, an Ethernet control chip CS8900 is externally connected to the control signal provided by the memory controller. Among them, the chip select signal of CS8900 selects NET_CS, that is, CS8900 The internal address space is mapped

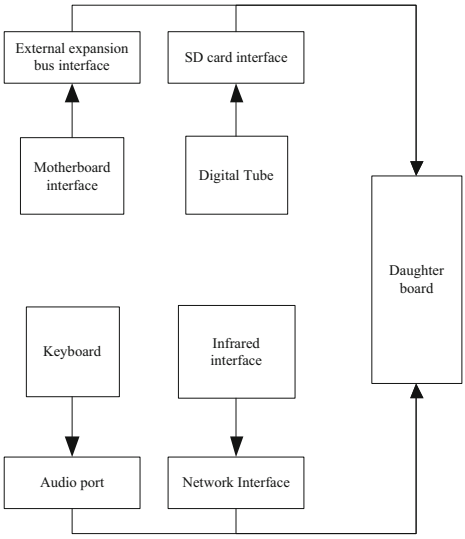

Fig. 2. Compatible motherboard structure block diagram

into the memory space pointed to by NET_CS. The choice of NET_CS is determined by the specific CPU daughter board [8].

LCD and touch screen interface circuit. The LCD selected in this design is the product LTM035A776C of TOSHIBA Company. LTM035A776C is a TFT LCD with touch function. For the S3C2440 daughter board, the touch screen is controlled directly through the dedicated interface of the touch screen provided by the chip; for the two daughter boards AT91SAM9263 and MC9328MX21, the touch screen is controlled by connecting an external AD chip ADS7843 through the SPI interface. Among them, the jumper is used to select which method is currently used to control the touch screen [9].

Audio interface module. The audio interface of the system is realized through the AC97 interface provided by the ARM chip and the external audio codec AD1981. The AC97 controller provides two serial data lines, clock lines and control lines to the external AD1981. AD1981 has three external interfaces, namely: headphone interface, microphone interface, and audio conversion interface.

JTAG interface module. All three ARM chips integrate a JTAG controller, providing data lines and control lines that conform to the JTAG standard, so the JTAG circuit of the system is relatively simple. Keyboard and digital tube circuit, keyboard and digital tube circuit are the key circuits on the teaching experiment platform. Most of the experimental courses include the experimental operation of keyboard and digital tube. There are no keyboard and digital tube controllers in the three ARM chips. This design uses a chip ZLG7290 designed by Zhou Ligong Company as the keyboard and digital tube controllers. ZLG7290 can directly drive 8-bit common-cathode nixie tubes (or 64 independent LEDs), and can also scan and manage up to 64 keys. At the same time, ZLG7290 is connected to the microcontroller by I2C bus, and the interface only needs two signal lines. Considering the board area, this design only expands 16 buttons and 8-bit digital

tubes. The 16 buttons cut out are managed by the signals DIG0-3 and SEGA-D, and the button values are 1–4, 9–12, 17–20, 25–28 respectively.

3 System Hardware Debugging

This section mainly introduces the system debugging method and part of the debugging process. When the printed circuit board is completed, you should not rush to solder the components, but first carefully check the connection of the printed circuit board against the schematic diagram, and check whether the power supply and the ground are short-circuited with a multimeter to ensure that there is no error before welding [10]. After the system is powered on, you should first check whether the circuit works abnormally. It is normal for the chip to have a certain amount of heat during operation. However, if any chip is particularly hot, there must be a fault, and it needs to be powered off and checked to confirm that it is correct before continuing. Power-on debugging. Debugging tools require oscilloscope, multimeter, electric soldering iron, etc., and ARM debugging development software and corresponding emulators. In the process of hardware debugging of this system, the development and debugging software RVDS provided by ARM company and its JTAG emulation software H-JTAG are used. The power supply circuit, crystal oscillator circuit and reset circuit are the basis for the normal operation of the whole system, and these three modules should be tested first [11]. This section mainly takes the S3C2440 platform as an example to introduce the hardware debugging method.

When debugging the power supply circuit, the circuit board after soldering is likely to be short-circuited and soldered [12]. If you directly connect the power supply at this time, it is likely to cause the main chip to heat up and burn. This situation has been encountered during debugging. After soldering the circuit, directly connect to the power supply, and the S3C2440 will start to heat up until it is hot. The correct debugging method is: before the system is powered on, first unplug the jumper near the power circuit on the motherboard to prevent the power circuit from supplying power voltage to the motherboard, and then use a multimeter to test whether the output voltage of the motherboard power conversion circuit is 3.3 V, the jumper can be plugged in under normal circumstances to debug other modules [13], and the test method of the power circuit of the daughter board is the same.

Reset circuit debugging, after the system is powered on, check the working conditions of each interface module, and find that the LED light representing the normal operation of the network card chip CS8900 is not lit normally. After checking the datasheet of CS8900, it is found that CS8900 needs positive pulse to reset, so the positioning problem occurs in the reset circuit. Add a 74HC14 inverter to the reset circuit. In this way, the negative pulse of the system reset signal can be inverted to obtain a positive pulse reset signal and provided to the CS8900. After power-on reset, CS8900 can work normally.

Crystal oscillator circuit debugging, the S3C2440 platform uses 16.9344 MHz and 32.768 kHz crystal oscillators. After power-on, use the oscilloscope to capture the waveforms of the above two crystal oscillators, and observe whether the output waveform parameters of the crystal oscillator are correct and whether the waveform is stable. During the debugging process, it was found that the crystal oscillator circuit of some daughter boards did not start to vibrate. This problem can be solved from two aspects:

① The size of the crystal capacitor;
② Whether the crystal is broken.

The following experience was obtained during the debugging process. Based on the stable operation of the crystal oscillator circuit, it is best to use an active crystal oscillator for the crystal oscillator circuit.

JTAG module debugging, on the premise that the basic circuits such as power supply circuit, crystal oscillator circuit and reset circuit work normally, the JTAG interface should be tested first, because as the dedicated DEBUG interface of the ARM chip, the development and debugging software RVDS is downloaded to the ARM chip through the JTAG interface Debug programs, which in turn debug other peripherals. Connect the development board to the PC through the JTAG interface, and run the H-JTAG software on the PC.

For peripheral circuit debugging, after the JTAG interface test is completed, other interfaces of the hardware platform can be debugged through the RVDS debugging tool [14]. RealView® Development Suite (RVDS) is a new-generation development tool mainly promoted by ARM after SDT and ADS1.2. Through RVDS, we can easily view and modify the internal registers of the ARM chip and the values in the memory, and we can also write test programs for each peripheral device to debug through RVDS.

When testing other peripheral interfaces, first test the power supply and ground corresponding to the peripheral interface, then test the connectivity of each signal line, and finally download the test program corresponding to the peripheral to the ARM chip through the JTAG interface, and pass the RVDS interface. Debug to test that the peripheral is functioning properly. The following takes serial port circuit debugging as an example to introduce the method of debugging through RVDS. Using the software RVDS, download the program compilation link to the development board to run through the JTAG interface, and found that there are characters displayed on the hyperterminal. The first few characters are correctly displayed, but the characters displayed after 4 or 5 are not, characters entered.

Use an oscilloscope to measure the data on the data line of the UART on the development board. The data sent is sent according to the RS232 protocol. The waveform display is correct, but the display on the HyperTerminal is wrong. It means that the data sent by the development board is correct. The sampling frequency of the PC when receiving is inconsistent with the sending frequency of the development board, which causes this error. After debugging, it was found that the root cause was the inaccurate setting of the main clock frequency of the development board, resulting in the baud rate factor not being the expected 115200. To accurately set the main clock, it is necessary to read the exact frequency of the main crystal oscillator. After modification, the frequency of the main crystal oscillator is 16.365 MHz, and the main clock is configured as 88.192 MHz. After the baud rate is set correctly, run the program, and the result is normal transmission and reception.

4 System Software Design

4.1 System Function Module Design Based on P2P Network

The server and client of the network teaching interactive system based on technology adopt the client server model in management. The teaching resources are classified, sorted and distributed on the central platform and transmitted to end users through the Internet. The central platform provides users with a variety of service functions and integrates various teaching resources. All service functions in the network teaching system are provided by the service center, including online live classroom, courseware download and on-demand, online communication, online examination, etc. The server center platform is the core part of the network teaching system. The backup center dynamically backs up the key data of the service center. In case of data loss of the center platform, the backup center can quickly restore the service capacity of the center platform.

All remote clients need to pass the server authentication and work together under the unified management of the server. Therefore, the server and client adopt the client server model in management. However, in order to prevent all remote clients from obtaining streaming media data from the data server, resulting in the emergence of system bottleneck problems, the point-to-point model is used in streaming media data transmission. Remote clients can obtain streaming media data not only from the data server, but also from other clients. This design can obviously reduce the data load of the server and improve the speed of users obtaining streaming media data.

On this basis, using the technology combined with streaming media, it is divided into two parts: client and server. The client function provides users with basic "system functions", such as user login, user registration, system help and online update. At the same time, it can realize online live classroom, courseware download and on-demand, online homework, online examination, exercise practice, online communication and other functions. The server side includes system management and course management.

First, the online live classroom applies the technology to the streaming media field and breaks the traditional client server mode. Clients can not only obtain data directly from the server, but also connect with each other to obtain streaming media data. Therefore, only some clients in the system need to obtain streaming media data from the server for playback, and the other clients can play through the connection established with each other. In this way, the service can be decentralized, so as to reduce the server load and support a wider range of streaming media release, support large-scale students to listen to classes online, and the investment cost is very low. At the same time, students can put forward questions to teachers online, teachers answer questions on site, correct errors in time and improve the quality of teaching.

Second, courseware download and on-demand. With the advantages of network information sharing, the courseware downloaded by nodes from the server can be shared with other nodes. With the expansion of the network scale, the more nodes, the greater the probability of finding the required courseware, so that the network scale can be expanded infinitely without server bottleneck.

Third, for online homework, the teacher provides some questions or specifies some contents to be placed in the "homework" folder of the local machine, which is set

to be shared when necessary, and learners can complete it on the local machine by downloading. After completion, use technology to send e-mail to teachers to verify students' learning. This is an effective supplement to "online learning" and "discussion", because the discussion is more about staying in the mind, fragmented and broken, not a whole. Therefore, it is necessary to take some discussion questions, of course, not limited to the discussion questions as homework, which should be actually done by students, corrected and counted.

Fourth, online communication, students find teachers to answer questions and solve doubts outside classroom time, or discuss and exchange problems among students. After students log in, they no longer need the support of the server. In this way, after the introduction of technology, compared with the restrictions of the server status on the communication between teachers and students through the chat room and other tools of the server under the mode, the communication of users under the system will not be limited, and will be more perfect.

Fifth, online examination, there are many methods of learning evaluation in the process of network teaching, among which online examination is an effective main means to test learners' learning effect. In network teaching, online examination ensures the authenticity of examination results to the greatest extent by effectively controlling the examination time. Its practice is similar to online homework, but it requires the time for learners to submit their answers.

Sixth, exercise management. When students log in and study, they can choose their own exercises. The exercise library contains the exercises of all online courses, so that students can choose and practice the learning content to the corresponding exercises after learning some courses. The content in the exercise library can be added, modified and deleted according to the change of course content. The research system of this subject takes the basic computer course as the experimental object, so the exercises include two parts, theoretical problems and practical problems. There are multiple-choice questions and fill in the blanks. The actual operation questions are directly taken out from the database, and the questions are provided by the computer test management interface. The management of exercises is limited to teachers who have the right to modify such courses.

Seventh, the specific process of user-on-demand process design based on P2P hybrid technology is as follows:

1) The user logs in to the P2P server;
2) Publish the content of P2P video-on-demand to the service webpage, and after finding the relevant ideological and political course resources required by users, such as Marx's philosophy, Marx's economics and other video resources, the P2P streaming media client program will perform a unique search on the video resources. The identification of the P2P network to distinguish other videos.
3) The on-demand system connects to the resource management server, finds the resource list of the content node through the identifier of the P2P network only, and schedules the content node through the attributes of the content node (such as client ID number, IP address, etc.).
4) After receiving the connection between the content server and the responding node, the video resource is stored by means of buffering through the Socket connection.

4.2 Database Structure Design

The E-R diagram, also known as the entity-relationship diagram, mainly represents the relationship between entities and attributes. Through the E-R diagram, developers can intuitively observe the attributes of each entity. The establishment of E-R diagram helps developers to design the content in the database more simply and clearly, which greatly improves the development efficiency of developers. Combined with the logical design of the database and the E-R diagram, the design of the physical structure of the database is realized, and the geographic name information table Ginfo is mainly designed to store the related information of different geographic names. The geographic name information table Ginfo is shown in Table 1.

Table 1. Geographic name information table Ginfo

Field name	Type of data	Remark
ID	Int	Database sequence is automatically generated
Pinyin	Varchar	Pinyin of geographical names
Text information	Mediumtext	Introduction to the relevant text of geographical names
Image storage path	Varchar	Geographic name image information storage path
Video storage path	Varchar	Geographic name video information storage path
Coding	Varchar	Encoding of geographic names

In the database design stage, the design of the logical structure and physical structure of the database has been completed, and the specific design and development work of the database program is realized in this stage. The system established a MySQL database intelsp, and established the geographic name information table Ginfo in the database intelsp. Next, the database development process is described in detail.

First install MySQL5.5.28 and Navicat Premium software. Navicat Premium is a visual database management tool. After the installation is successful, first establish a connection with the MySQL database. After the connection is successful, you can create a database intelsp in the visual database management tool Navicat Premium, and then create a geographic name in the database. In the information data table Ginfo, enter all the geographic information data on the sand table in the Ginfo table. After the input is successful, you can see the content of the geographic information table Ginfo on the software interface.

The main task of the background server is to wait for the response to the client request. After receiving the client request, it first performs data analysis to determine whether it needs to be retrieved. The data that needs to be retrieved is subjected to a Lucene-based database full-text retrieval. The retrieval results are as follows: On the other hand, it is sent to the bottom embedded sand table controller through WiFi, Bluetooth or serial communication, and the microprocessor on the controller parses the data received by the serial port, so as to control the specific LEDs, light cards and light strips on the sand table; The server-side application program directly plays the multimedia information related

to the retrieval result according to the parsed instruction. The multimedia information includes text, pictures, and videos. Considering that there may be multiple images for a location, the playback rule for images is one every 2 s.

4.3 System Index Function Design

In order to deal with the massive online interactive teaching resource set and interactive search problem, this study uses domain index method to reformulate online interactive teaching resource set by borrowing domain.

Definition 1. Domain: The combination of attributes of a data set is called a domain. Use D to describe the online interactive teaching resources. If Ω represents the complete set of field values, then:

$$D = \{x | x \in \Omega\} \tag{1}$$

The resource set S reformulated by the domain is described by the following formula:

$$S = \{D_1, D_2, \cdots, D_n\} \tag{2}$$

Definition 2. Domain correlation degree: For domain Q, I, the correlation degree of domain can be expressed as:

$$t(Q, I) = |Q \cap I|/|Q| \tag{3}$$

where $|\cdot|$ stands for the basis of the set. Generally, Q represents the query domain, I represents the index domain, and the correlation degree of the domain is $t(Q, I) \in [0, 1]$. The larger its value, the better the link between the domains.

Definition 3. Domain search: according to the proposed threshold value $t^* \in [0, 1]$ of domain Q, domain set I and correlation degree, the process of searching the correlation degree beyond t^* from domain set I is described as domain search, and its formalization can be expressed as:

$$X : t(Q, X) \geq t^*, X \in I \tag{4}$$

Definition 4. Domain index: An index consisting of hash values of domain I is a domain index. Generally speaking, the signature vector will be divided into b-type partitions, and there will be r rows in all partitions, so the correlation between the probability of becoming a pre-selected domain and the Haccard phase velocity s can be described as follows:

$$P(s|b, r) = 1 - \left(1 - s^r\right)^b \tag{5}$$

As for the asymmetry of pre-correlation degree, this paper uses the mutual conversion between domain correlation degree and Jaccard similarity degree s to solve the problem, and the correlation is shown in Formula (6) and (7).

$$\hat{s}_{x,q}(t) = t/(x/q + 1 - t) \tag{6}$$

$$\hat{t}_{x,q}(s) = (x/q + 1)s/(s + 1) \tag{7}$$

where, $x = |X|$, $q = |Q|$ and X, $Q \subset D$ represent the bases of fields X and Q respectively.

To sum up, on the basis of designing system function modules and database structure based on P2P network, the index function of the system is designed and the system software environment is completed.

5 Experimental Comparative Analysis

To verify the effectiveness of the online interactive teaching system of Sanda Course Based on P2P network, the following experiments are designed. In order to avoid the singleness of the experimental results, the traditional teaching system is compared with the system in this paper.

5.1 Comparison of Interactive Response Time

The response time comparison results between the system in this paper and the traditional system are shown in Fig. 3.

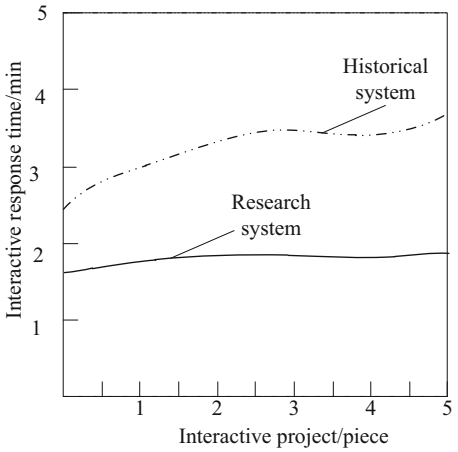

Fig. 3. Interactive response time comparison

According to Fig. 3, compared with the historical system, the response time of the system in this paper is less in each operation, and the interactive response time is always below 2 min, indicating that the system has a strong timeliness.

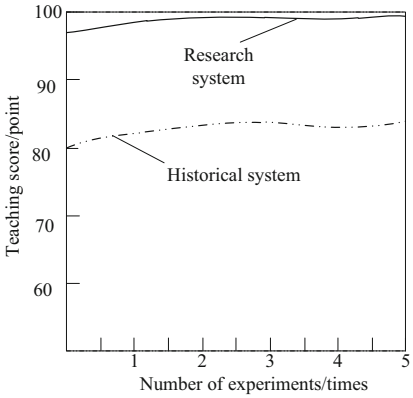

Fig. 4. Comparison of teaching achievements

5.2 Comparison of Teaching Performance

After applying the two systems, the comparison results of students' scores in the school are shown in Fig. 4.

Through the analysis of the results shown in Fig. 4, it can be seen that after the application of the traditional system, the teaching score fluctuates between 80 and 85 points. However, after the application of this system, the student's score is higher, and always keeps above 97 points. It shows that the system can obviously improve the teaching effect. This is because the system in this paper improves the efficiency of interaction in the online teaching process, and the information obtained is more accurate, thus improving the teaching effect.

5.3 Content Search Accuracy Comparison

Two systems are used to find the content in the system respectively, and the accuracy comparison results of content search are shown in Fig. 5.

By analyzing the results shown in Fig. 5, it can be found that compared with the traditional teaching system, the system in this paper has a higher accuracy in searching for teaching resources and interactive teaching content, and its accuracy rate is always above 95%, thus fully proving the reliability of the system in this paper. This is because the system in this paper solves the traditional mode of server is easy to become the system bottleneck problem, is the system has high flexibility and scalability.

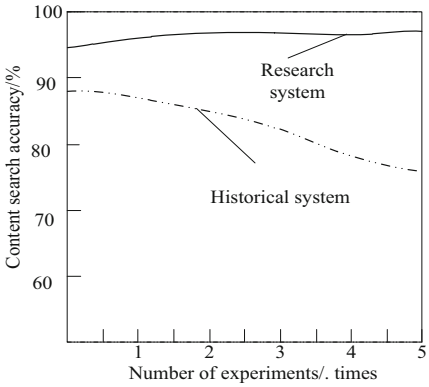

Fig. 5. Content search accuracy comparison

6 Conclusion

The innovation of this paper is the application of P2P technology in the construction of network teaching system, which can well solve the problems of network teaching resource sharing and user interaction, improve the interaction, real-time and personalized, reduce the burden of the server. At the same time, this paper also studies and analyzes the technical theories related to streaming media, and designs and implements a low-cost powerful network teaching interactive system.

The research work of this paper is summarized as follows:

(1) This paper studies the principle of P2P network related technology, analyzes the advantages and disadvantages of the technology in detail, and expounds the P2P network structure and application field of the technology;
(2) The network structure and logical structure of the system are constructed, which not only solves the problem that the server is easy to become the system bottleneck in the traditional mode, but also has strong flexibility, fault tolerance and expansibility.

The verification shows that after the system is put into practical application, the interactive response time of the system is shorter, the content search accuracy is higher, and the teaching performance is significantly improved, indicating that the system has a high application advantage.

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