An Automatic Control Algorithm for Sampling and Timing of Civil Radar Signal Based on DSP

Juan Li[1(✉)] and Lingling Cui[2]

[1] College of Intelligent Equipment and Automotive Engineering, Wuxi Vocational Institute of Commerce, Wuxi 214153, China
343384882@qq.com

[2] Department of Physical and Health Education, Wuxi Vocational Institute of Commerce, Wuxi 214153, China

Abstract. Aiming at the problem of fixed period sampling control of radar signal and event triggered variable period sampling control, there are few research results at present, so a DSP based automatic control algorithm for civil radar signal sampling timing is designed. Using orthogonal intermittent sampling to implement sampling modulation on radar signals, combined with improved UNet3+network and sequence data recognition method, the modulation signal recognition is completed. Based on the recognition results, a DSP processor is designed with TTA technology as the core, integrating phase-locked loop synchronization and timing sampling technology to achieve automatic control of the signal synchronization sampling process. The test results show that the time control error of the algorithm is low, the control performance is good, and the control stability is higher than 95%. With the extension of the sampling period, the control stability does not show a downward trend.

Keywords: DSP Processor · Orthogonal Intermittent Sampling · Civil Radar · Signal Sampling Control

1 Introduction

After World War I, due to the potential threat of the Nazi German Air Force, the first batch of radars developed in the 1930s. During the Second World War, pulse delay system has been used to create moving target detection (MTD) radar. With the increase of oscillator stability, it has developed into full pulse Doppler radar. In addition to detecting moving targets, it can also measure target speed. In the period after the Second World War, the theory of radar system made a lot of progress, but the hardware limited the method of pulse Doppler. With the development of very large scale integrated circuits (VLSI) in the 1970s, the application of digital technology and computers is more extensive and in-depth, and the rise of pulse Doppler radar, the synthetic aperture technology can obtain high-resolution radar images similar to visible light imaging under the weather conditions with extremely low visibility. Since the Second World War, radar technology has become

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increasingly popular and its performance has become increasingly perfect. Therefore, radar has been widely used in military, such as early warning, search, surveillance radar, fire control radar, and guidance radar; Civil use, such as weather radar, control radar, remote sensing equipment, etc.

In the field of civil radar application, radar is widely used in a variety of occasions, such as unmanned monitoring for motion parameter detection and inching parameter detection of indoor human targets to achieve smart home care; It is used for intelligent driving, and can assist in reverse parking, intelligent obstacle avoidance, detection and positioning of pedestrians and vehicles [1]. In the application of civil radar, signal sampling control has always been a key research problem.

In recent decades, due to the rapid development of digital technology and computer technology, more and more digital components have been used in the process of control systems, and analog controllers have also been replaced by computer digital controllers. In order to better adapt to the changes brought about by computers and digital components, scholars have proposed the sampling control theory. With the development of sampling control theory, fixed period sampling control method and variable period sampling control method have attracted extensive attention of many scholars.

The fixed period sampling control method is to sample at a fixed time interval, and use the components with signal holding function to keep the last sampling time information during the non sampling period, so as to control the system using the sampling information. Compared with the traditional continuous controller, the fixed period sampling control has the characteristics of saving transmission resources, saving computing resources, and strong applicability. At the same time, it is also easy to apply in the actual computer digital control process. In practical applications, sampling control has also been widely used, such as the actual paper industry, high-precision electric simulation turntable system, networked traction control system, etc. [2]. The fixed period sampling control method has become a hot research direction in the control field. Compared with the fixed period sampling control method, the variable period sampling control method collects the data of the system by changing the sampling period, and uses the sampling data to design the relevant variable period sampling controller control system. The more common method is the event trigger control method. Its main idea is to set the event trigger mechanism. When the event trigger mechanism is satisfied, it needs to sample the relevant information of the system. If the trigger mechanism is not satisfied, it uses a signal holding component to keep the sampling information unchanged until the next trigger time. Therefore, only when the conditional trigger mechanism is met, the system information needs to be sampled. Based on the above analysis, due to the rapid development of digital technology and computer technology, the fixed period sampling control method and variable period sampling control method are two key and hot research topics in the current control field, and some representative research results have been achieved. However, the achievements of fixed period sampling control and event triggered variable period sampling control in the field of fuzzy adaptive control are relatively few, and no systematic theoretical achievements have been formed.

For this reason, the automatic control problem of fixed period sampling of civil radar signal is studied, and some achievements have been made in the research of this problem. Some scholars have proposed a FPGA based method of rotor vibration signal full cycle equal phase sampling control. This method uses the Keyphasor Frequency Multiplier signal as the trigger signal of A/D conversion. The Keyphasor Frequency Multiplier circuit is implemented by the internal logic device of FPGA chip, and the periodic linear interpolation prediction module is added to the circuit to improve the accuracy of Keyphasor Frequency Multiplier. The research results show that the key phase frequency multiplication circuit designed by this method can achieve the predetermined function, and has the advantages of high integration, wide frequency multiplication range, etc. It can be widely used in the full cycle equal phase sampling control of rotor vibration signals. Some scholars proposed that the accuracy of data acquisition system should include the accuracy of sampling signal amplitude and the accuracy of sampling control timing. A design scheme of trigger timing sampling control in data acquisition system was given, which realized a comprehensive program control of multi trigger mode and solved the problem of precise synchronous trigger timing sampling control. Although both methods mentioned above can achieve automatic control of sampling timing, there is a problem of significant time control error. Therefore, a DSP based automatic control algorithm for sampling and timing of civil radar signals is designed to improve the accuracy of automatic control for sampling and timing of civil radar signals. Using orthogonal intermittent sampling to implement sampling modulation on the radar signal, the orthogonal intermittent sampling modulated radar signal is obtained. Improve the UNet3+network to balance recognition accuracy and training time, solve the problem of low recognition accuracy in complex electromagnetic environments, and achieve recognition of sampled modulation signals. Based on the results, a phase-locked loop synchronous sampling control circuit is designed using DSP as the core processor, combined with phase-locked loop synchronization and timing sampling technology, to achieve automatic control of the signal synchronous sampling process.

2 Design of Automatic Control Algorithm for Sampling and Timing of Civil Radar Signal

2.1 Signal Sampling and Modulation

The radar signal is sampled and modulated by quadrature intermittent sampling, and the quadrature intermittent sampling modulated radar signal is obtained.

Civil radar signal is composed of M The frequency of each sub pulse can be expressed as:

$$\begin{cases} \mathrm{l}_m = l_0 + m\Delta l \\ m = 0, 1, 2, \ldots, M - 1 \end{cases} \tag{1}$$

In formula (1) m Indicates the sub pulse serial number; l_m Indicates the frequency of each sub pulse; l_0 Represents the starting frequency; Δl Indicates the frequency interval between adjacent sub pulses [3].

According to the above assumptions, the radar signal can be expressed as:

$$y(r) = \sum_{m=0}^{M-1} rect\left(\frac{r}{\alpha}\right) \exp(k2\pi \mathrm{l}_m r) \tag{2}$$

In formula (2)r Represents a fast time variable; α Indicates the pulse width; k Represents the interval parameter.

among r Meet the following formula:

$$-\frac{R}{2} \leq r \leq \frac{R}{2} \tag{3}$$

In formula (3), R is a real number.

The schematic diagram of civil radar signal is shown in Fig. 1.

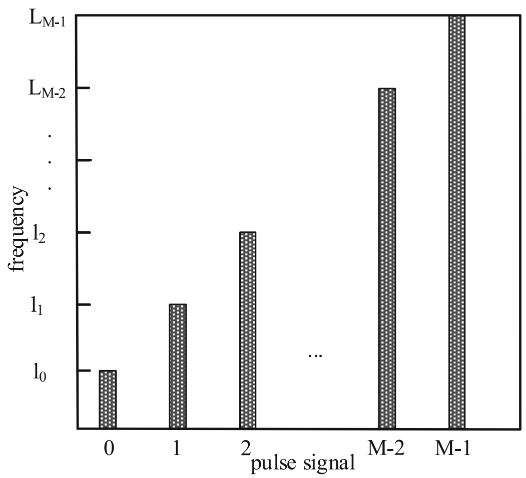

Fig. 1. Schematic diagram of civil radar signal

To ensure the orthogonality between subpulses, according to the characteristics of sin c (□) function, the frequency interval between subpulses of radar signal Δl The following formula should be met:

$$\Delta l = \frac{b}{\alpha} \tag{4}$$

In formula (4)b It is a positive integer.

In particular, it can make $\Delta l = \frac{1}{\alpha}$.

The equivalent bandwidth of civil radar signal can be expressed as:

$$C = M \Delta l \tag{5}$$

Therefore, it uses multiple narrow band sub pulses to achieve equivalent large bandwidth and can be used as radar imaging signal [4]. For civil radar, FFT and other signal processing methods based on Fourier transform are often used for imaging processing, and the corresponding range resolution is:

$$\Delta U = \frac{d}{2C} \tag{6}$$

In formula (6) d Is the transmission rate of electromagnetic wave.

The non blurring distance is:

$$\Delta u = \left[-\frac{d}{4\Delta l}, \frac{d}{4\Delta l} \right] \tag{7}$$

The model of quadrature coded intermittent sampling modulating civil radar signal is shown in Fig. 2.

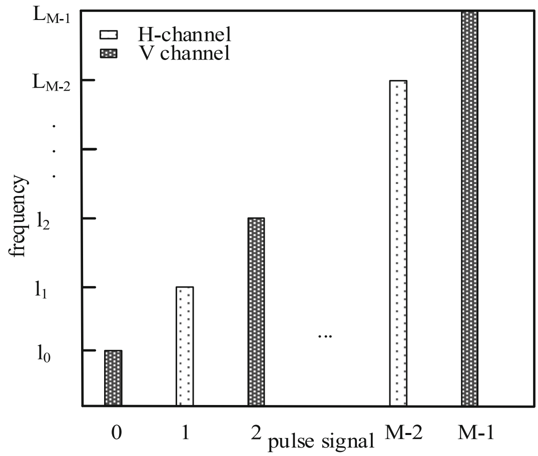

Fig. 2. Schematic diagram of quadrature coded intermittent sampling modulated radar signal

For H channel and V channel, randomly select one of them from the complete civil radar signal $\frac{M}{2}$ It is composed of mutually orthogonal sub pulses. The sub signal frequencies of the two orthogonal polarization channels can be expressed as:

$$l_{Hm} = l_0 + F_H(m)\Delta l \tag{8}$$

$$l_{Vm} = l_0 + F_V(m)\Delta l \tag{9}$$

In formula (4)F_H, F_V Is the orthogonal subset of the integer set [0: M □ 1], where the number of elements of each is $\frac{M}{2}$ [5].

Quadrature coded intermittent sampling modulated civil radar signal can be expressed as:

$$y_H(r) = \sum_{m=0}^{M/2-1} rect\left(\frac{r}{\alpha}\right) \exp(k2\pi l_{Hm} r) \tag{10}$$

$$y_V(r) = \sum_{m=0}^{M/2-1} rect\left(\frac{r}{\alpha}\right) \exp(k2\pi l_{Vm} r) \tag{11}$$

Due to the orthogonality between subpulses of civil radar signals, the same polarization component and cross polarization component of the quadrature coded intermittent sampling modulation signal can be transformed by Fourier transform of the received echo signal and l_{Hm}, l_{Vm} Index is detached.

2.2 Identification of Sampled Modulation Signal

The recognition method based on sequence data is used to realize the recognition of sampled modulation signals. Compared with the method of processing time-frequency images, sequence data generally does not need various complex transformations, and the amount of calculation is relatively small, which can largely retain the information of the original data, and can be suitable for processing large amounts of data. UNet3+network is introduced and improved to give consideration to both recognition accuracy and training time, so as to solve the problem of low recognition accuracy in complex electromagnetic environment.

Recognition of radar signals based on deep learning, the better the features extracted, the better the recognition ability of neural networks [6]. UNet3+network integrates shallow features and deep features, and better describes signal features by complementing each other to avoid the loss of key information, so that the network can judge through more features and has better recognition ability. Although the UNet3+network has a strong ability to extract features, it also has some limitations: the unimproved UNet3+network has five levels, and every additional network level requires more feature fusion, resulting in an overly complex model structure, requiring more operations, and reducing the training speed of the network.

Aiming at the problems of the above UNet3+network, an improved UNet3+network model [7] is proposed on the basis of the original network. There are two main improvements: first, in order to improve the training speed of the network, the hierarchy of the network is deleted, as shown in the following formula:

$$f = 5 - 2 = 3 \tag{12}$$

On the premise of avoiding the decline of network recognition accuracy, reduce redundant fusion and reduce the amount of computation.

The second is the introduction of attention mechanism. Although UNet3+network has the ability to extract detailed data features, not all the extracted features are helpful to judge the recognition signal. Some features are invalid features. The attention mechanism will invalidate the redundant features, so that the network can focus on key features, highlight the impact of key features, and improve network performance.

The improved UNet3+network structure includes convolutional pooling layer module, feature fusion module, attention layer and other layers. In the convolution pooling layer module, there are three one-dimensional convolution pooling layers with the same parameters. The feature is extracted through 32 convolution cores with a length of 5. The three convolution pooling layers are followed by regularization layers with coefficients of 0.2, 0.1, and 0.1 to prevent over fitting. Then through convolution layers 4, 5 and 6, 8 convolution kernels with length of 5 are used for convolution operations. In the feature fusion module is the feature fusion of full scale skip connection, where convolution layers 7 and 8 are convolutional operations through 8 convolution kernels with length of 7, and convolution pooling layer 9 is convolutional operations through 8 convolution kernels with length of 7. All the maximum pooled layers in the model have a size of 2. Finally, the regularized layer is followed by the tiling layer and the full connection layer to output the final result [8] (Tables 1 and 2)

Table 1. Module Structure of Convolution Pooling Layer

S/N	Hierarchy	Input	Output
1	Convolution pooling layer 1	(None, 1024, 1)	(None, 512, 32)
2	Regularization layer 1	(None, 512, 32)	(None, 512, 32)
3	Convolution pooling layer 2	(None, 512, 32)	(None, 256, 32)
4	Regularization layer 2	(None, 256, 32)	(None, 256, 32)
5	Convolution pooling layer 3	(None, 256, 32)	(None, 128, 32)
6	Regularization layer 3	Input: (None, 128, 32)	Output: (None, 128, 32)

Table 2. Structure of feature fusion module

S/N	Hierarchy	Input	Output
1	Feature fusion layer 1	Input 1: (None, 512,8) Input 2: (None, 256, 8) Input 3: (None, 128,8)	(None, 896, 8)
2	Feature fusion layer 2	Input 1: (None, 512, 8) Input 2: (None, 128, 8) Input 3: (None, 896, 8)	(None, 1536, 8)

The input of attention layer is (None, 1536, 8), and the output is (None, 1536, 8).

The structure of other levels is shown in Table 3.

The training process of the model is as follows:

Step 1 Data input

Input radiation source data and corresponding labels into the network model.

Step 2 Sample pretreatment

Min Max normalization is performed on the sample set, and the sample value obtained will be limited to [0, 1].

Step 3 Convert Label

The labels of the eight types of signals are converted into unique hot codes, which are represented as binary vectors.

Step 4 Build a training dataset

In order to strengthen the generalization ability of the model, random seeds were used to disrupt eight types of signal samples, and the samples were divided into training sets, verification sets, and test sets at a ratio of 0.47:0.23:0.30;

Table 3. Structure of other levels

S/N	Hierarchy	Input	Output
1	Convolution layer 4	(None, 512, 32)	(None, 512, 8)
2	Convolution layer 5	(None, 256, 32)	(None, 256, 8)
3	Convolution layer 6	(None, 128, 32)	(None, 128, 8)
4	Convolution layer 7	(None, 896, 8)	(None, 896, 8)
5	BN floor 1	(None, 896, 8)	(None, 896, 8)
6	Convolution layer 8	(None, 896, 8)	(None, 896, 8)
7	Convolution pooling layer 9	(None, 1536, 8)	(None, 1536, 8)
8	BN floor 2	(None, 1536, 8)	(None, 1536, 8)
9	Regularization layer 4	(None, 1536, 8)	(None, 1536, 8)
10	Tile	(None, 1536, 8)	(None, 12288)
11	Full connection layer	(None, 12288)	(None, 8)

Step 5 Set the early stop mechanism

In network training, when the loss of a round of verification set is greater than the loss m of the previous round of verification set, and all losses after four more rounds of training are greater than m, the network training is ended;

Step 6 Compile the network

Adam is used as the network optimizer, and category is used_Crossentropy function calculates the loss;

Step 7 Add a learning rate dynamic adjustment mechanism

The learning rate is initially set to 0.0001. During network training, when the loss of verification set increases, the learning rate of this round is multiplied by 0.5 as the learning rate of the next round of training. The minimum learning rate is not less than 0.0000125;

Step 8 Classified network training

Set the number of samples selected for each batch of training to 512 and the maximum number of training rounds to 50 for training.

2.3 Sampling Timing Automatic Control

According to the result recognition, a PLL synchronous sampling control circuit is designed with DSP as the core processor, combined with PLL synchronization and timing sampling technology, to realize the automatic control of signal synchronous sampling process.

Based on TTA technology, a DSP processor is designed, which is composed of Internet and processing unit.

The Internet provides a channel for each unit in the processor to exchange data. It includes two basic modules: Socket and bus. In addition to providing data exchange function, the bus is also used to transmit control signals, such as source and target register

IDs, function unit latch signals, etc. Socket provides the connection between function unit and register file and bus. Each socket can be connected to one or more buses and one or more registers [9] of a function unit. The input socket transfers the data from the bus to the function unit and register file, and the result socket places the data from the function unit and register file on the bus. The input socket is further divided into a trigger socket and an operand socket. The only difference between them is that the trigger socket transmits data at the same time, and the operation code is also passed into the functional unit to specify the type of operation. The source address field and destination address field are transferred from the control bus to all connection points. A three input socket and two output socket interconnection network is designed, as shown in Fig. 3.

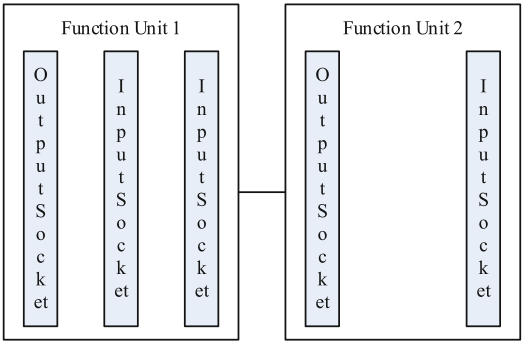

Fig. 3. Interconnection network structure design

The programming method of TTA is to specify some required data values to flow in TN. Therefore, this architecture has only one operation mode: moving from one FU to another. In general, FU is connected to TN through three different types of registers: Operand, Trigger and Result. All transfers are from register to register.

The functions of the three registers are shown in Table 4.

The function unit can be pipelined internally. In the first stage, the operand register (O) and trigger register (T) temporarily store data from the input socket. Because the data of the operand socket can be temporarily stored through the operand register, the data can be written to the operand socket in advance. When the data is transferred to the trigger socket, the operation begins. In the first stage, a register contains an operation code, which controls which operation the functional unit performs. The operation code is encoded in the target ID used to indicate that the functional unit triggers the socket. Each pipeline segment of the functional unit contains a combination logic and pipeline register. All pipeline segments of the functional unit are synchronized with the instruction stream specified by the compiler. Every time an instruction flows out, the pipeline of the functional unit will advance one step [10].

In TTA structure, FU and data transmission network are completely separate, and the pipeline of transmission network and FU is also completely independent. Optimizing FU structure means maximizing the pipeline of FU. There will be a unique instruction prefetching unit, a unique Guard unit (responsible for instruction coding and conditional execution), and a unique Valid unit (used to obtain the value in the result register of the

Table 4. Functions of three registers

S/N	Register	Function
1	Operand	The operation mode is the same as GPR except that the corresponding FU of this operand register is different after being triggered
2	Trigger	The transmission written to the trigger register can cause the operation of the corresponding FU. The transmitted value is used as the operand of this operation. If more operands are needed, they can be extracted from other operand registers. In order to perform different operations on the same FU, different address contents of trigger register can be accessed
3	Result	Most FUs are pipelined, so operations can be started once per clock cycle. When the result of one operation leaves the pipeline, it will be written to the result register of FU. Starting from this result register, it can be written to other FUs in the next cycle through TN

FU unit) in the FU. The pipelining is realized in the following way: Hybrid pipeline: It is implemented in the TTA system structure in the way of Hybrid pipeline. In this pipeline mode, lower level pipelines can perform operations in advance if they do not affect the final result, which is equivalent to the multi-function in the pipeline. Hybrid pipeline allows maximum program scheduling freedom. The only limitation is the fixed length of pipeline and the fixed speed of each stage. Data can be read in or read out at any time. Of course, some causality must be considered. For example, when no data is read into the operation register, it is wrong to read the data in the result register.

The use of Guard in the TTA structure makes conditional execution possible. The execution of each MOVE instruction is conditional. Thus, each MOVE instruction includes the Guard selection bit. The MOVE instruction encoding method is related to the setting of the guard unit parameters SINGLEGUARD, PARMOVES, GUARDSPECSIZE. The function of SINGLEGUARD indicates that if SINGLEGUARD is defined, an instruction corresponds to a guard. If SINGLEGUARD is not defined, a MOVE includes a guard. As shown in Fig. 4 and Fig. 5.

In the TTA architecture, the functional unit is the main body that performs data operations. The function unit obtains data from the input socket, and places the result on the result socket after the operation is completed.

The PLL synchronous sampling control circuit consists of five parts: DSP processor, second-order active low-pass filter circuit, voltage zero crossing comparison circuit, PLL and frequency division circuit.

The structure of the circuit is shown in Fig. 6.

The cut-off frequency of the second-order active low-pass filter circuit is Wuqi, which is responsible for filtering out the second and above second harmonics to obtain pure fundamental signal. The voltage zero crossing comparison circuit is responsible for converting the fundamental sinusoidal signal obtained by the second-order low-pass filter into a square wave signal and outputting it to the back-end phase-locked loop and frequency division circuit for fundamental frequency multiplication. The obtained frequency multiplication signal is the control signal of the sampling period [11].

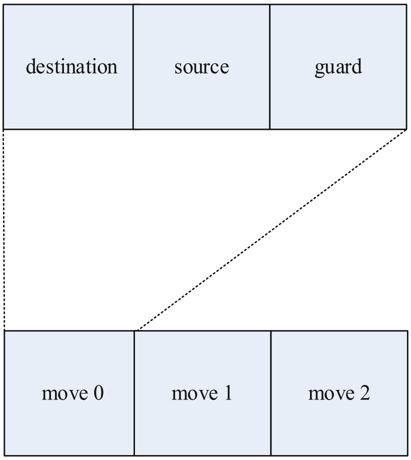

Fig. 4. Undefined instruction format of SINGLEGUARD

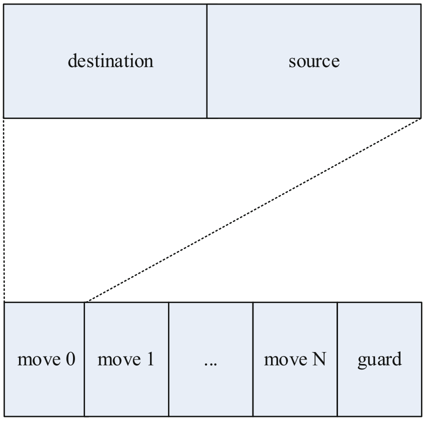

Fig. 5. Command format defined by SINGLEGUARD

The PLL frequency multiplication output frequency is 12800 Hz, and the control of system sampling is staggered, that is, 128 out of 256 samples are radar signals, and the other 128 are analog ground signals collected for zero calibration. The main chips used in the synchronous sampling control circuit of PLL include CD4046 and CD4020.

3 Case Test

3.1 Experimental Process

Relevant parameters of civil radar signals are shown in Table 5.

The design algorithm is used to automatically control the sampling and timing of the experimental civil radar signal. Firstly, the quadrature intermittent sampling is used to

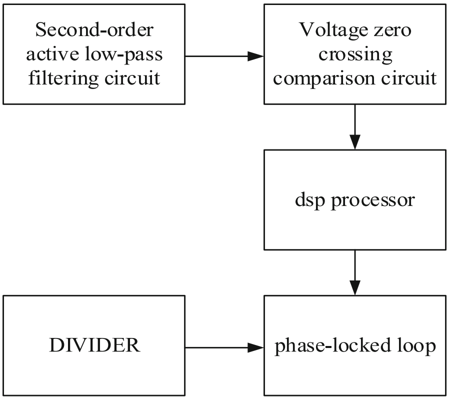

Fig. 6. Structure design of the circuit

Table 5. Relevant Parameters of Experimental Civil Radar Signal

S/N	Parameter	Parameter value	Company
1	Signal carrier frequency	30	GHz
2	Signal pulse width	45	μs
3	Signal bandwidth	8	MHz
4	Target speed	22	m/s
5	Pulse repetition period	550	μs
6	Signal IF	80	MHz
7	Sampling rate	40	MHz
8	Target slant distance	22	km

sample and modulate the radar signal of the experimental civil radar, and the quadrature intermittent sampling modulated radar signal is obtained, as shown in Fig. 7.

Then the recognition method based on sequence data is used to realize the recognition of sampled modulation signals. In recognition, the improved UNet3+network is trained first, and the training results are shown in Fig. 8 and Fig. 9.

It can be seen from the above figure that the improved UNet3+network model converges faster.

At last, the automatic control of signal synchronous sampling process is realized by PLL synchronous sampling control circuit. The time control error and control stability of the design algorithm are tested respectively. In the testing, two traditional methods, the FPGA based rotor vibration signal full cycle equal phase sampling control method and the trigger timing sampling control method in the data acquisition system, will be used as comparative testing methods, and represented by Method 1 and Method 2 respectively.

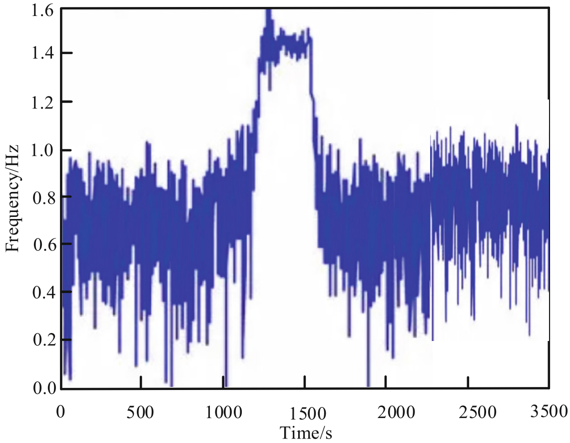

Fig. 7. Quadrature Intermittent Sampling Modulated Radar Signal Obtained

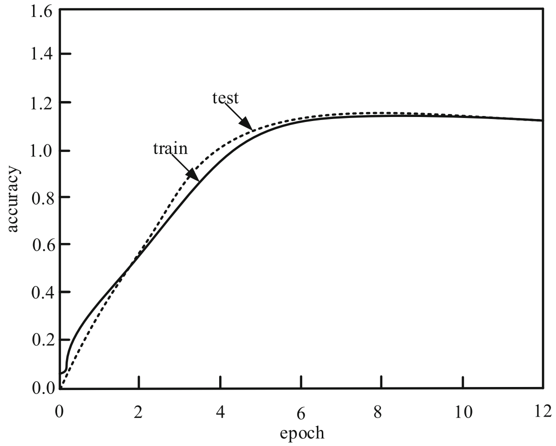

Fig. 8. Accuracy Curve

3.2 Test Results of Time Control Error

The time control error test results of test design algorithm and method 1 and method 2 under different sampling periods are shown in Table 6.

The test results in the above table show that the time control errors of the three methods are rising with the extension of the sampling period. The time control error of the design algorithm is below 2.54 ms, which is generally lower than the time control error of Method 1 and Method 2, which shows that the automatic control performance of the design algorithm is stronger.

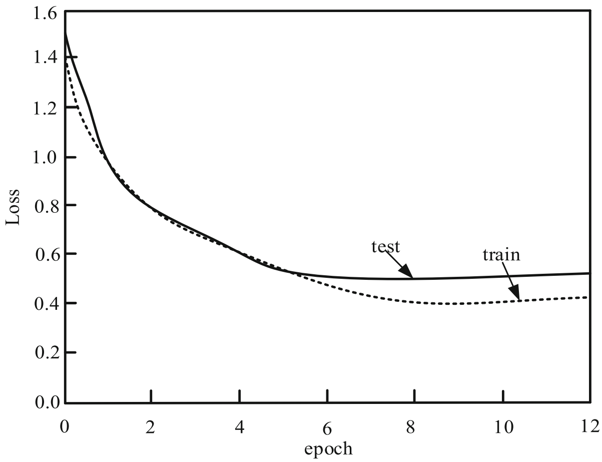

Fig. 9. Loss Curve

Table 6. Test Results of Time Control Error

Sampling period (s)	Time control error (ms)		
	Design algorithm	Method 1	Method 2
50	1.36	5.63	8.36
60	1.58	5.98	8.49
70	1.69	6.24	8.64
80	1.84	6.48	8.82
90	1.90	6.75	8.91
100	2.08	6.89	9.05
110	2.28	7.05	9.46
120	2.32	7.21	9.82
130	2.39	7.49	9.90
140	2.41	7.59	10.08
150	2.54	7.85	10.20

3.3 Control Stability Test Results

Then test the control stability of the design algorithm and method 1 and method 2 in different sampling periods. The test results are shown in Table 7.

According to the test results in the table above, the overall control stability of the design algorithm is far higher than that of Method 1 and Method 2. At the same time, with the extension of the sampling period, the control stability of Method 1 and Method 2 shows a downward trend, while the control stability of the design algorithm does not show a downward trend, which has been higher than 95%.

Table 7. Control Stability Test Results

Sampling period (s)	Control stability (%)		
	Design algorithm	Method 1	Method 2
50	95.634	86.326	82.963
60	95.874	86.302	82.908
70	95.125	86.268	82.900
80	95.365	86.228	82.586
90	95.025	86.086	82.521
100	95.985	86.005	82.498
110	95.652	85.058	82.432
120	95.458	83.219	82.405
130	95.365	83.208	81.352
140	95.158	83.196	81.304
150	95.365	83.187	81.210

4 Conclusion

An automatic control algorithm for sampling and timing of civil radar signals based on DSP has been designed, and some scientific achievements have been made. The experimental results show that the time control error of this algorithm is below 2.54 ms, and the control stability is above 95%. However, according to many other hot issues in this field, the author believes that there are still many aspects to be further studied, such as how to save resources and ensure the control effect of the periodic sampling controller, and the need for further application of the design algorithm.

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