# Area Efficient and Ultra Low Power Full Adder Design Based on GDI Technique for Computing Systems

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**Abstract.** The relevance of ultra-low-voltage (ULV) operation for attaining minimal energy usage has increased recently. The fundamental building element of computational arithmetic in many computer and signal/image processing applications is the full adder. An innovative 1-bit hybrid adder circuit that uses both multi-threshold voltage (MVT) transistor logic and GDI (gate-diffusion input) logic is disclosed. The suggested motivation of the Multi Threshold Voltage-gate-diffusion input hybrid adder design is to furnish low energy efficient utilization with a small footprint. Standard 45 nano-meter CMOS process technology is used to simulate the suggested hybrid architecture with a ULV of 0.2 V. The suggested design made considerable improvements in contrast to the previous published designs, yielding >57% and 92% reductions Using only 14 transistors in the Energy and Delay Product respectively, according to the post-layout simulation findings. The suggested design technique produces full functionality, which shows resistance against the processes of global, local variations. The suggested design offers >57% energy efficient compared to the current efforts, according to energy measures that are adjusted for 32 and 22 nm technologies.

**Keywords:** MVT · GDI · ULV · TGA · TFA · Energy Delay Product

## 1 Introduction

There are numerous applications needing fast speed, compact space, and low power consumption due to technological improvements and the rise in the usage of portable communication systems including computers, smart phones, Internet of Things (IoT) devices, i-Pads and others. Therefore, low-energy circuits are required for the creation of components of systems and processors with specialized use [1]. The implementation of digital systems is a demanding area of interest for circuit design experts due to this need. Operating digital circuits at ULV, or at close to or below the transistor's One of the most efficient strategies to decrease energy consumption is to use threshold voltage [2].


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The most prevalent and often utilized arithmetic operations in various DSP systems and very large-scale integration (VLSI) are further, subtraction, multiplication, and accumulation. High-performance DSPs and application-specific processors were made possible by when algorithms with standards such as correlation-convolution-digital filtering are executed; these arithmetic operations are effectively used [3]. The one bit complete full adder cell serves as the fundamental implementing element for carrying out these arithmetic operations. Therefore, improving the entire adder cell's performance is crucial for improving the performance of the system/architecture as a whole. Numerous complete adder ideas using various logic and technological philosophies have been documented in the literature. While other systems employ numerous logic styles, some are built on a single logic style (hybrid designs). Each complete adder design has a similar functionality, but they all have advantages and drawbacks in terms of performance variables including size, speed, and power usage.

The most common method is the full adder architecture for static C-CMOS complementary metal-oxide semiconductors [4]. The 28 transistor architecture resembles a typical N-MOS and P-MOS PU and PD transistors in a CMOS framework. This structure's key benefit is that it is resistant to transistor size and supply voltage scaling. Additionally, it has complete swing logic, which is necessary for constructing intricate structures. Due to the huge PMOS transistors used in this configuration, it has a high input capacitance and takes up more space. Regarding power use and transistor count, mirror adders are among the clever designs that resemble static CMOS full adders, although they have shorter carry propagation latency than CCMOS [5].

Another common design using 32 transistors is the entire adder using CPL logic [6–9]. CMOS does not use supply lines, rather, pass transistor source in PTL is coupled to certain input signals. Although this adder logic's numerous intermediary switching nodes provide efficient voltage swing restoration and higher transistor count make it an unsuitable option for low power applications. Transmission gate logic complete adders are suggested as a solution to the pass transistor logic problem with voltage deterioration [10]. Alioto and associates suggested Shams et al. [11] provided the Transmission Gate Adder (TGA), which employs twenty transistors, in contrast to the Transmission Function Adder - (TFA), which uses sixteen transistors. The transmission function theory and transmission gates serve as the foundation for these adders. The parallel coupling of NMOS and PMOS pass transistors creates the transmission gate structure. The major benefit of its low power efficient is strength of its transmission gate logic arrangement, however due to its weak driving capabilities, Due to cascading of either TFA or TGA; this logic is not advised to creating complicated systems.

To decrease the area, latency, and power, since then, there have been a number of hybrid full adder works described [12–14] a hybrid adder with 14 transistors (14T) was presented by Vesterbacka [15]; however it had pass logic transistors with no complete swing. In Hung et al. [16], another comparable hybrid adder with only 10 transistors was presented. Poor driving capabilities affect both the 14T and 10T adders, which have 10 transistors each [17], suggested a HPSC. It concurrently generates the XOR and XNOR functions using a six transistor pass logic network. Full swing logic is produced by the HPSC full adder, albeit at the expense of additional latency and transistor use. The majority-based adder is another adder that employs hybrid logic [18]. It requires

capacitors and static inverters to produce the superior of capabilities because of less number of transistors. Complete adder with 24 transistors (24T) based on a 3-input XOR architecture provided by Tung et al. [19] also employs two distinct types of logic: pass transistor and CMOS. Goel et al. [20] suggested The FA-Hybrid, a different CPL-based hybrid full adder, which employs an unique XOR/XNOR architecture utilizing cross-coupled PMOS transistors with NMOS transistors increase speed. It offers superior driving capabilities but consumes more power when the output, static CMOS inverters are employed.

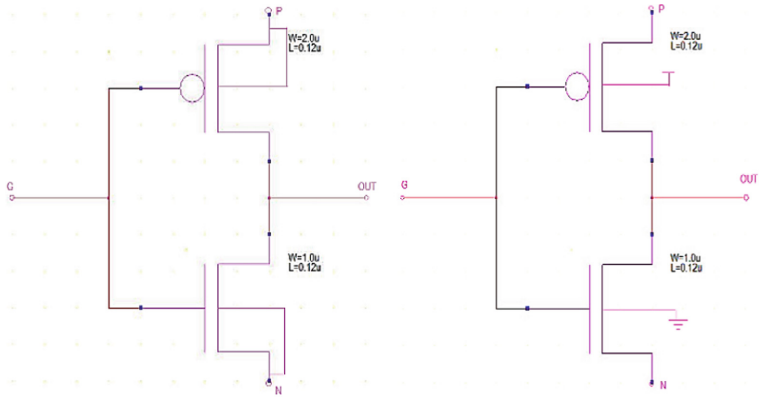


**Fig. 1.** a). Originally Proposed, b). CMOS Compatible

DP Logic Full Adder (DPTL-FA) and Swing Restored PT Logic Full Adder (SRPL-FA) are two hybrid designs that Aguirre et al. [21] suggested (DPL-FA). For more energy-efficient computing, these complete adders were created employing ground-less/powerless pass transistors. In contrast to DPL-FA, which uses complementary transistors, SRPL-FA uses PMOS restoration transistors to achieve full swing logic. Bhattacharyya et al. [22] suggested another hybrid 16T full adder (16T Hybrid). Weak inverters in the sum generating module and robust carry module which consists of TG gates were used in this complete adder design to lower the PDP. Full swing outputs are provided by Gate-diffusion-input based OR, AND and XOR gates in a different full adder architecture. Because swing restoration transistors are used for each individual gate in this system, more transistors are needed. Recently, a brand-new, 10-transistor complete Adder circuit (10T) for applications requiring minimal power was suggested [23]. If buffers are not employed, this architecture falls short in terms of energy efficiency and complete logic swing. The majority of hybrid full adders designs do, however, demonstrate gain in only power, speed, or area at the price of the other performance criteria.

There is a need to investigate novel design techniques since none of the entire adder designs that have hitherto been published in-survey show reliable working in furnishing full logic- swing logic with a space- and energy-saving ULV result. The innovative energy-efficient complete adder cell described in this study was created by combining

multiple threshold voltage transistors with the GDI approach. The section of this essay is categorized into the following. In this Sect. 2, the GDI approach is briefly summarized. The design strategy for the suggested complete adder circuit is shown in Sect. 3. In Sect. 4, simulation findings and yield comparisons of the suggested design with several ones already in use are covered. Sect. 5 presents yield of 32-bit CP adder, and Sect. 6 summarizes the results.

## 2 GDI Approach Overview

This section provides a quick introduction to Gate-Diffusion Input, one of the modern digital logic approaches that have gained popularity [24]. Using the GDI approach, very sophisticated logic functions may be realized using just two transistors. The usage i.e. straightforward cell, seen in Fig. 1, is essential to GDI logic. The cell's construction is comparable to a static-CMOS inverter, although there certain important variations to be aware of.

The GDI cell has three inputs: the N-i/p, which is linked to the drain, source of the NMOS, the P-i/p, which is linked to the drain, source of the PMOS, and the G-i/p common input, which is linked to both the PMOS and NMOS.

The GDI technique was initially created for manufacturing in Silicon-on-Insulator (SOI) and twin-tub CMOS technologies [25]. Later, a Gate DI cell that is compatible with normal CMOS was introduced. The majority of logic operations, such as AND, OR, XOR, and MUX, were demonstrated to be complex and necessitate the use of 6–12 transistors when implemented Using transmission gate logic and static CMOS. However, the same operations could be implemented by simply changing the inputs in GDI cells, requiring only two transistors.. Comparison of the number of transistors used in Gate DI and conventional CMOS designing of various logic functions is shown in Table 2 along with Table 1 contains the Boolean table for leveraging GDI to implement various Boolean functions. Unlike the ubiquitous NAND and NOR logic gates, GDI's F1 and F2 universal logic functions may be utilized to implement additional complicated functions more effectively.

## 3 Proposed Model of Hybrid Full Adder Design

On the whole, a simple 1-bit complete adder's logic operations be described as

$$\text{Sum Output} = (\text{A xor B}) \text{ xor C} \tag{1}$$

$$\text{Carry\_out} = \text{AB} + \text{Cin.(A xor B)} \tag{2}$$

Only 14 transistors are used in the suggested complete adder architecture, as seen in Fig. 2. Five logic blocks that were created utilizing the MVT-GDI approach make up the majority of it.

$$\text{Sum Output} = \text{Cin (A xor B)} + \text{Cin (A x} - \text{nor B)} \tag{3}$$

One Swing Restored Transmission Gate (SRTG), two multiplexers, one XOR/XNOR, two XOR/XNOR, and technology are the other components. They were then altered near Table 1: application of various logic operations using GDI cells (Table 3).

**Table 1.** Utilizing GDI, some Boolean functions

| N | P | G | OUT | Function |
|---|---|---|---|---|
| 0 | B | A | A'B | F1 |
| B | 1 | A | A' + B | F2 |
| 0 | 1 | A | A' | NOT |
| B | 0 | A | AB | AND |
| 1 | B | A | A + B | OR |
| C | B | A | A'B + AC | MUX |

**Table 2.** Comparison of Transistors Count

| Function | Required Transistors Number | |
|---|---|---|
| | CMOS | GDI |
| f1 | six | two |
| f2 | six | two |
| or | six | two |
| not | two | two |
| and | six | Two |
| xor | twelve | Four |
| mux | twelve | Two |

**Table 3.** Transistor Sizes for Proposed Design

| Transistor Name | Length (nm) | Width(nm) |
|---|---|---|
| T1, 5 | 45 | 240 |
| T2, 6 | 45 | 120 |
| T3, 7 | 45 | 360 |
| T4, 8 | 45 | 120 |
| T11 | 45 | 480 |
| T9, 10, 12, 13, 14 | 45 | 120 |

Block of SRPTs or swing restored pass transistors. The GDI approach is used in the creation of the XOR/XNOR block. The XOR/XNOR blocks' inverters are integrated with typical VT devices since the route of the inverters has no voltage loss. In order to achieve the sum function, The Gate DI Multiplexer-1 multiplexes the control input (Cin) with the result of the X-OR (A B) and the X-NOR (A X-NOR B). As a result, the (1) can also be represented as in (3).

The GDI MUX-2 produces the carry output ($C_{out}$), multiplexing the inputs C-in and B by connecting a decision line to the X-NOR logic's output (A X-NOR B). Consequently, the (2) can also be shown as in (4)

$$\text{Carry Out} = (\text{A x} - \text{nor B}) \,.\, C_{in} + (\text{A x} - \text{nor B})\text{B} \tag{4}$$

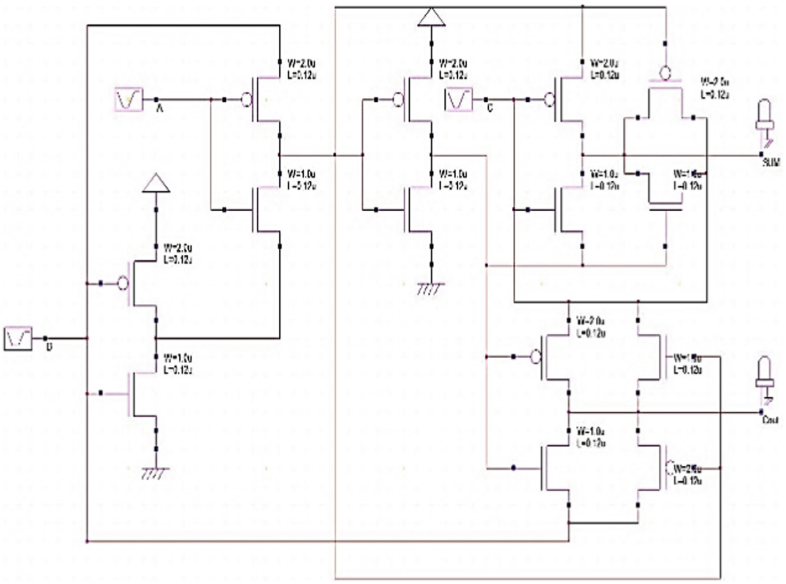

**Fig. 2.** Proposed 14 T Hybrid Full Adder

The suggested structure resembles other earlier XOR/XNOR logic-based systems as well as the authors' earlier GDI-based approach, although none of them achieves complete logic swing with just 14 transistors. A SRTG at the sum o/p and SRPTs at the carry o/p's are used in the suggested design to assure the entire swing (Cout). Table 4 illustrates how this complete adder operates with relation to the transistor states. When the sum o/p generation GDI MUX1 and the carry o/p generation Gate D input MUX-2 experience a VT drop The swing restoration transistors (T11, T12, and T13) are visible., and T14) are "ON" to give complete swing logic. Since, as indicated in Table 4, there is frequently no VT drop at the output; the transistors (T11, T12, T13, and T14) are also integrated with regular VT transistors.

**Table 4.** Functional Table

| A | B | C | SUM | Cout |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## 4 Comparisons of Results and Performance

The outcomes of the simulations and performance evaluations of the suggested complete adders are presented in this section. Cadence 45 nm CMOS technology is used for the simulations, with a Ultra LV of 0.2 V. The simulations' results for, Energy Delay Product (EDP), power, speed, energy and layout area performance metrics are contrasted with those of other designs described in the written word. Table 5 shows the simulation results for all adders, along with their number of transistor and area of the layout. The entire full –adder design shown in Table 5 are run at a speed of 20 kHz and a temperature of 300 K to preserve consistency in comparisons. For any of the complete adder architectures, no additional buffers are required to produce fair results. The observations of different adders performance for each criteria is shown in further detail below Table 5.

**Table 5.** Simulation Results Comparison

| Design | Average Power | Transistor Count | Reference |
|---|---|---|---|
| C-CMOS | 2.568 | 28 | [4, 6] |
| 16T Hybrid | 2.506 | 16 | [18] |
| CPL | 6.236 | 32 | [8, 9] |
| TFA | 2.98 | 16 | [10] |
| Proposed | 3.053 | 14 | Present |

From Table 5, it is clear that the count of transistors and greater switching frequency, the CPL design consumes the most energy. The load's charge and discharge capacitances resulted in this power consumption, which may be stated as follows: (5)

$$P = \alpha C_L V_{DD}^2 . f \tag{5}$$

where f is the circuit's operating frequency, CF is the switching frequency, and CL load capacitance.. Due to its lower transistor density, the GDI architecture is determined

to utilize the least amount of power. However, although having the same number of transistors, the GDI design uses less power than the 10T version because it has less leakage current [26–28]. The introduction of extra Low VT devices and swing repaired gates, which increase the switching activity and leakage components, respectively causes the suggested design to use more power than necessary. Because there is less delay, which is a crucial factor while running at ULV, this cannot be a problem in terms of energy usage.

Due to the exponential growth of the delay with supply voltage scaling in accordance with [29], it is crucial to include the delay while determining the circuit's energy metric when it is running at ULV. For strong inversion operation, the (5) can be represented as in (6).

$$C_L V_{DD} / I_{0e}^{((VDD-VT)/nV_{th})} \tag{6}$$

The latency in the sub-threshold zone of operation is exponentially larger due to the exponentially falling ON-current, contrary to what is predicted, where there is no major dependence on the VDD during strong inversion operation (Ion). It is evident from (5) that when the circuit operates at ULV, speed will exponentially decline, narrowing application range to low- to medium-frequency ranges [30, 31].

By subtracting delay equals 50% (input) of the input minus 50% (output)of the voltage swing calculated for each input transition. The speed is significantly increased since In the design proposed, the carry input ($C_{in}$) is propagated via a one GDInput-MUX, minimizing the carry delay propagated. When compared to previous designs in the literature, it can be shown that the suggested design has a substantially lower latency and achieves >64% savings. This is accomplished by utilizing more swing restored gates and low VT components, which enhance output driving capabilities. The 10T design's longer delay is mostly caused by its lower driving power at lower supply voltage.For digital computational systems, the two key performance indicators that assess a circuit's effectiveness are energy and the Energy Delay Product (EDP). Table 5 makes it evident that, when compared to the other designs, the suggested design has the best energy and EDP parameters.

The suggested complete adder circuit's area is determined by the Fig. 3 shows architecture created for 45 nm technology. Due to the higher transistor density of the CPL architecture, it requires more space, density, and it also has a layout that is more complicated with the existence of additional metal-rails used to implement the logic. Despite having more transistors, $C^2$MOS & mirror full-adder designs use about the same space in the TGA design because of their straightforward and consistent architectures. With the exception of the 10T and GDI designs, the suggested design takes up considerably less space than the other concepts.

Additionally, the suggested design offers consistent performance TT, FF, FS, SF and SS are just a few of the process corners that they can be used for. Figure 2 displays the differences in the suggested design's power consumption and delay. As anticipated, the largest power consumption and delay are shown at the FF and SS corners, while the least values are seen at the SS and FF process corners.

The energy metric of the proposed design in 45 nm technology is normalized to 32 and 22 nm and compared with the recently proposed CMOS hybrid full adder designs in

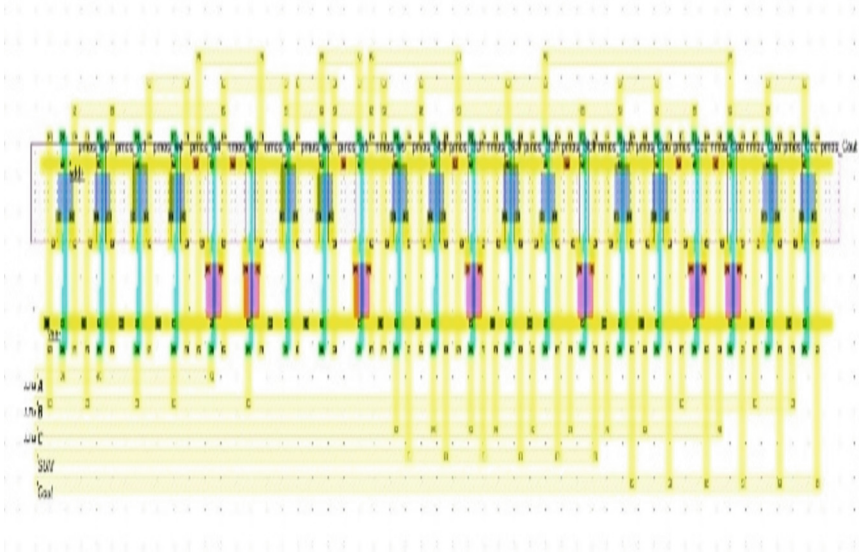

**Fig. 3.** Proposed 14 T Hybrid Full Adder

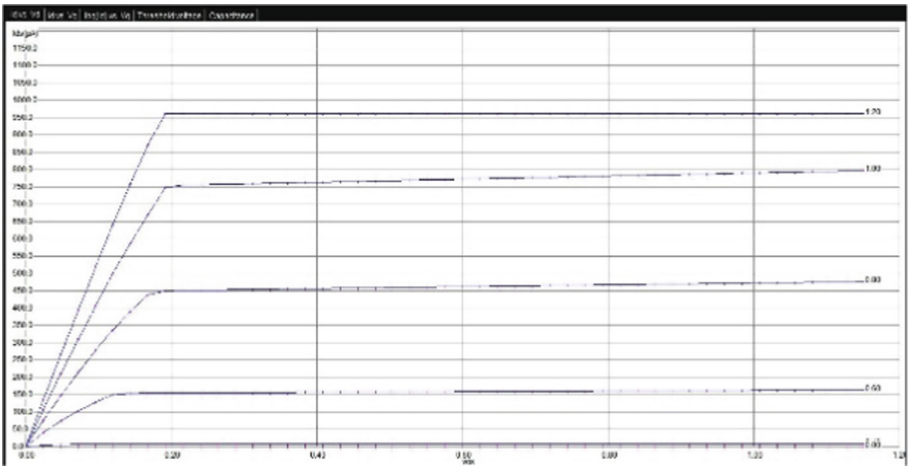

**Fig. 4.** $I_{ds}$ and $V_{ds}$ Responses

order to determine the efficiency of a suggested development with the latest technology improving trends adhering to the (ITRS) and (IRDS). According to Fig. 4, 5 the normalized energy (EN) meter is derived from the technological scaling trends of the energy measure and VDD.

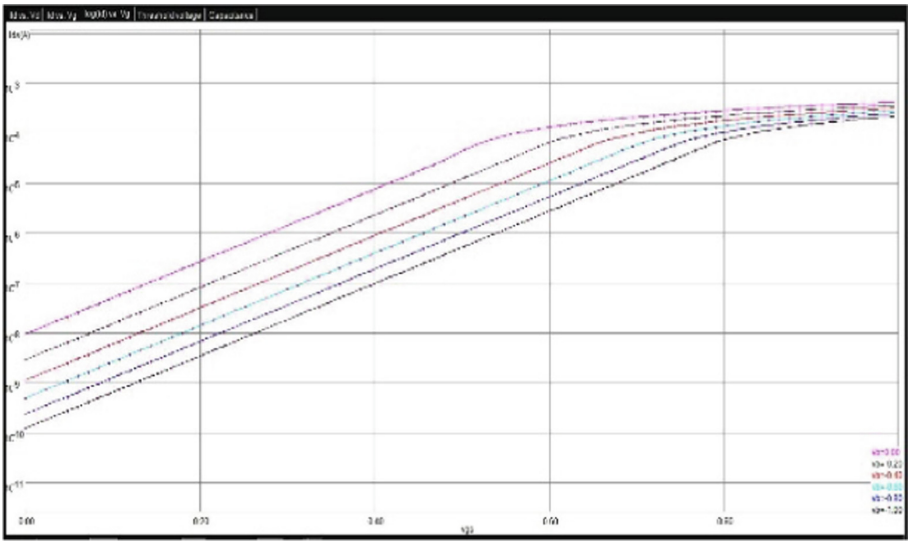

**Fig. 5.** Log $I_d$ and $V_g$ Responses

## 5 32-Bit Carry Propagation Adder Performance

To exercise the efficiency of the suggested gate input-based crossover architecture in hand on applications, the authors cascaded the suggested one bit FA design to produce a 32-bit CP adder structure. Carry propagation occurs in this from the first adder block to the last. The authors included the buffers at the right points in the design to guarantee the cascaded system's improved driving capabilities. According to (10), how many GDI cells can be connected between two buffers under the assumption that the cascaded system's overall maximum permissible voltage drop is 0.2 VDD. Using the GDI technique as the foundation for the authors' recommended designs, N's value was estimated from (10) using the formula Vdrop = VT, yielding a result of 2. It was also possible to mimic this 32-bit adder design with and without the use of buffers. Using buffers drastically reduced the latency (Fig. 6).

$$N = 0.2\, V_{DD}/V_{drop} \tag{7}$$

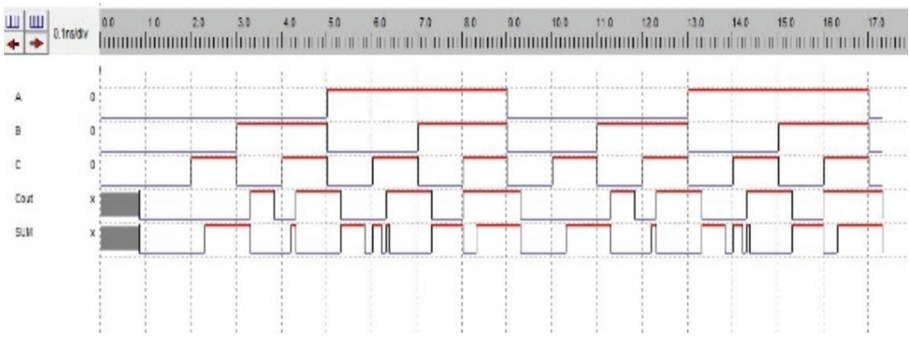


**Fig. 6.** Simulation Results

## 6 Conclusion

Here, the authors present the 14TMVT-GDI, a brand-new complete adder circuit. The simulations were run in cadence mode using a 0.2 V and 45 nm technology ULV. The outcomes are contrasted with other published hybrid, 10T, and GDI full adder designs as well as typical such as CMOS, CPL, TGA, and others, are full adder architectures. The suggested Designs are resistant to regional and global change changes, according to Monte-Carlo simulations. According to developments in ITRS technology scaling, normalized energy consumption also reveals that the suggested design delivers greater energy savings of 57% during the time before the current works. The suggested architecture was expanded upon to incorporate 32-bit full adders at the relevant stages (after two stages), both with and without the usage of buffers. Therefore, the majority of applications for energy- and space-efficient computing might adopt the suggested complete adder circuit architecture.

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