BLE Receiver with Fast DC Offset Cancellation and Carrier Frequency Offset Compensation

Cong Qiu(✉)

School of Electronic Communication Technology, Shenzhen Institute of Information Technology, Shenzhen, Guangdong Province, People's Republic of China
qiucong@sziit.edu.cn

Abstract. A BLE receiver with fast DC offset cancellation and carrier frequency offset (CFO) compensation is presented. The receiver employs a fully integrated RF front-end and a digital modem. The BLE SoC with embedded flash is fabricated in 55 nm RF CMOS technology, the receiver achieves sensitivity of −95 dBm and the CFO compensation in digital modem helps to extend the CFO tolerance from ± 100 kHz (BLE spec.) to ± 250 kHz with only 2 dB sensitivity degradation.

Keywords: Bluetooth low energy · DC offset cancellation · Carrier frequency offset compensation · System-on-chip

1 Introduction

Bluetooth Low-Energy (BLE) is becoming widely used in consumer IoT devices because it can communicate directly with mobile terminals (smart phones or tablets) and consumes very low average energy. In real wireless environment, the signal strength varies greatly, the receiver is required to have high gain and fast gain switching, which may lead to DC offset problem. On the other hand, due to the non-ideal reference crystals for the transmission and reception, there must be a certain carrier frequency offset between both side, which will also reduce the reception performance. In this work, a receiver with fast DC offset cancellation (DCOC) and carrier frequency offset (CFO) compensation is presented, it employs a fully integrated RF front-end and a digital modem.

2 Design of Building Blocks

As shown in Fig. 1, the proposed receiver adopts a single-conversion low-IF architecture with integrated tunable complex filter which performs image rejection and partial channel selection functionality. The down-converted IF signal is amplified by the PGA (Programable Gain Amplifier) and then digitized by the ADC for further signal processing in digital domain. The local-oscillator (LO) of RX is generated by a 4.8 GHz frequency synthesizer, the choice of a LO frequency of 2 × RF solves the pulling in TX, it can also minimize the effect of LO leakage into the receiver, thereby reducing LO self-mixing induced DC offset.

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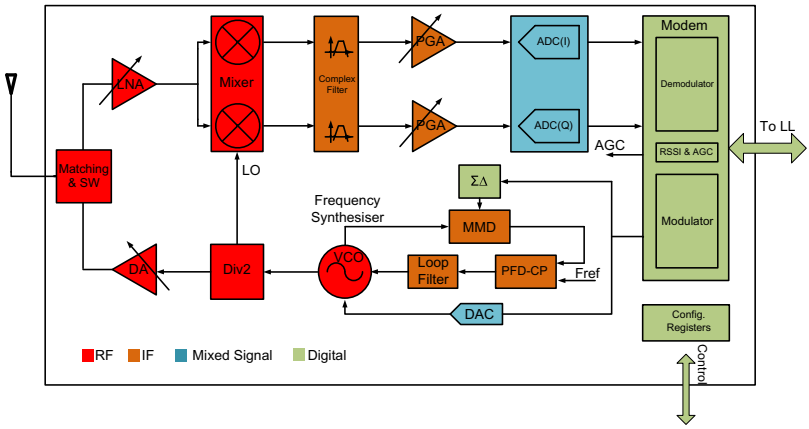

Fig. 1. Transceiver architecture

2.1 RF Front-End with On-chip Matching

The LNA input is shared with the PA output pin using an on-chip matching network and switches [1], as shown in Fig. 2, The LNA [2] is an inductor source degenerated amplifier with L-C load at the output, it is differential, requiring a transformer acts as BALUN for single-end conversion. In RX mode, switch S1 is shorted to ground and switch S2 is open, LG, CP, together with the transformer (LP, LS1, LS2) realize the desired LNA input matching network.

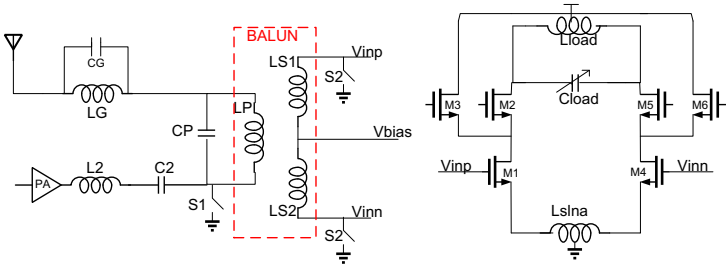

Fig. 2. RF front-end and on-chip matching

2.2 DCOC Scheme

To avoid saturating the ADC or deteriorating the RX sensitivity performance, DC offset cancellation (DCOC) is needed, especially when the gain of the PGA is large (30 dB or above) [3]. Figure 3 shows the block diagram of the proposed DCOC scheme, I-Path and Q-Path DC offset is cancelled individually, the analog comparator (COMP) compares the differential output of I-Path(Q-Path) and generates “0” or “1”, the digital counter accumulates the numbers of “0” and “1” for several microseconds and then control the 8-bit DAC to cancel the DC offset at the input of RX ABB (analog

baseband, including complex filter and PGA) to keep the numbers of "0" and "1" are equal to each other, thus the DC offset residual is close to zero. According to BLE specification, there is only 8 μs preamble ("01010101" or "10101010" pattern) for automatic gain control (AGC) [4], DCOC should be settled in such short time. A lookup table with different DAC codes related to different RX gain is used to meet such stringent requirement. The codes in the table will be updated every time the SoC wakes up from sleep mode and stored in the retention RAM.

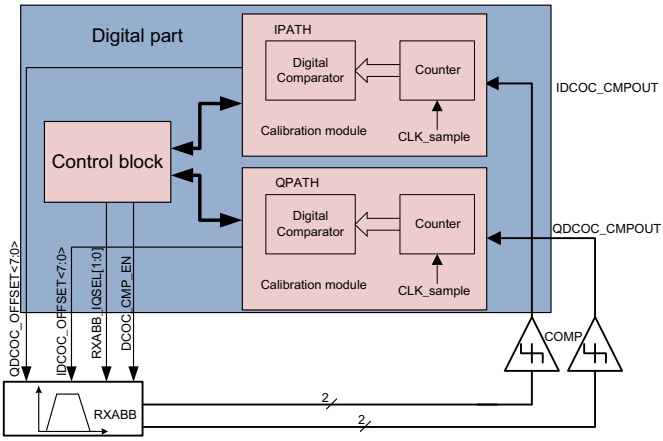

Fig. 3. DCOC scheme

2.3 Digital Modem with CFO Compensation

Figure 4 shows the digital GFSK modem, which has several functionalities such as RSSI calculation, AGC, digital down-conversion (DDC), channel-select filtering(FIR), carrier recovery etc. The Carrier Frequency Offset (CFO) is estimated based on the preamble pattern and feed-forward compensated during demodulation process.

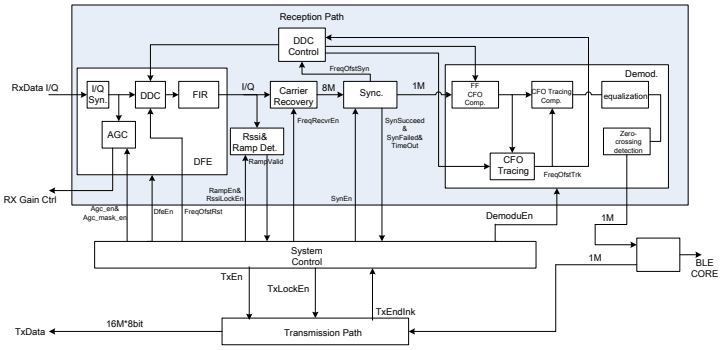

Fig. 4. Modem architecture

3 Measurement Results

The SoC is fabricated in 55 nm RF CMOS technology and the die photo is shown in Fig. 5. The radio (RF), modem, link controller, CPU, and memories (embedded flash, SRAM) are all integrated on chip, along with a PMU (Bulk DC-DC Converter and LDOs), oscillators (Crystal and RC Oscillators) and digital & analog peripheral blocks.

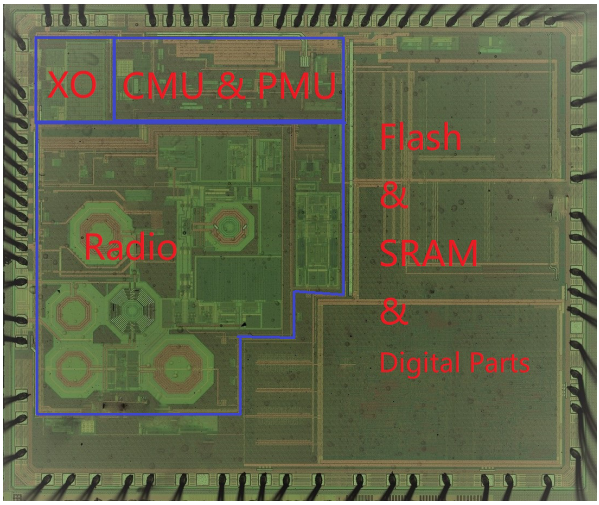

Fig. 5. Die photo

3.1 RX Input Reflection Coefficient

The input reflection coefficient in RX mode is measured by a vector network analyzer as shown in Fig. 6. It achieves good matching, less than -15 dB at 2.4 GHz.

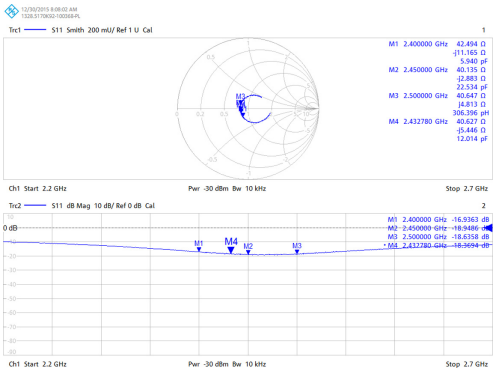

Fig. 6. RX input reflection coefficient

3.2 DCOC Settling Time

Figure 7 and Fig. 8 show the DCOC and AGC settling process respectively, the settling time is less than 3 μs while switching PGA gain from 18 dB to 42 dB, which satisfies the requirement of BLE system (less than 8 μs).

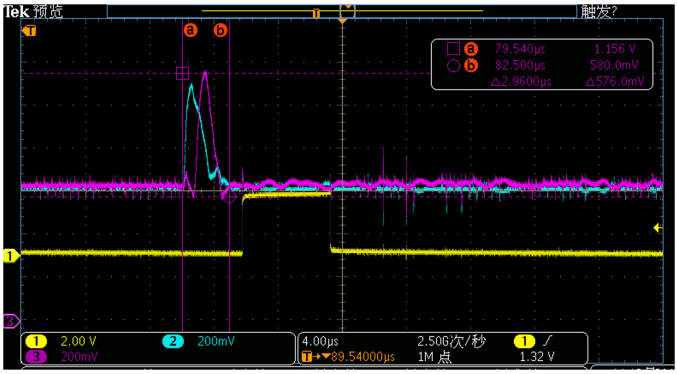

Fig. 7. DCOC settling process (The blue and pink lines represent I-Path and Q-Path DC offset respectively). (Color figure online)

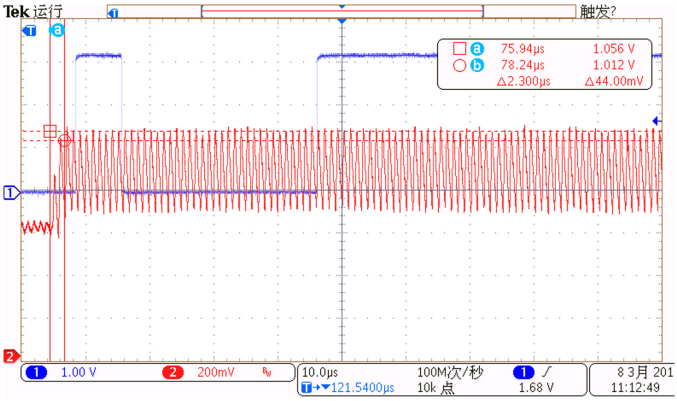

Fig. 8. AGC settling process (−70 dBm Input, RXABB gain 18 dB–42 dB)

3.3 Rx Sensitivity

Figure 9 shows the packet error rate (PER) performance of the RX. The RX measurement follows the BLE specification definition, i.e., packet error rate (PER) of 30.8% [4], and it achieves a sensitivity of −95 dBm for 37 octet packets (1 Mbps) with zero carrier-frequency offset (CFO). The CFO compensation in digital modem helps to extend the CFO tolerance from ± 100 kHz (BLE spec.) to ± 250 kHz, the sensitivity degradation is only about 2 dB.

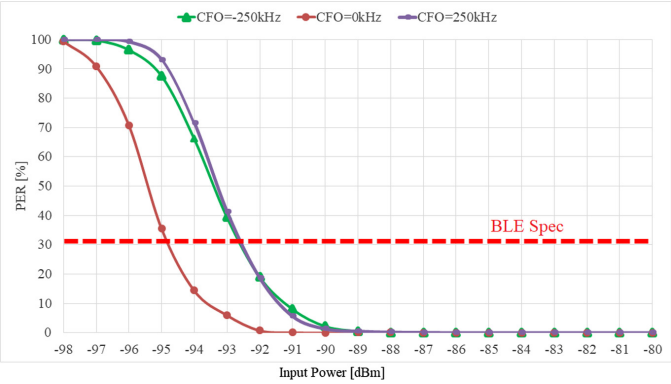

Fig. 9. RX sensitivity

4 Conclusion

A fully integrated BLE receiver with fast DCOC and CFO compensation in 55-nm RF CMOS process was presented. The DCOC settling time is less than 3 μs and the CFO tolerance is extended to ± 250 kHz with only 2 dB sensitivity degradation.

References

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