A 3-Stacked GaN HEMT Power Amplifier with Independently Biased Technique

Luong Duy Manh[1(✉)], Tran Thi Thu Huong[1], Bui Quoc Doanh[1], and Vo Quang Son[2]

[1] Le Quy Don Technical University, 236 Hoang Quoc Viet, Hanoi, Vietnam
duymanhcs2@mta.edu.vn

[2] University of Transport and Communications, No. 3 Cau Giay, Hanoi, Vietnam

Abstract. A design of 3-stacked GaN high-electron-mobility transistor radio-frequency power amplifier using independently biased technique is presented. The power amplifier operates at 1.6 GHz for wireless communications applications. By independently setting proper bias conditions, DC power consumption of the power amplifier can be reduced leading to efficiency enhancement without output power degradation. A performance comparison of the proposed power amplifier with a conventional 3-stacked power amplifier has been performed. The simulated results indicate that the proposed power amplifier offers superior efficiency over the conventional one.

Keywords: Power amplifier · GaN HEMT · Independently biased

1 Introduction

Traditional circuit configurations have been proposed to improve performance of power amplifier including Darlington [1,2], cascode [3,4] and hybrid [5] configurations. The Darlington configuration can handle very high current capability that is highly suitable for power amplifier design. The cascode configuration, however, can offer various advantages such as wide bandwidth and high gain. The hybrid configuration which combines a bipolar junction transistor (BJT) and a field effect transistor (FET) can offer low output impedance and low DC power consumption. Although these configurations have been proved to deliver various promising advantages, they still exhibit inherent drawbacks for high-frequency power amplifier design. One of the most critical drawbacks of these configurations is that they are not able to independently adjust bias condition of each transistor in the configuration. This reduces degrees of freedom in performance improvement. Recently, independently biased InGaP/GaAs HBT cascode [6] and independently biased 3-stacked InGaP/GaAs Heterojunction bipolar transistor (HBT) [7] configurations have been reported for RF power amplifier (PA) design. Theses proposed configurations can offer the possibility of independent control

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of bias condition. Nevertheless, they still exhibit low output power due to low power capability of a HBT device.

In addition to these configurations, an independently biased 3-stacked GaN high-electron-mobility transistor (HEMT) has been introduced in [8]. However, this structure was just in the form of a bare chip and the investigated results were performed for this type of chip but not for a power amplifier design. In this paper we practically implement a design of a PA based on the independently biased technique for a 3-stack GaN HEMT structure as presented in [8]. An investigation on how an independently biased approach in the 3-stacked GaN HEMT configuration can improve efficiency and output power is carried out. The rest of the paper is organized as follow: Sect. 2 will describe in details the proposed amplifier. Investigation of performance of the proposed amplifier will be conducted in Sect. 3. Then Sect. 4 will present experiment including experimental setup for large-signal measurement and measured results. Finally, Sect. 5 will conclude the paper.

2 Descriptions of the Proposed Amplifier

2.1 3-Stacked GaN HEMT MMIC Chip

Schematic of the 3-stacked GaN HEMT configuration is illustrated in Fig. 1a. Three GaN HEMT devices are connected to each other in a cascode-type topology. In addition to the conventional bias terminals including gate bias and drain bias terminals, two additional bias terminals are inserted to two floating points between the first and the second transistors and between the second and the third transistors. Owing to this approach, bias condition of each transistor in the proposed configuration can be independently controlled. In practice, the 3-stacked GaN HEMT structure is realized using a MMIC (Monolithic Microwave Integrated Circuit) technology from WIN Semiconductor Corp. foundry service [9]. The service includes following information: metal thickness = 4 μm, substrate thickness = 100 μm. The schematic and MMIC layout of this structure are described in Fig. 1. As can be seen in the figure, in the MMIC layout, two RF-bypass capacitors are realized using a metal-insulator-metal (MIM) technology while input and output terminals are ground-signal-ground (GSG) connections for chip evaluation using GSG probes in practice. Interconnects inside the MMIC chip are made using metal transmission lines. Three GaN HEMTs have the same size of 0.25 μm × 0.75 μm × 4 fingers. The total size of the MMIC chip is 674 μm × 1025 μm

2.2 Power Amplifier

Figure 2 shows descriptions of the proposed amplifier which is realized using the 3-stacked GaN HEMT topology as an active device. The MMIC chip is connected to the external components including input/output matching networks and biasing lines through gold bonding wires (BW) with a diameter of

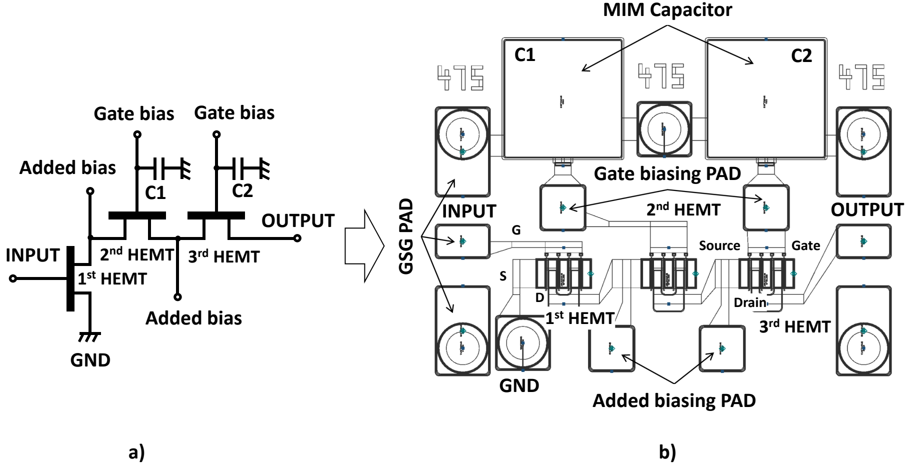

Fig. 1. Proposed 3-stacked GaN HEMT topology: a) Schematic and b) MMIC layout.

30 μm. Input matching network (IMN) and output matching network (OMN) are implemented using off-chip lumped components from Murata libraries [10]. Values of the IMN components are: L_1 : LQW18AN4N3C00 (4.3 nH), C_1 : GRM1555C1HR90WA01 (0.9 pF) and values of the OMN components are: L_2 : LQW18AN12NG00 (12 nH), C_2 : GRM1555C1HR30WA01 (0.3 pF). Gate bias of the first transistor and drain bias of the third transistor are implemented using Bias-Tees including a RF choke inductor and a block capacitor C_b. In addition, drain bias of the first and the second transistors are implemented using two quarter wavelength transmission lines. Here, it is noted that the IMN and OMN are designed to match source and load impedances of the MMIC chip to 50 Ω at only the fundamental frequency without using any harmonic termination techniques. This is a reason why the IMN and OMN just include a combination of a inductor and a capacitor as indicated in the figure. Optimum fundamental source and load impedances are found by using a simulated load/source pull method based on non-linear models of GaN HEMT provided by WIN Semiconductor Corp. Their values are found as follow: $Z_S = 79.3 + j138.6\,\Omega$, $Z_L = 134.7 + j174.1\,\Omega$ where Z_S and Z_L are the optimum source and load impedances, respectively.

3 Performance Evaluation

3.1 V_{d1} Variation

The most important feature of the proposed amplifier is the high degree of freedom in bias adjustment of each transistor leading to the PA performance improvement. In the proposed circuit topology as indicated in Fig. 1, two added

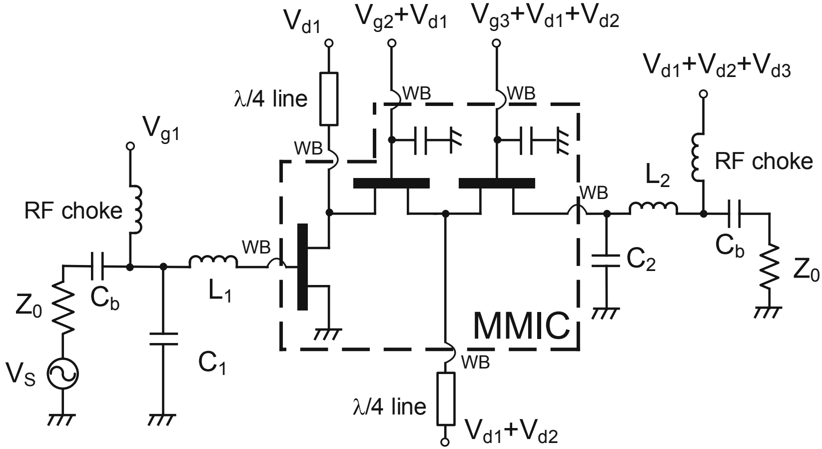

Fig. 2. Schematic.

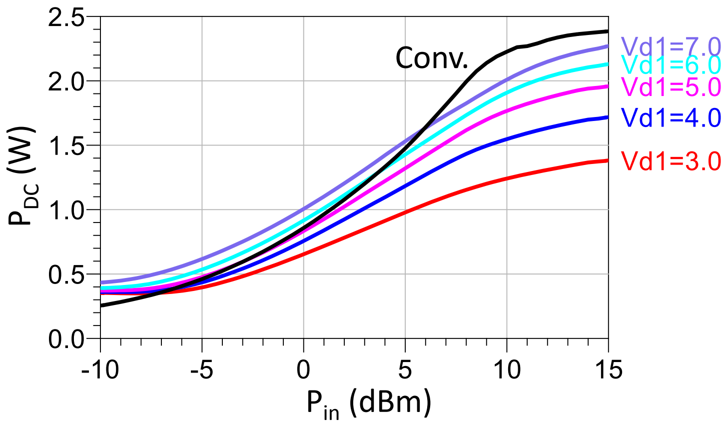

Fig. 3. DC power of the conventional and proposed 3-stacked PA vs. input power with variation of $V_{\mathbf{d1}}$. The black curve represents DC power of the conventional configuration.

bias terminals have been included in order to bias the drain terminals of the first ($V_{\mathbf{d1}}$) and the second ($V_{\mathbf{d2}}$) transistors. This means, by appropriately controlling these bias values ($V_{\mathbf{d1}}$ and $V_{\mathbf{d2}}$), PA performance such as power added efficiency (PAE) and output power can be significantly improved. Firstly, the variation of $V_{\mathbf{d1}}$ will be investigated. The main contribution of this independent bias control is to re-contribute the DC power consumption of the PA. This helps to increase efficiency while ensure sufficient output power. This re-contribution of the DC

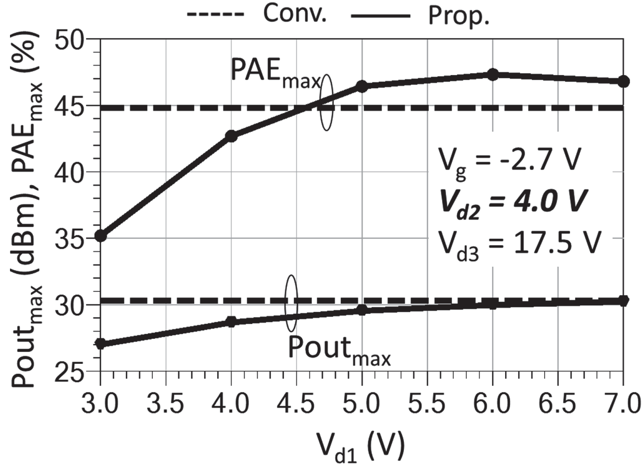

Fig. 4. Maximum PAE and Pout as a function of varied $V_{\mathbf{d1}}$. Performance comparison with a conventional structure is also shown.

power can be seen in Fig. 3. Decreasing $V_{\mathbf{d1}}$ while keeping $V_{\mathbf{d2}}$ and $V_{\mathbf{d}}$ results in lower DC power at high input power region. This means that maximum efficiency (PAE) can be enhanced since the maximum PAE occurs at the high input power region. This can be further understood because there is a re-contribution of quiescent drain currents among transistors leading to a re-contribution of DC power consumption when changing the bias values. On the other hand, a conventional 3-stacked configuration which has a similar topology with the proposed 3-stacked one as indicated in Fig. 1a but without using two added bias terminals is not able to make this re-contribution of the DC power. Here, it is noted that all three transistors of the proposed configuration are biased in a class-AB. All three gate bias voltages are set to -2.7 V and the third drain bias voltage ($V_{\mathbf{d3}}$) is kept at a constant value of 27.5 V. Similar bias conditions are made for both the conventional and proposed configurations in order to make a logical comparison between them. The effect of DC power reduction with respect to the change of $V_{\mathbf{d1}}$ on PA performance can be clearly seen in Fig. 4. As can be seen in the figure, when $V_{\mathbf{d1}}$ changes from 3.0 V to 7.0 V, both PAE and Pout can be significantly varied. When $V_{\mathbf{d1}}$ increases, $\mathbf{PAE_{max}}$ can be higher than that of the conventional one while $\mathbf{Pout_{max}}$ can still remain the same level as the conventional one. To make a superior trade-off between efficiency and output power compared with that of the conventional one, $V_{\mathbf{d1}}$ should be set to 5.5 V.

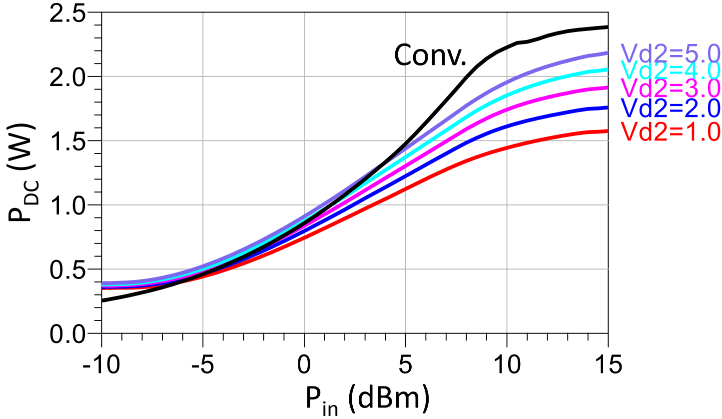

Fig. 5. DC power of the conventional and proposed 3-stacked PA vs. input power with variation of $V_{\mathbf{d2}}$. The black curve represents DC power of the conventional configuration.

3.2 $V_{\mathbf{d2}}$ variation

After setting $V_{\mathbf{d1}}$, $V_{\mathbf{d2}}$ then will be considered for performance improvement. Figure 5 illustrates the effect of $V_{\mathbf{d2}}$ variation on the DC power re-contribution inside the PA. It once gain can be seen that decreasing $V_{\mathbf{d1}}$ while keeping $V_{\mathbf{d1}}$ and $V_{\mathbf{d}}$ results in lower DC power at high input power region. This re-contribution of DC power also helps to increase PAE with an expense of low output power.

The dependence of maximum PAE and maximum Pout of the conventional and proposed 3-stacked GaN HEMT configurations with variation of $V_{\mathbf{d2}}$ is shown in Fig. 6. In this figure $V_{\mathbf{d1}}$ is kept at 5.5 V. The figure shows that when $V_{\mathbf{d2}}$ changes from 1 to 5 V, maximum PAE first increases and reaches maximum values at the middle region and drop at high values while maximum Pout increases with the increasing $V_{\mathbf{d2}}$. According to this figure, to remain sufficient output power without degradation of efficiency over the conventional one, $V_{\mathbf{d2}}$ is chosen to be 4.0 V.

4 Experiment

4.1 PA Prototype

After considering optimum bias conditions for the proposed PA, a prototype of the PA has been fabricated as indicated in Fig. 7. The external Bias-Tees for biasing the gate of the first transistor and the drain of the third transistor are not shown in the figure. Female and male SMA connectors function as the input and output ports, respectively. The prototype was fabricated on a Megtron6 substrate from Panasonic with following parameters: dielectric constant = 3.7, substrate thickness = 0.75 mm, dissipation factor = 0.002 and copper thickness =

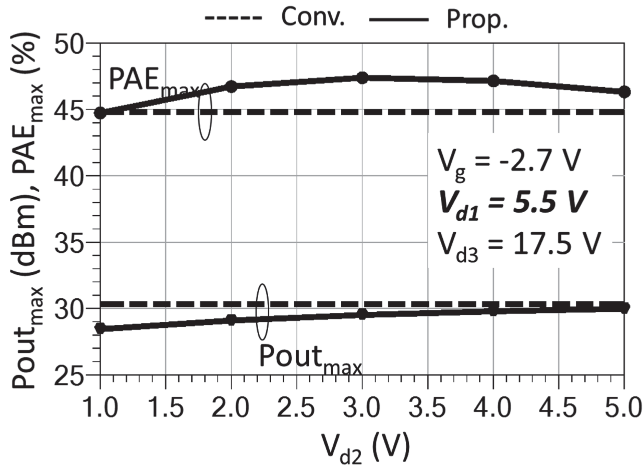

Fig. 6. Maximum PAE and Pout as a function of varied $V_{\mathbf{d2}}$. Performance comparison with a conventional structure is also shown.

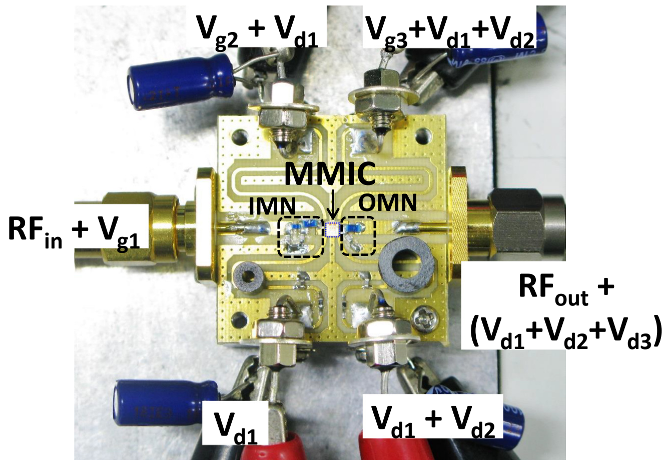

Fig. 7. Fabricated PA prototype.

35 µm. In the measurement of the PA prototype, bias condition of each transistor which are found from the previous section are used. The bias conditions for the proposed configuration are as follow: $V_{\mathbf{g}} = -2.7\,\text{V}$, $V_{\mathbf{d1}} = 5.5$ V, $V_{\mathbf{d2}} = 4.0\,\text{V}$, $V_{\mathbf{d}} = 17.5\,\text{V}$ while the bias conditions for the conventional one are as follow: $V_{\mathbf{g}} = -2.7\,\text{V}$, $V_{\mathbf{d}} = 27\,\text{V}$ which is equivalent to $V_{\mathbf{d1}} + V_{\mathbf{d2}} + V_{\mathbf{d3}}$.

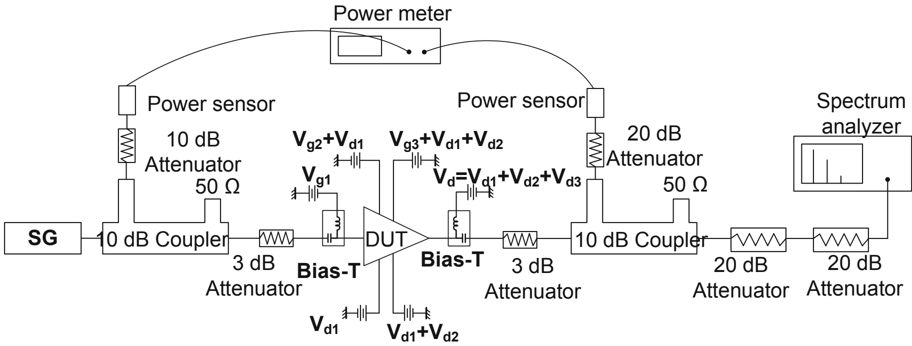

Fig. 8. Experimental setup.

4.2 Experimental Setup

The experimental setup for large-signal measurement of the PA prototype is described in Fig. 8. A microwave signal generator (SG) is employed to input RF signal to the PA at an operation frequency 1.6 GHz. Two Bias-Tee symbols are clearly visible in the figure. Two RF directional couplers are used to slit the input and output RF signals to make input and output power measurement. Power measurement is made by using power sensors combined with a power meter. All components for power measurement are carefully calibrated prior to make actual measurements. A spectrum analyzer (SA) is employed to check the output spectrum as well as to verify if the PA is unintentionally oscillated during the large-signal measurement.

4.3 Measured Results

The measured large-signal performance including PAE, output power and gain are shown in Fig. 9 which shows the measured and simulated PAE, Pout and gain of the designed PA. The PA is biased at the optimum bias condition which is found from the previous sections. The practival bias condition is given as follow: $V_{\mathbf{g}} = -2.7$ V, $V_{\mathbf{d1}} = 5.5$ V, $V_{\mathbf{d2}} = 4.0$ V, $V_{\mathbf{d}} = 17.5$ V. As can be seen in the figure, measured results agree well with the simulated one. This implies that the simulations predict well performance of the proposed 3-stacked Gan HEMT PA. There are some discrepancies between simulation and measurements caused by losses in the PA assembly process and losses in realistic lumped components.

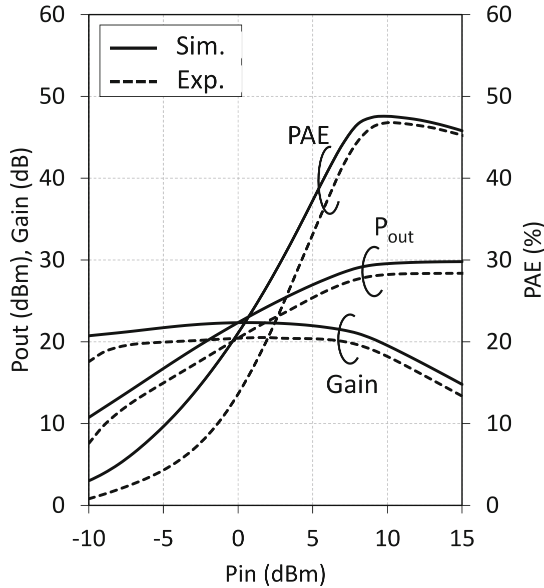

Fig. 9. Large-signal performance measurement vs. simulation.

5 Conclusion

This paper presents the design of the independently biased 3-stacked GaN HEMT power amplifier operating at 1.6 GHz for wireless communications. It has been shown that by independently adjusting the added bias terminals $V_{\mathbf{d1}}$ and $V_{\mathbf{d2}}$, efficiency of the proposed PA can be significantly improved due to the re-contribution mechanism of DC power consumption. When comparing with a conventional 3-stacked GaN HEMT amplifier, the proposed amplifier exhibits higher efficiency with similar output power level if $V_{\mathbf{d1}}$ and $V_{\mathbf{d2}}$ are properly controlled. The measured results agree well with the simulated ones validating the design method.

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