An Ultra-low-Power Integrated Heartbeat Detector for Wearable Sensors

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Abstract. To optimize energy consumption in wearable sensor networks, an efficient scheme is to set the sensors in sleep mode and wake them up to engage communication. However, synchronicity between the sensors needs to be assured by always-on local oscillators. This work proposes a different topology that takes advantage of the heart beat to wake-up wearable sensors. The electrocardiogram (ECG) is detected by two probes and then converted into a pulse signal. Using 28-nm FD-SOI CMOS technology, this solution is implemented on a circuit consuming 19 nW at a 900 mV supply voltage, hence suitable for long term and wearable applications.

Keywords: Heartbeat detection · Integrated circuit design · 2-electrode sensing · FD-SOI technology

1 Introduction

In the context of wearable systems, every integrated sensor needs a long battery life in order to avoid frequent replacements. Because communication is the most energy-hungry part of each sensor, data exchanges between the sensors (or nodes) and aggregators have to be reduced to a minimum, while maintaining the synchronization between all the nodes.

A conventional solution to address this problem is putting the nodes to sleep most of the time, and regularly wake up the nodes at defined time steps. During the wake-up phase, the aggregator can establish specific communication with certain nodes, which remain active, whereas the others return in sleep mode. While reducing the average power consumption of the nodes, it requires an always-on local oscillator in each node. Moreover, all the oscillators have to be in sync so that the communication between the aggregator and the nodes can be established.

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On the human body, the heartbeats can be interpreted as a clock signal with a low duty cycle, and act as a synchronized wake-up signal [1,9]. An example of a heart-rate paced communication is depicted in Fig. 1. A typical application for this slow-paced scheme is posture or pose recognition [11,12]. Once a heartbeat occurs, all the nodes and the aggregator are activated. The aggregator sets up a communication with some nodes, *e.g.* Node1, and the other nodes go back in sleep mode. Compared to the previous scheme, the local oscillators are replaced by independent heartbeat detectors in each node. This method has the advantage to ensure synchronicity for the wake-up phase between all the nodes distributed on the entire body.

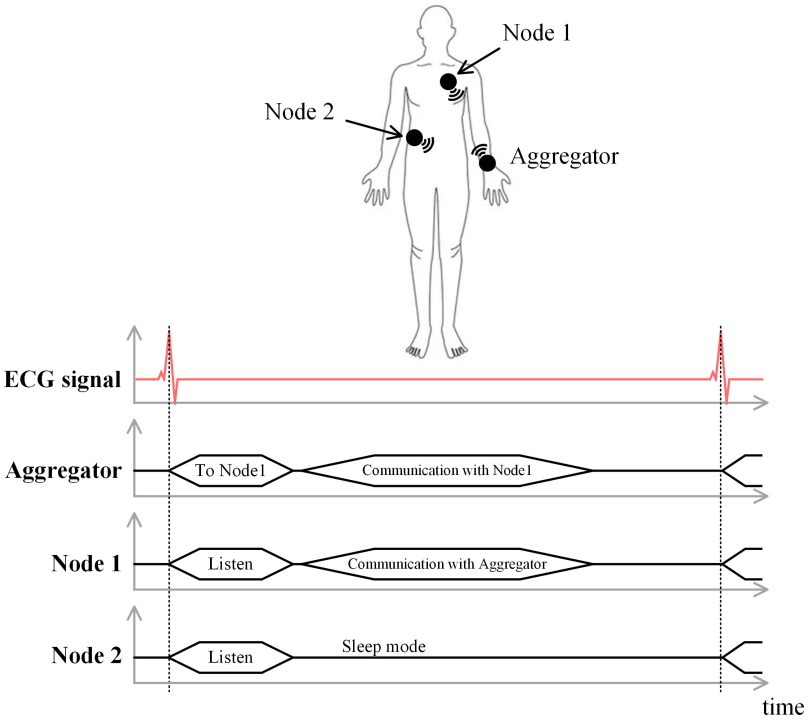

Fig. 1. Example of heart-rate scheduled communication between wearable sensors.

For an always-on system, using Components Off-The-Shelf (COTS) is not an option, as the power of such a system is in the range of tens of milliwatts, like in [14]. In the state-of-the-art, integrated heartbeat detection is done by digitizing the ECG signal with an Analog-to-Digital Converter (ADC), and then processing the digital data with a Digital Signal Processor (DSP) [4,10]. However, this scheme is truly efficient when the objective is to reconstruct the ECG signal with high fidelity [5,7,15,17]. In the proposed context, only the fact that a heartbeat occurred is important, not the waveform in itself. Therefore, an

energy-hungry structure ADC + DSP is not relevant to be embedded on each node. Moreover, in all the systems, a reference electrode located far from the sensing electrodes is needed to get rid of parasitics, 50 Hz interference. A 2-electrode heartbeat detector circuit focusing on timing and not on signal reconstruction has been integrated in [8], consuming 58 nW. An external microcontroller (not taken into account in the energy consumption figure) is nonetheless still needed to adjust the comparator threshold. In [3], Bose *et al.* present a 2-electrode heartbeat detection system with self-adaptation of the comparator threshold consuming 504 nW in the analog front-end. However, in these 2 reference works, the comparator threshold is adapted compared to an absolute reference, and needs to be changed dynamically depending on the baseline drift of the ECG signal. The calibration circuit is therefore active all the time and increases the energy consumption of the whole system. Moreover, the last work relies on the fact that the 2 electrodes are far from each other (tens of centimeters) to sense a significant difference between the ECG signals, which limits the embedded character and comfort of the system.

This paper proposes a standalone heartbeat detector circuit functioning without an external microcontroller, making use of the 28-nm FD-SOI CMOS process for self-calibration through body biasing. The detection threshold is set using the common-mode of the ECG signal as a reference. Therefore, once calibrated, the decision threshold does not need to change. The 28-nm FD-SOI CMOS technology process also offers efficient co-integration with advanced-pitch digital circuits for embedded processing using the heart-rate as a clock signal. The proposed circuit was designed to function with 2 cm-spaced electrode signals lower than 1 mV, without a need for an additional reference electrode on the body, and thus completely integrable on a wearable device. The proposed circuit has been simulated with a 900 mV supply V_{DD} and consumes 19 nW.

This paper is organized into the following sections. Section 2 provides an overview of the system, Sect. 3 explains the circuit blocks in detail, Sect. 4 presents the results from both system-level and transistor-level simulations and Sect. 5 concludes the paper.

2 System Overview

The proposed structure is based on the differential ECG heart rate measured between 2 input electrodes, depicted in Fig. 2. The objective is to detect the high amplitude of the R-wave in the QRS complex for each heartbeat. The 2 electrodes are capacitively coupled to the inputs of the differential amplifiers for DC offset suppression. The input biasing voltage is set to $V_{DD}/2$ through large resistors in the TΩ range allowing input impedances orders of magnitude larger than the electrodes impedances $1/G_1$ and $1/G_2$. These resistors are implemented using transistor-based pseudo-resistors, yielding a silicon occupation of 10 μm^2, and thus compatible with on-chip integration. The resulting high-pass filters are called **HPF1** and **HPF2**.

Since the electrodes are very close from each other, they sense the same ECG signal with very few differences. The closer the 2 ECG signals are, the

more the difference needs to be amplified to be sensed. However, the energy consumption of the analog front-end increases with the amplifier gain. To amplify the difference between the ECG signals without increasing the amplifier gain, the values of the capacitances in the filters **HPF1** and **HPF2** are voluntarily mismatched so that the 2 cut-off frequencies are not matched anymore, and as a result the 2 filtered ECG signals are different. The filters original cut-off frequency is set 15 Hz to attenuate baseline drift and motion artifact. The influence of the voluntary frequency mismatch is studied further in Sect. 4.1.

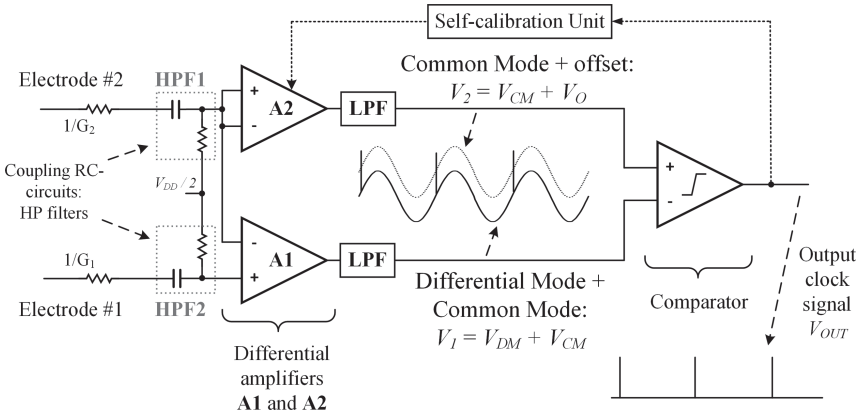

Fig. 2. Block diagram of the proposed circuit.

The differential ECG signal is first amplified by amplifier **A1** with a differential gain G_D. Amplifier **A1** is used to amplify both the differential signal of the probes corresponding to the heart rate (typically in the range of 100 µV to 1 mV from [16]), and also the common mode of the input signals with a lower gain G_{CM}. It also includes a Common-Mode Feedback (CMFB) loop for internal stability. Amplifier **A2** is designed the same way as **A1**, especially with a similar G_{CM}, and permits amplifying the common mode reference only, by putting the same signal at both inputs of the amplifier. The output of **A1**, *i.e.* V_1, is thus composed of the amplified differential signal V_{DM}, and the amplified common mode V_{CM}. The output of **A2**, *i.e.* V_2, is composed of the amplified common mode V_{CM} and an intentional offset V_O of at least 10 mV. The amplifiers have to be designed so that noise is negligible compared to V_O, thus making the circuit noise tolerant. Then, by generating similar common-mode components in V_1 and V_2, they can be neglected if only the difference of V_1 and V_2 is taken into account. Besides, the proposed structure avoids using filters with different bandwidths by extracting separately differential and common modes, hence avoiding large capacitors. This is a significant advantage for scalability and integration purposes.

Identical low-pass filters (**LPF** in Fig. 2) are inserted after each amplifier to reduce 50 Hz residual frequency component, due to the lack of the reference elec-

trode. A threshold comparator is then used to compare V_1 and V_2 and generate the desired clock signal V_{OUT}. V_1 and V_2 having the same common mode, the differential signal V_{DM}, representing the presence of a heartbeat, is eventually compared to the offset V_O. V_O has to be set so that it is lower to the amplified R-wave:

$$|V_O| \leq |V_{DM}|. \tag{1}$$

When a heartbeat occurs, V_{DM} crosses V_O, the threshold comparator toggles and generates the desired pulse.

Finally, a self-calibration unit uses the system output signal V_{OUT} to adjust the offset V_O generated by amplifier **A2**. The obtained V_O has to respect the condition expressed in (1), so that the low-duty-cycled targeted clock signal is output at V_{OUT}. The calibration process is done once, off-line, at device start-up, since there is no need to change the threshold value while the device stays in the same measurement conditions.

The main advantage of the proposed structure is that the reference signal of the comparator is based on the common-mode voltage output of the amplifiers, so that only the differential voltage component between the 2 electrodes can be considered. As a result, in terms of amplifier design, the Common-Mode Rejection Ratio (CMRR) requirement is lowered compared to a single-amplifier structure where the same design is used for both differential signal amplification and common-mode attenuation.

However, since the proposed scheme relies on an identical common-mode gain in 2 distinct amplifiers, the local mismatch between similar transistors in **A1** and **A2** is to be addressed. For that purpose, it is mitigated at the layout level by placing matched transistors next to one another using interdigitated gates for connection. The self-configuration unit feedback loop ensures a correct behavior of the system despite the remaining transistor mismatch.

3 Circuit Design

3.1 Amplifier A1

The structure of the amplifiers used in this approach is a conventional 3-stage amplifier structure. It is composed of a differential pair and a gain stage. The electrical schematic of amplifier **A1** is shown in Fig. 3. For the differential pair, composed of M_{11} and M_{12}, the inputs are connected to PMOS transistors instead of the NMOS transistors to mitigate the $1/f$ noise. The gain stage, composed of 2 transistors in the conventional amplifier structure (M_{15} and M_{16} in Fig. 3), is doubled with the purpose of increasing the gain (addition of M_{17} and M_{18}). The body voltage of M_{17} is fixed and set to $V_{DD}/2$. For this application, there is no need for a high CMRR because the system does not need to be linear and detect all the components of the heartbeats. Thus, the design effort can be set on lowering the current consumption while still acquiring the R-wave with high precision. A CMFB circuit is added to the structure for stability and ensures operation at a fixed common-mode voltage for the first 2 stages. It presents the particularity to directly drive the body voltage of transistors M_{13} and M_{14}.

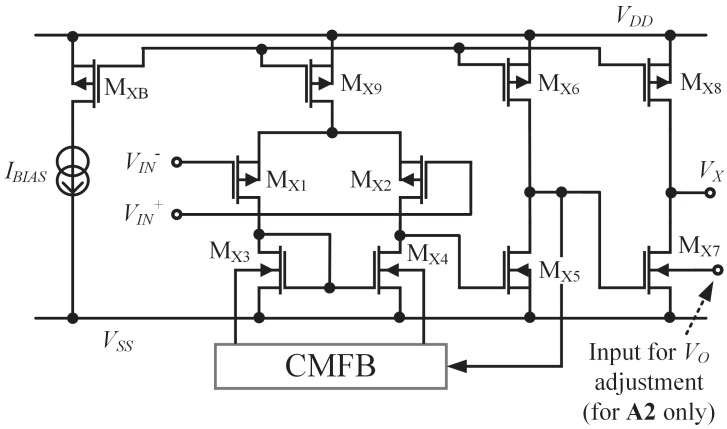

Fig. 3. Electrical schematic of the designed amplifiers **A1** and **A2**, including each a Common-Mode Feedback (CMFB) loop. The naming convention is $X = 1$ for **A1**, $X = 2$ for **A2**. In **A2**, the bulk of M_{27} is connected to the self-calibration unit for V_O adjustment.

3.2 Amplifier A2

Amplifier **A2** is designed using the same structure as in amplifier **A1**, shown in Fig. 3. Both CMFB circuits in **A1** and **A2** share the same voltage reference. However, in the last stage, the transistor M_{27} is modified so that the bulk voltage can be modified by the self-calibration unit, Fig. 3. For simplicity reasons, the possible range of M_{27} bulk voltage is from 0 V to V_{DD}. Increasing or decreasing this voltage will decrease or increase the output offset, respectively. This feature is therefore used to generate the additional offset V_O at the output of the amplifier.

3.3 Threshold Comparator

The designed threshold comparator is a conventional operational amplifier used as a comparator, as shown in Fig. 4. The differential gain of the amplifier is maximized so that the slightest difference between V_{IN}^+ and V_{IN}^- saturates the output V_{COMP} between V_{SS} and V_{DD}. Besides, the transistors' dimensions are designed to optimize the slew-rate, and thus the response rapidity of the comparator.

3.4 Self-calibration Unit

The self-calibration unit acts as the feedback loop for adjusting the offset voltage of **A2**, Fig. 5. It takes V_{OUT} as an input and charges the capacitor C_C with a constant current I_{CHARGE}, depending on the duty cycle of V_{OUT}. To calibrate the system, the resulting voltage V_C must be between 2 reference voltages V_{refL} and V_{refH}, defined externally depending on the user. If V_C is over V_{refH}, it means

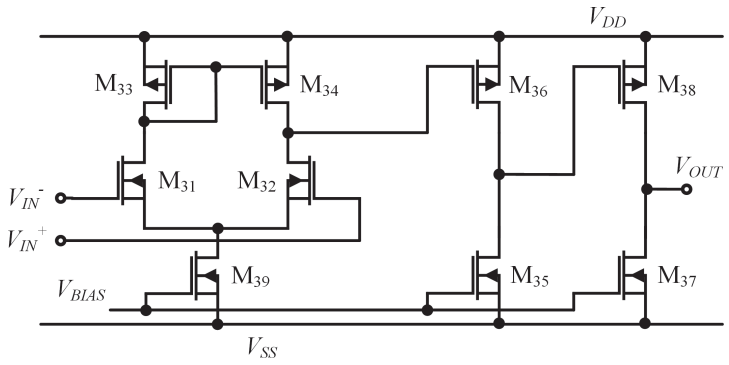

Fig. 4. Electrical schematic of the designed threshold comparator.

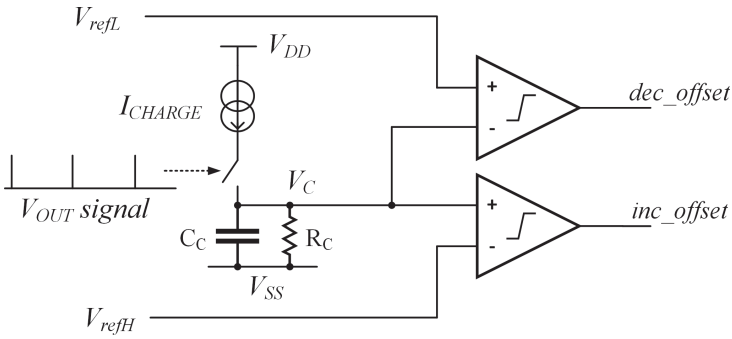

Fig. 5. Block diagram of the proposed scheme for the self-calibration unit.

that the offset component V_O is too low, and the signal *inc_offset* is set. If V_C is below V_{refL}, the signal *dec_offset* is set instead. The digital signals *inc_offset* and *dec_offset* are then used to command a charge pump circuit allowing to increase and decrease the body biasing of M_{27}, respectively. In addition, a resistor R_C is used to discharge the capacitor C_C. The passive components R_C and C_C can be implemented off-chip so that the resulting time constant can be adapted externally to each person's heartbeat. Once the value of V_O is calibrated, it does not need to change while the system is on-line, therefore the self-calibration unit can be put in sleep mode.

4 Results

4.1 System-Level Model

The proposed structure has been simulated using *Matlab*®, and the intermediate signals are shown in Fig. 6. The ECG signal is generated by the *ECGSYN* application from Physionet [6,13], 50 Hz coupling due to the absence of a reference electrode, Fig. 6-(a). Its amplitude and shape are similar to that of a

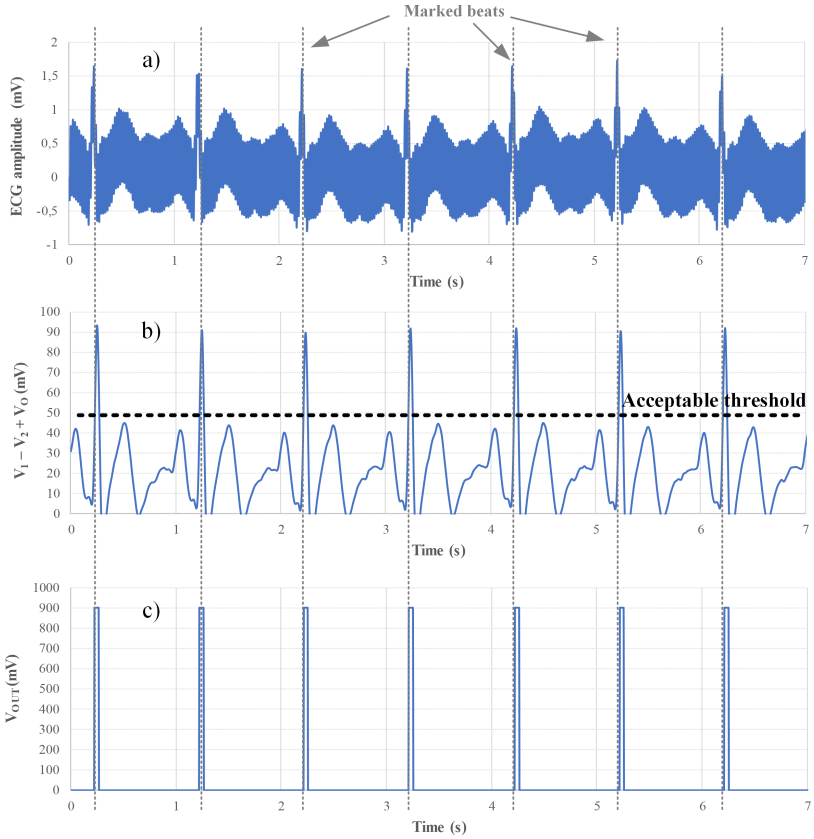

Fig. 6. Transient response of different voltages in the simulated system using *Matlab*®. a) Input signal at electrode #1, 50 Hz coupling. b) Difference between the signals V_1 and V_2 at the output of the amplifiers **A1** and **A2**, without taking the threshold V_O into account. An acceptable value of V_O is indicated on the graph. c) Output signal V_{OUT}.

measured ECG signal [13], sensed by both electrodes as they are next to each other. A random electrode conductivity is modeled, depending on the electrode material itself and its placement on the skin. The highpass filters **HPF1** and **HPF2** are designed to have a cut-off frequency 15 Hz, allowing the attenuation of motion artifacts and baseline wandering caused by the respiration [2]. The model includes a random variation of the passive elements values, extracted from transistor-level Monte-Carlo simulations. Moreover, a voluntary mismatch between the highpass filters capacitances is added to enhance the differences between the 2 input signals. Given simulation results, a 40% capacitance mismatch can produce a detectable differential voltage corresponding to the R-wave at the output of **A1**. However, a capacitance mismatch superior to 150% bring the filter cut-off frequency closer 50 Hz, and produces a differential voltage

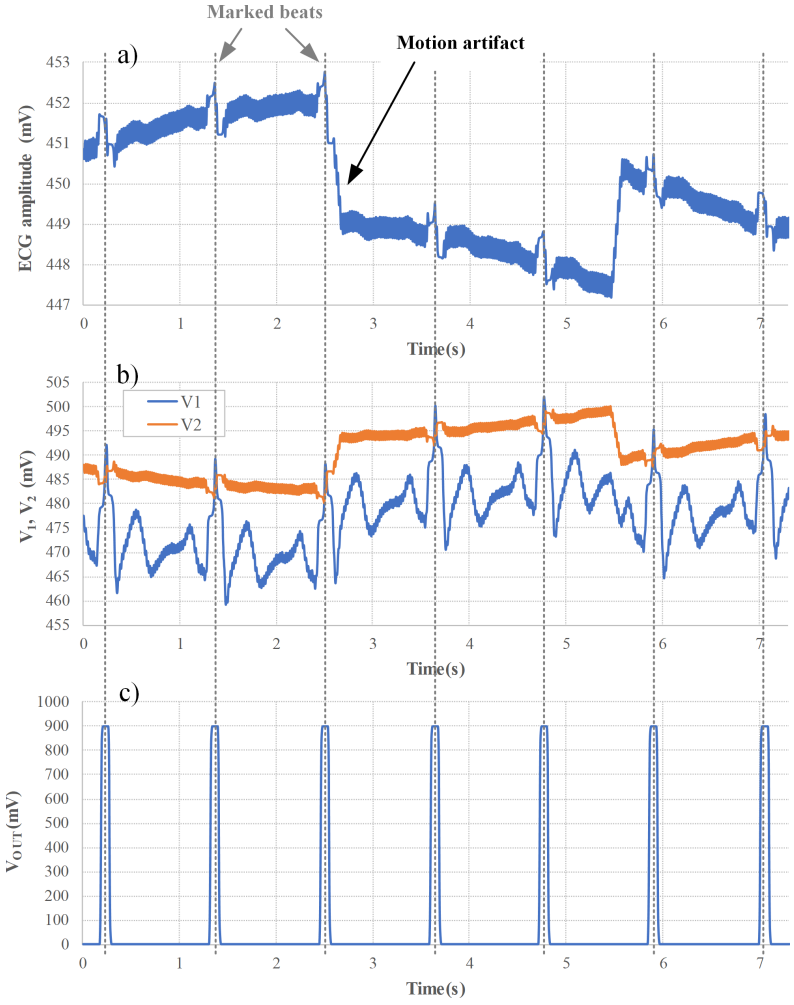

Fig. 7. Transient response of different voltages in the system simulated using *Spectre*®. a) Input signal at electrode #1, 50 Hz coupling, baseline drift and motion artifact. b) Intermediate signals at the output of the amplifiers **A1** and **A2**. c) Output signal V_{OUT}.

including also amplified environmental artifacts and not only the R-wave. The recovery of the heartbeat is not possible anymore. A capacitance mismatch of 100% is thus set for the behavioral simulations.

Amplifiers **A1** and **A2** are then modeled, with a differential gain G_D and a common-mode gain G_{CM}. The CMRR value of the amplifiers is derived from those 2 gain values. For a defined value of the CMRR, the model generates 100 ECG signals for statistical purposes, and tests if an acceptable value of the threshold V_O exists after the processing of each signal, as in Fig. 6-(b). If this value exists, a test is

considered a success and the signal V_{OUT} is output, Fig. 6-(c). Otherwise, the test is considered a failure. From the simulation, a minimum CMRR of 41 dB is needed to ensure a 95% success rate. This requirement is thus used to refine the amplifier design described in Sect. 3.1.

4.2 Transistor-Level Simulations

The circuit is designed using STMicroelectronics 28-nm FD-SOI CMOS. This technology process allows a fine tuning of the transistors back biasing, needed for previously described scheme. Besides, the 28-nm FD-SOI CMOS process allows efficient co-integration with advanced-pitch digital circuits for embedded processing using the heart-rate as a clock signal.

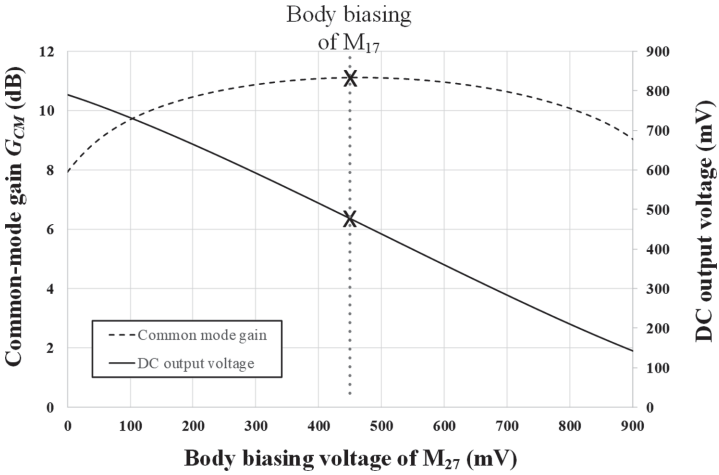

Fig. 8. DC response of the DC output voltage of **A2** depending on the body biasing voltage of M_{27}.

The circuit behavior has been simulated using *Spectre*®. The voltage supply V_{DD} is set to 900 mV. The current bias of the amplifiers I_{BIAS} is set to 2 nA, while the bias of the comparator is set to 1 nA. For transistor mismatch mitigation, the transistor lengths have been set to 3 times the minimal allowed length. The ECG signal is also generated by the *ECGSYN* application, and 50 Hz coupling, baseline drift and a motion artifact, using frequency components and amplitudes described in [2]. The obtained input wave is displayed in Fig. 7-(a). The outputs of both amplifiers **A1** and **A2**, V_1 and V_2, respectively, are shown in Fig. 7-(b). While the amplified common mode is still present in V_1 and V_2, the high differential gain G_D allows to extract the expected R-wave in V_1. As in Fig. 7-(b), the common-mode voltage reference allows reacting to the environmental perturbations. In the self-calibration unit, V_{refL} and V_{refH} are set so that the offset voltage V_O of V_2 is 16 mV. The output voltage of the heartbeat

detector V_C is shown in Fig. 7-(c). Considering the offset calibration, Fig. 8 shows that the DC output voltage of **A2** can be tuned in that range with a variation of the body biasing voltage of M_{27} that does not modify the common-mode gain G_{CM} of **A2**, thus enabling self-calibration without risking a behavioral change in the amplifiers.

The amplifiers consume 7.5 nW each, and the comparator consumes only 4.2 nW at 60 bpm. The system power consumption is 19 nW without taking into account the automatic offset calibration unit, since it is in sleep mode while on-line.

Since they are the most power-hungry part of the system, the characteristics of the amplifiers are compared with state-of-the-art ECG amplifiers, Table 1. In this work, even though the CMRR is far below that of conventional instrumentation amplifiers used for ECG detection [3,4,8,17], it is still sufficient for the application since signal reconstruction is not needed. Moreover, since the CMRR constraint is lowered, an ultra-low-power design can be envisioned for the amplifiers, yielding to a total power consumption reduction of more than 50% compared to an amplifier used for a similar application [8]. This system is thus suitable for near-sensor integration.

Table 1. Characteristics of state-of-the-art ECG amplifiers

	[4]	[17]	[8]	[3]	**This work**
Application	ECG recording	ECG recording	Single heartbeat detection	Single heartbeat detection	**Single heartbeat detection**
Technology process	65-nm bulk	0.35-µm bulk	0.18-µm bulk	0.18-µm bulk	**28-nm FD-SOI**
CMRR	>80 dB	>65 dB	68 dB	>50 dB	**48.9 dB**
Amplifier power consumption	64 nW	320 nW	50.4 nW	504 nW	**7.5 nW (x2)**
Self-adaptative detection threshold ?	No	No	No	Yes (92 nW)	**Yes (4.2 nW on-line)**

5 Conclusion

This work presents a low power circuit for wearable systems detecting the ECG signal and converting the heart rate into a digital signal. This solution permits waking up the sensors from time to time (e.g. once or twice per second), and consumes only 19 nW at a 900 mV supply voltage. The applications for this integrated circuit are in medical monitoring and more generally in high autonomy

wearable systems. Compared to state-of-the-art on-chip solutions, the structure of this circuit is simpler and self-adjustable, since there is no need to reproduce the exact shape of the signal. Thereby, a high CMRR is not required unlike in conventional instrumentation amplifiers, and the global consumption is lowered.

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