Full Swing Logic Based Full Adder for Low Power Applications

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Abstract. During the design of Application-Specific Integrated Circuits, a whole adder logic circuit plays a significant role. The full adder is a fundamental part of the majority of VLSI and DSP applications. Power consumption in full adders is one of the key factors; hence it is necessary to build full adders with low power consumption. Full adders are developed in this work employing full swing AND, OR, and XOR gates and compared with pass transistor logic (PTL) based AND, OR, and XOR gates, and complementary metal oxide semiconductor logic (CMOS) based AND gate, OR gate, and XOR gate. The Mentor Graphics Tool is used to construct and simulate every planned circuit. After receiving simulation data, we compared the power consumption, delay and PDP of several complete adder-based logic designs. In the proposed full swing XOR, the power dissipation and delay is decreased by 10.5% and 9.8% respectively and hence the full swing full adder PDP is decreased by 0.6%. As compared to alternative full adder designs based on logic, full swing by using gates like AND gate, by using the OR gate, and with the help XOR gate, full adder design consumes less power and hence suitable for low power applications.

Keywords: Full Adder · TGL · PTL · Mentor Graphics Tool

1 Introduction

The concept of smart cities has gained tremendous momentum in recent years as urban areas around the world strive to harness the power of technology to enhance the quality of life for their residents. Smart cities leverage various Internet of Things (IoT) applications and interconnected systems to efficiently manage resources, improve infrastructure, and deliver better services. One crucial aspect that underpins the success of smart city initiatives is the implementation of low-power solutions [1]. Low power plays a pivotal role in enabling the sustainable growth and long-term viability of smart cities, ensuring that these technological advancements are energy-efficient, environmentally friendly, and economically feasible.

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Adders are widely utilized as circuit components in Very Large Scale Integration (VLSI) systems, including microprocessors and Digital Signal Processing (DSP) processors. It serves as the hub for several other processes, including address computation, multiplication, and division. Adders are crucial to the overall system performance in most digital systems [2]. As a result, improving adder's performance is a key objective. The study into low power microelectronics has increased due to the tremendous rise in portable systems like laptops. The cause of this is because battery technology develops more slowly than microelectronics technology [3]. The mobile systems have a finite quantity of electricity at their disposal. Low power design has thus grown to be a significant design restriction [4]. The most computationally intensive applications, such as multimedia processing and DSP, may now be realized in hardware to increase speed of operation. However, as the market for portable electronics grows, so do the researchers' motivations to pursue smaller silicon areas, faster processing, longer battery lives, and improved dependability [5].

The complete adder design is crucial to digital computing. The complete adder design requirements are often several in natures. One of the properties, transistor count, affects the system complexity of arithmetic circuits like multipliers and Arithmetic Logic Units (ALU), among others [6]. The other two key factors in the design of complete adders would be power consumption and speed [7, 8]. Yet, their interactions with one another are paradoxical. To achieve the best design tradeoffs, energy usage per operations and power delayed products have been defined. The right choice of logic types can improve the performance of digital circuits. Various logical approaches frequently emphasize achieving one facet of performance at the price of another. While executing the identical function, the logic styles differ in how they calculate intermediary nodes and transistor counts [9].

Numerous comprehensive adders are designed so far, including those that use static CMOS, with the help of dynamic circuits, and having the large number of transmission gates, with the help of GDI logic, and having the pass transistor logic (PTL) [10, 11]. For the purpose of producing sum and carry outputs, the well-established static CMOS which are adders along with help of complementary pull up PMOS and having the pulling down NMOS networks that need 28 no. of transistors. PTL is a substitute for CMOS that offers implementations of the majority of functionalities with fewer transistors. This may lower total capacitances, increasing speed and reducing power dissipation in the process. The output voltage, however, varies in the PTL-based design because of a certain threshold voltage reduction occurs throughout the circuit input and the circuit output. The Complementary Pass Logic (CPL) and along with the differential restoring circuit that is Swing Restored PTL is a adaptations can be used to remedy this issue (SRPL). However, these logics lead to higher shorts of current, a greater transistors count, and more intricate wiring connections since they require complementary input signals [12].

Another strategy to reduce complexity in logic construction is to use transmission gates. Reference [13] discusses the entire adder implementation that makes use of a transmission gate. It takes 20 transistors; a transmission function adder, which only needs 16, is another option for additional transistor count reduction. Reference [14] discusses this option. As an alternative to CMOS logic, GDI logic is offered. A logic function may be implemented using this low-power design method with fewer transistors. A threshold

value V_t separates the output the result that comes maximum or minimum in the voltages from the V_{DD} that is the voltage which results the circuit to work or ground in GDI gates, resulting in a smaller voltage swing at the outputs [15, 16]. It is advantageous for power usage when the voltage swing is reduced. Nevertheless, if cascaded operation is used, this could result in sluggish switching. The reduced output may possibly result in circuit malfunction while operating at low V_{DD} [17].

In order to attain full swing functioning, additional consideration must be required. This work implements an effective technique for digital circuits, comprised of full swing by using gates like AND gate, by using the OR gate, and with the help XOR gate, and using the transistors like pass transistor logic, and by using the CMOS logic.

2 Ultra-Low Power Design Requirement

As smart cities evolve and integrate a multitude of IoT devices and systems, the demand for energy increases exponentially. These devices, such as sensors, actuators, and communication modules, form the backbone of a smart city infrastructure. They collect and exchange vast amounts of data, enabling city authorities to monitor various aspects of urban life, including traffic flow, waste management, energy consumption, and public safety. However, this increased reliance on technology and connectivity poses significant challenges, particularly in terms of power consumption.

1. Energy Efficiency: Smart cities need to optimize energy consumption to ensure sustainable development. By implementing low-power devices and systems, cities can minimize their overall energy footprint. Low-power solutions can significantly extend battery life, reducing the frequency of battery replacements or recharging [18]. This, in turn, reduces the operational costs associated with maintaining and powering the vast network of IoT devices deployed throughout the city.
2. Scalability and Expansion: A crucial characteristic of smart cities is their ability to scale and accommodate future growth. Low-power solutions enable the deployment of a larger number of devices without overburdening the existing power infrastructure [19]. By adopting energy-efficient technologies, smart cities can expand their IoT networks without straining resources or compromising system performance.
3. Environmental Sustainability: The environmental impact of urbanization is a growing concern worldwide. By incorporating low-power devices and systems, smart cities can contribute to reducing greenhouse gas emissions and minimizing their ecological footprint. Energy-efficient IoT solutions decrease the demand for non-renewable energy sources, leading to a more sustainable and eco-friendly urban environment [20].
4. Reliability and Resilience: In smart cities, maintaining the reliability and resilience of IoT systems is crucial for uninterrupted service delivery. Low-power devices can operate for extended periods without needing frequent maintenance, ensuring the continuous functioning of critical applications. Additionally, energy-efficient technologies are less susceptible to power outages, allowing smart cities to remain operational even during unforeseen events or emergencies [21, 22].

In the pursuit of building efficient and sustainable smart cities, low-power solutions have emerged as a vital enabler. By embracing energy-efficient technologies, smart cities can minimize their energy consumption, optimize resource allocation, and reduce their environmental impact [23]. Low-power devices and systems pave the way for scalable and resilient IoT networks, ensuring the long-term viability and success of smart city initiatives. As cities continue to evolve and adapt to the ever-changing technological landscape, prioritizing low power will remain essential in creating truly intelligent, energy-conscious, and livable urban environments [24].

3 Traditional Approach

3.1 XOR Gate using CMOS Logic

A two-input XOR gate is a fundamental digital logic gate that outputs true (1) when the number of true inputs is odd. The operation of a two-input XOR gate using CMOS logic involves the use of both NMOS and PMOS transistors. Dynamic power consumption occurs during switching when the output transitions between logic 0 and logic 1. During this period, both NMOS and PMOS transistors momentarily conduct, causing a short power surge. This causes a brief surge in power consumption, which can be significant in high-frequency operation or large-scale designs. The XOR gate's delay is primarily influenced by the cascaded structure of the inverters within the circuit. This can become a limitation in high-performance applications where ultra-fast operation is essential.

The power-delay product (PDP) represents the trade-off between power consumption and circuit speed. In high-performance systems, optimizing the PDP is crucial, and CMOS XOR gates may not be the most efficient choice. CMOS XOR gates require a relatively higher number of transistors compared to simpler gates like NAND and NOR gates. Each XOR gate needs 14 transistors, which can lead to increased chip complexity and area consumption [25]. In large-scale designs, the higher transistor count can contribute to increased manufacturing costs and may limit the overall chip integration. Due to the complex structure and cascaded nature of the XOR gate, its ability to drive multiple loads can be limited.

The CMOS XOR gates have proven to be versatile and widely used in many digital applications, they do have certain disadvantages, particularly concerning power consumption during switching, delay compared to simpler gates, and the number of transistors required. In some cases, a different gate implementation might be more suitable for achieving the desired balance between power efficiency, speed, and transistor count. The CMOS XOR gate circuit diagram is as shown in Fig. 1.

3.2 XOR Gate Using PTL

PTL XOR gates typically require fewer transistors compared to CMOS XOR gates, which can lead to a smaller silicon area and lower manufacturing costs. Due to the reduced transistor count, PTL XOR gates generally consume less power than CMOS XOR gates, making them more energy-efficient. PTL XOR gates have simpler transistor paths, leading to shorter signal propagation delays and faster switching times compared

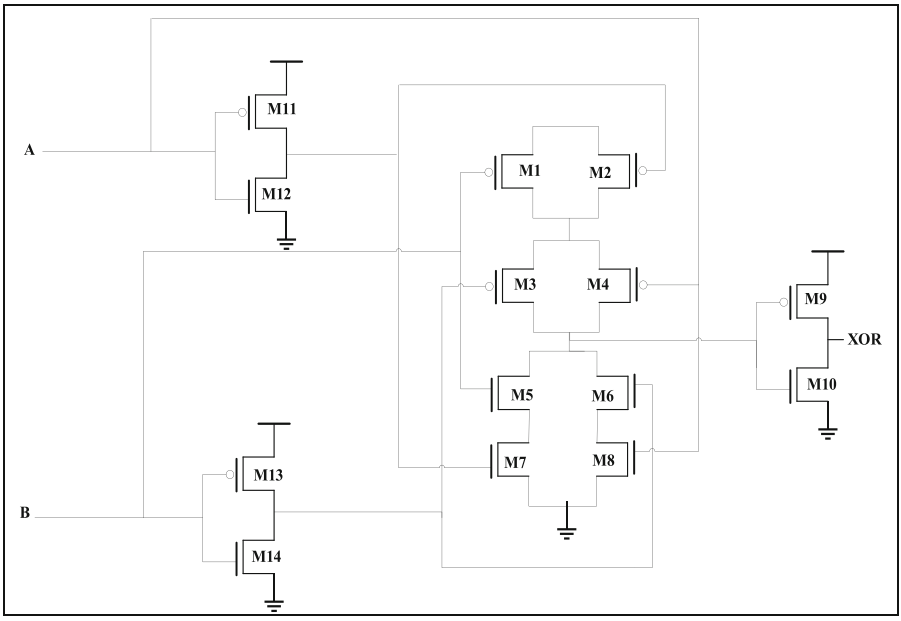

Fig. 1. Circuit schematic of XOR using CMOS logic

to CMOS XOR gates [26]. PTL gates can perform well at lower supply voltages, making them suitable for low-power and energy-constrained applications.

PTL XOR gates suffer from some signal degradation issues due to the presence of parasitic capacitance and resistance in the pass transistors, which can affect the circuit's overall performance. The noise margin (the tolerance for signal fluctuations) of PTL XOR gates is generally lower than that of CMOS XOR gates, making them more susceptible to noise and manufacturing variations. PTL XOR gates have a limited ability to drive multiple loads (fan-out), which can restrict their use in complex circuits with high fan-out requirements. The circuit schematic of XOR using PTL is represented in Fig. 2.

3.3 XOR Gate Using Full Swing Logic

The power consumption of the FA cell can be decreased by designing the XOR gate efficiently, as it is a major consumer of power. Additionally, there are various circuit proposals available for implementing an efficient XOR gate in digital circuits design. The full swing based XOR gate is shown in Fig. 3.

In Fig. 3, due to two NOT gates on the critical route, the double pass transistor XOR gate circuit, which comprises eight transistors, consumes a lot of power. The power dissipated in short-circuits and overall increases with the size of these transistors since doing so results in an intermediate node with a high capacitance. There is a minor increase in critical route latency under ideal PDP circumstances as well [27].

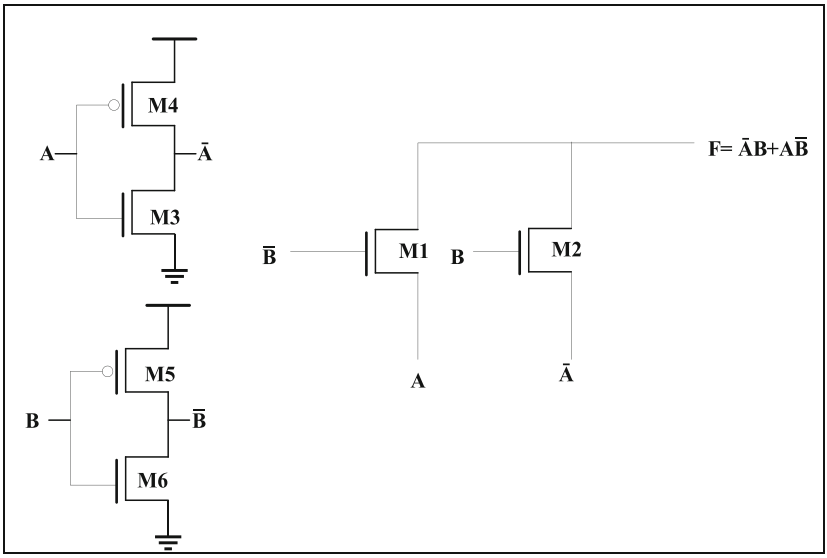

Fig. 2. Circuit schematic of XOR using PTL

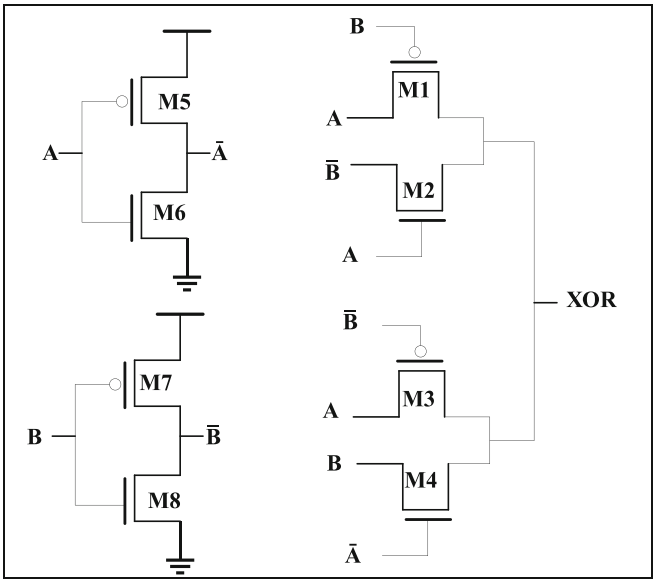

Fig. 3. Circuit schematic of XOR using FSL

Figure 4 shows The PTL logic-based XOR gate circuit, which consists of six transistors, has a better latency and power consumption than an alternative circuit. However, it employs NOT gates on the critical route, which might be problematic. Because an NMOS transistor was used in the XOR circuit, has less latency Because PMOS transistors are slower than NMOS transistors, not gates should be larger in order to maximize XOR speed [28].

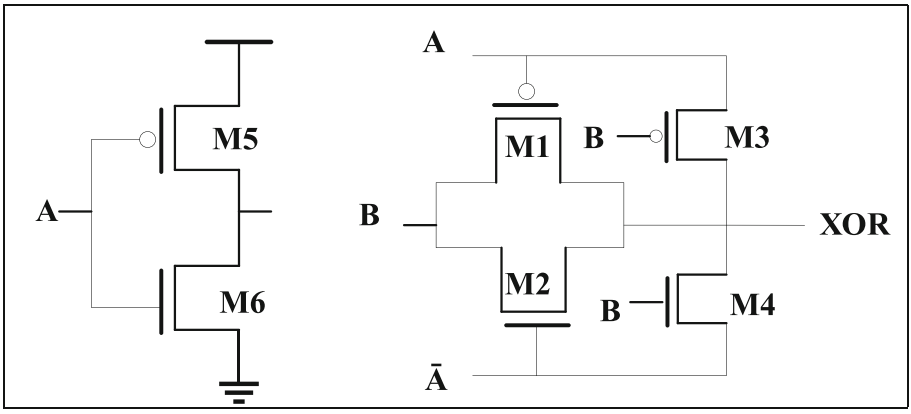

Fig. 4. Circuit schematic of XOR using full swing PTL

4 Proposed Methodology

The non-full-swing XOR circuit of Fig. 5 [29] is efficient in terms of the power and delay. Furthermore, this structure has an output voltage drop problem for only one input logical value.

To solve this problem and give the XOR gates an ideal shape; we propose the circuit shown in Fig. 6. This arrangement creates a perfect swing for all possible input combinations. In the critical route of the circuit, the proposed XOR gate does not contain a NOT gate. Compared to all other circuits, the delay is shorter and the drive strength this better. The proposed XOR gate has one more transistor than the structure shown in Fig. 4, but it operates faster and consumes less power.

The input capacitances in A and B of the XOR circuit depicted in Fig. 6 are not balanced because one of them has to be connected to the input of the NOT gate and the other to the diffuser of the NMOS transistor. As a result, input A, which is likewise linked to the NOT gate, has to be connected to a transistor with a lower input capacitance. Full-swing output, less wiring, good drivable capacitance and simple circuit structure of the proposed XOR circuits are their advantages.

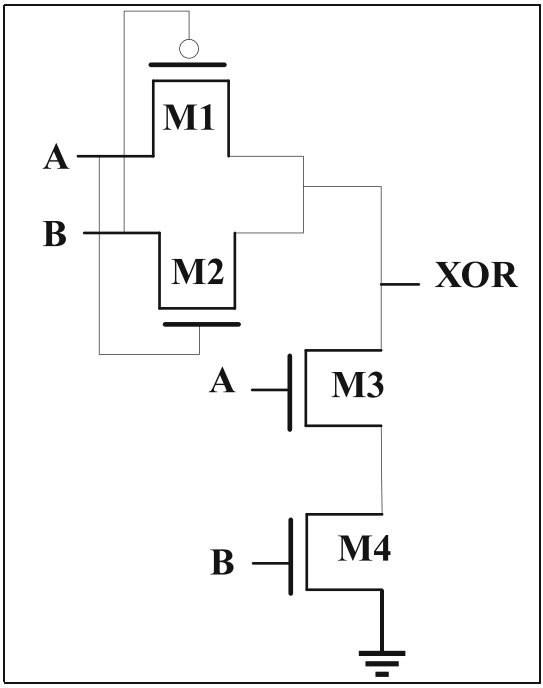

Fig. 5. Circuit schematic of non-full swing XOR

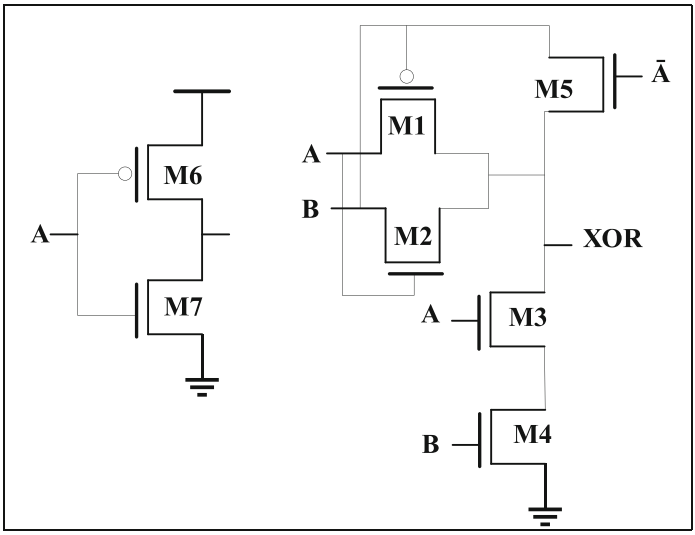

Fig. 6. Circuit schematic of proposed XOR using FSL

5 Design, Implementation and Simulation Results

The PTL XOR gate is designed using pass transistors as the main building blocks. It consists of transmission gates or pass gates that pass or block signals based on the control signals. The CMOS XOR gate is designed using Complementary Metal-Oxide-Semiconductor (CMOS) technology. It employs a combination of NMOS and PMOS transistors to create the XOR function. Full Swing Logic is a design style that enhances noise immunity and signal integrity. The XOR gate designed using Full Swing Logic combines the benefits of both PTL and CMOS techniques to achieve high performance.

Mentor Graphics provides a suite of electronic design automation tools. The design of the XOR gates (PTL, CMOS, and Full Swing Logic) is implemented using the appropriate tool from the Mentor Graphics suite. This involves drawing the circuit schematics, setting up the transistor models, specifying the technology parameters, and defining the logic function of the XOR gate.

After implementation, the XOR gates are simulated using the Mentor Graphics tool to verify their functionality and performance. The outputs waveform of every circuitry may be seen when all the circuitry have been constructed and modeled to use the mentor graphical tool.

5.1 Implementation of XOR Gate Using CMOS Logic

For CMOS XOR gate, the simulation will demonstrate its higher noise immunity, better signal integrity, and high fan-out capability. But it might exhibit increased power consumption and longer switching delays. Figures 7 and 8 depict the simulated design and waveforms of an XOR gate employing CMOS respectively.

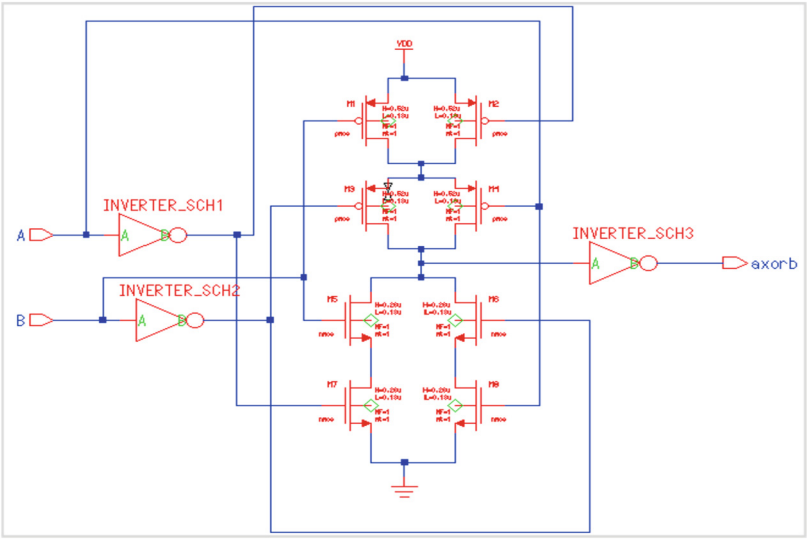

Fig. 7. Schematic for simulating XOR with CMOS

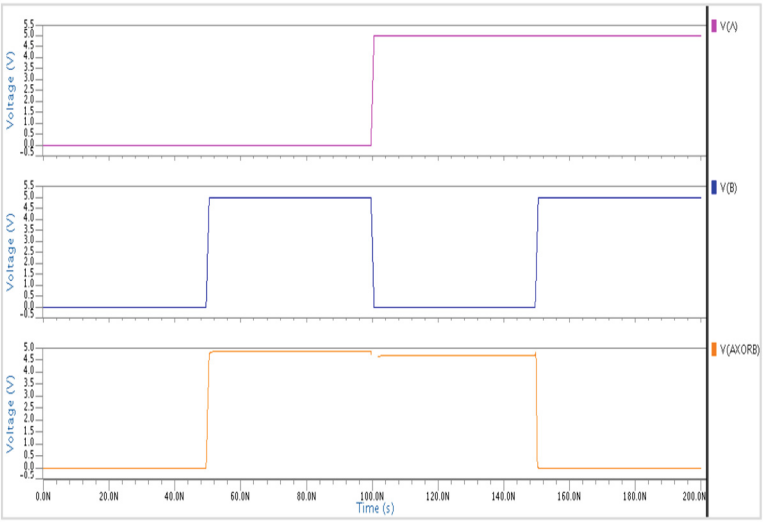

Fig. 8. Waveforms for simulating XOR gate with CMOS

5.2 Implementation of XOR Gate Using PTL

For Pass Transistor Logic (PTL) XOR gate, the simulation will validate its reduced transistor count, low power consumption, and faster switching speed. However, it may show limitations in noise margin and signal degradation. Figures 9 and 10 depict the simulated design and waveforms of an XOR gate employing pass transistors respectively.

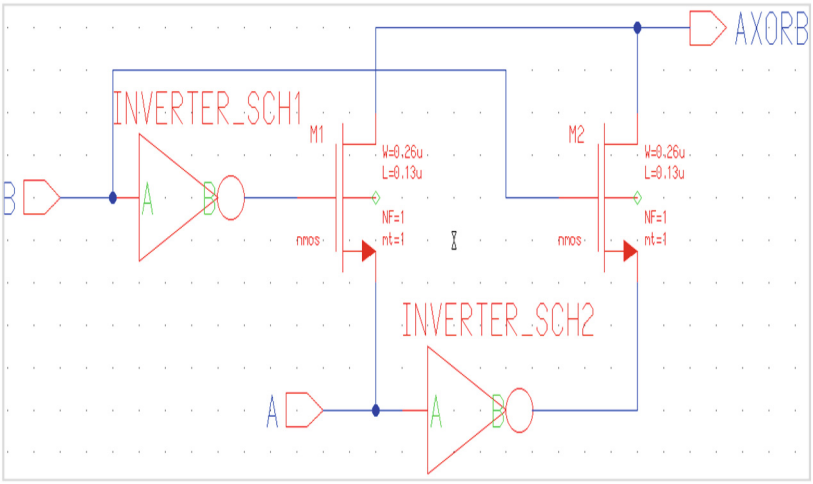

Fig. 9. Schematic for stimulating XOR gate with PTL

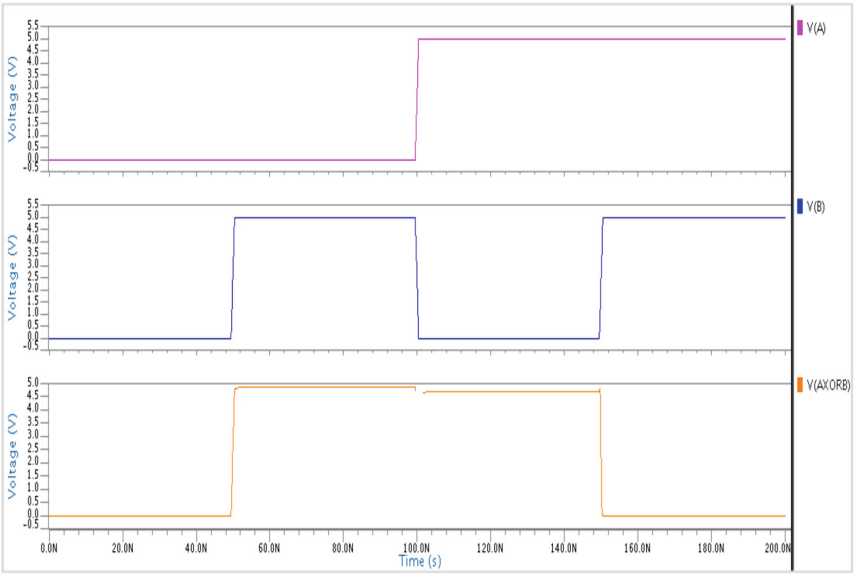

Fig. 10. Waveforms for stimulating XOR gate with PTL

5.3 Implementation of Proposed XOR Gate Using FSL

For full swing logic XOR gate, the simulation results will aim to show the advantages of combining PTL and CMOS techniques, such as improved noise immunity, signal integrity, and moderate power consumption. Figures 11 and 12 demonstrate the simulation design and waveforms for a XOR gate utilizing a full-swing XOR gate.

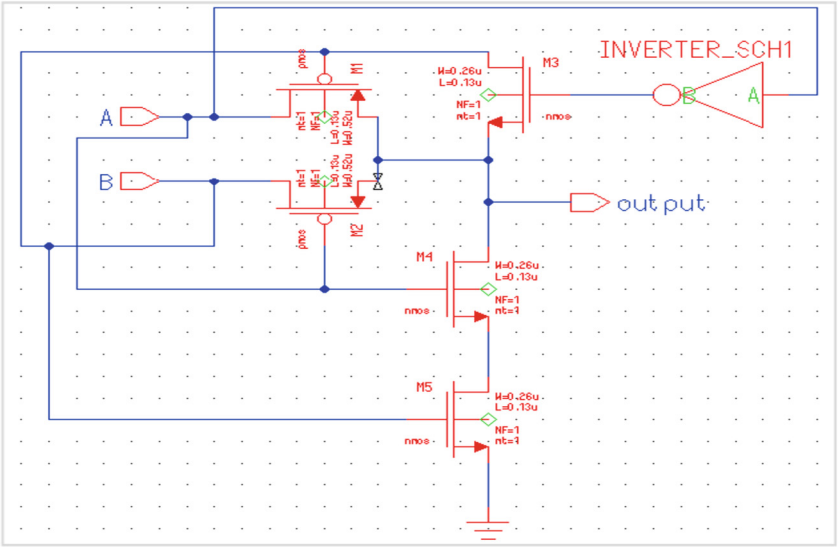

Fig. 11. Schematic for simulating proposed XOR with Full swing

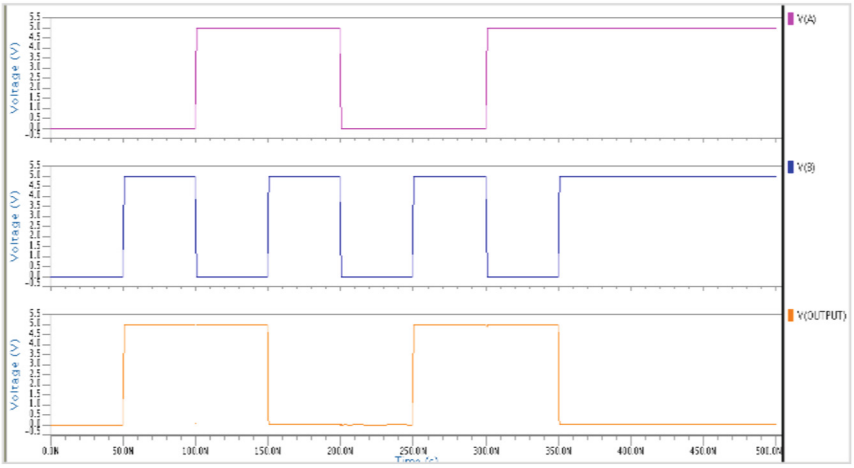

Fig. 12. Waveforms for simulating proposed XOR gate with Fullswing

The simulation results will include waveforms depicting the input and output behavior of each XOR gate, and they will be analyzed to evaluate the design's performance and adherence to specifications. Any design improvements or optimizations can be made based on these simulation results before proceeding to the physical fabrication process.

5.4 Implementation of Full Adder Using Proposed XOR Gate

The CMOS Full Adder is designed using CMOS technology, utilizing a combination of NMOS and PMOS transistors to perform addition. The PTL full adder is designed using pass transistors, and it performs addition using XOR gates and other logic gates implemented using pass transistors. The Proposed Full Swing XOR gate is a novel design that aims to combine the benefits of Pass Transistor Logic (PTL), CMOS Logic, and Full Swing Logic to achieve improved performance, including high noise immunity, low power consumption, and faster switching times.

The full adders (PTL full adder, CMOS full adder, and proposed full swing XOR gate full adder) are implemented using the Mentor Graphics tool suite. The tool is utilized to draw the circuit schematics, set up the transistor models, define the logic functions, and specify the technology parameters for each Full Adder design. Figure 13 depicts the full adder simulator design.

Each full adder design is simulated using the Mentor Graphics tool to evaluate its functionality and performance. The proposed full swing XOR gate used within the full adder is compared to the other three designs (PTL, CMOS, and full swing logic) in terms of noise immunity, power consumption, switching speed, signal integrity, and other relevant parameters. Simulation waveforms show the input-output behavior of each Full Adder, allowing for a detailed analysis of their respective performance. Figures 14, 15, and 16 illustrate, respectively, the simulated waveforms for full adders utilizing CMOS logic, pass transistor logic and proposed full swing circuitry.

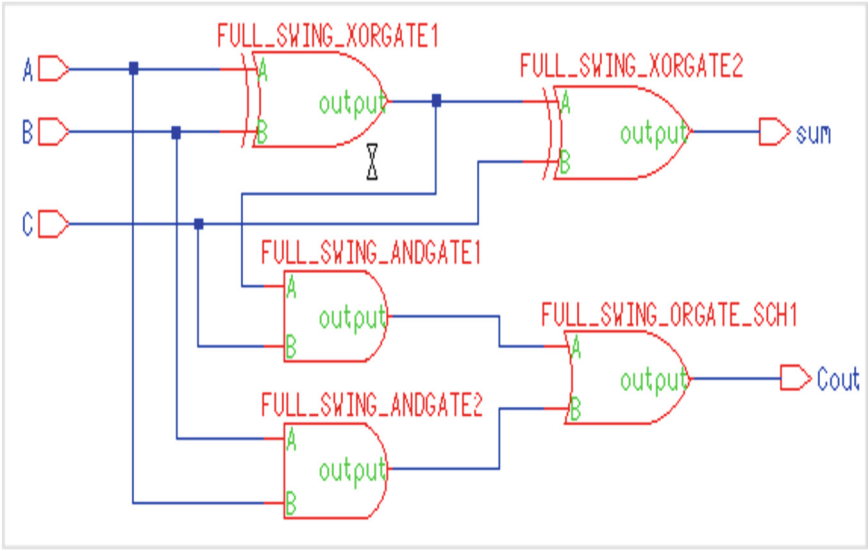

Fig. 13. Schematic of full adder using proposed full swing XOR gate

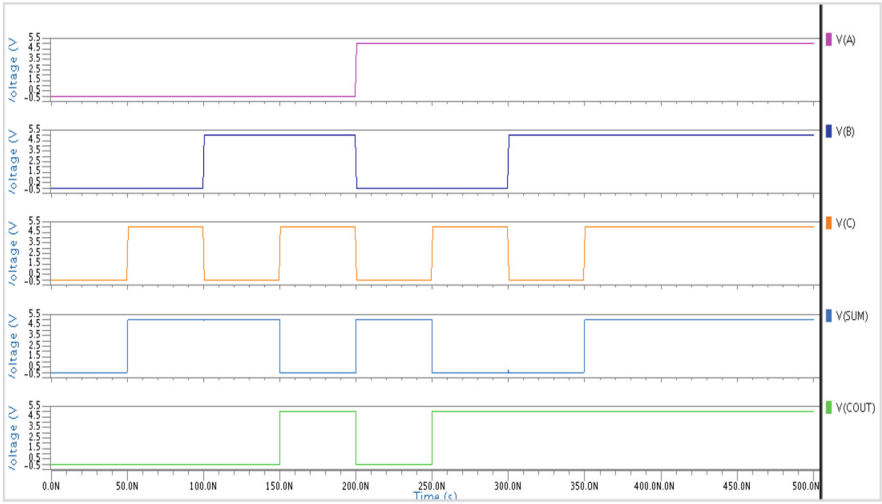

Fig. 14. Waveforms for simulating full adder with CMOS logic

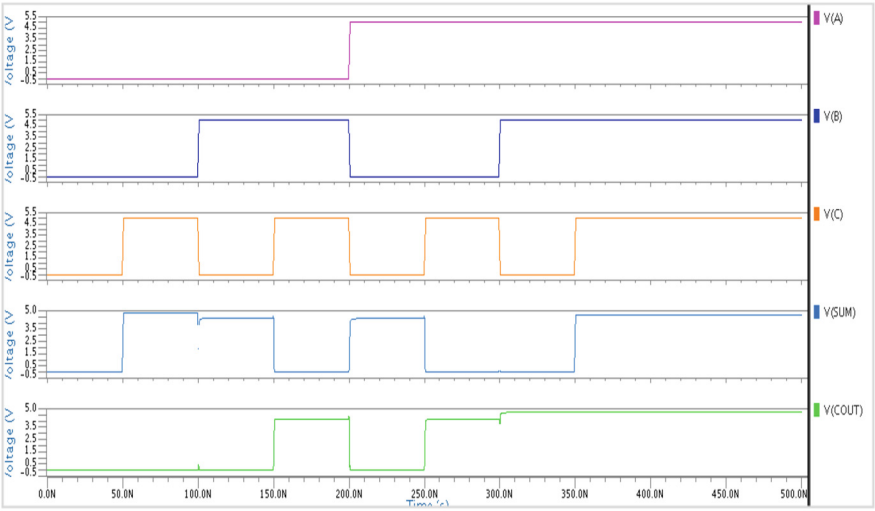

Fig. 15. Waveforms for simulating full adder with PTL.

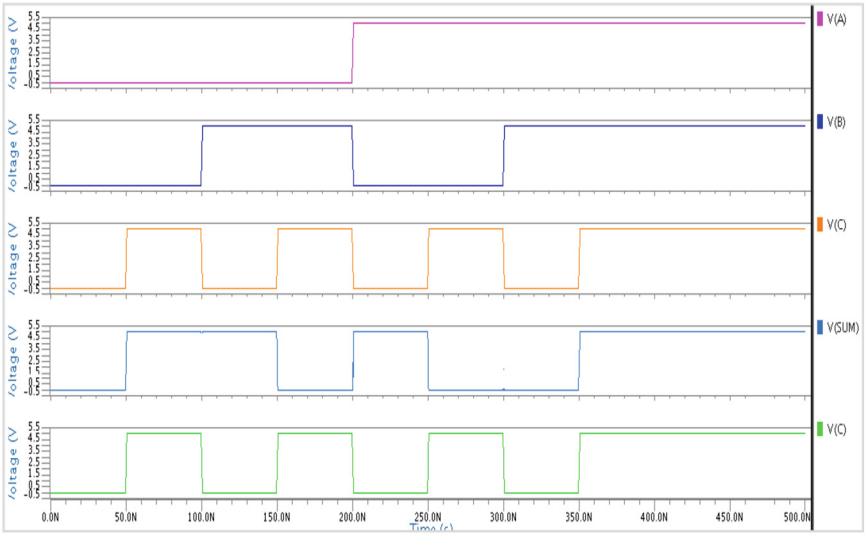

Fig. 16. Waveforms for simulating full adder using proposed full swing XOR gate

6 Performance Evaluation

The Proposed Full Swing XOR gate combines various logic techniques to achieve better noise immunity, making it more robust against signal disturbances and manufacturing variations. The proposed Full Swing XOR gate strikes a balance between the low-power advantages of PTL XOR gates and the power efficiency of CMOS XOR gates, offering moderate power consumption. While Full Swing XOR gates may not be as fast as PTL

gates, they generally provide faster switching times compared to CMOS XOR gates. In regards to power consumption,delay and PDP, the following Table 1 compares several XOR gate designs.

Table 1. Performance evaluation of XOR gates in various logics

XOR Designs	No. of Transistors	Power Dissipation (μW)	Delay (pS)	PDP (aJ)
Ref [24]	14	2.48	26.1	64.7
Ref [11]	6	2.14	23.6	50.5
Ref [27]	4	2.46	21.5	52.9
Ref [12]	8	2.50	25.8	64.5
Ref [30]	8	2.48	24.3	60.2
Proposed	**7**	**2.22**	**21.9**	**48.6**

The simulation results are compared to identify the strengths and weaknesses of each Full Adder design. The Proposed Full Swing XOR gate's impact on the overall performance of the Full Adder is evaluated, and it is compared against the traditional PTL, CMOS, and Full Swing Logic implementations. The comparison aims to demonstrate how the proposed Full Swing XOR gate enhances the Full Adder's performance, potentially providing advantages in various aspects over the other logic designs. Comparing several full adder designs in regards to power dispersion, delay and PDP is shown in Table 2 below.

Table 2. Performance evaluation of Full adder using XOR gates in various logics

XOR Designs	Power Dissipation (μW)	Delay (pS)	PDP (aJ)
CMOS [7]	3.61	212	765.3
DPL [16]	4.89	98.8	483.1
CMOS [11]	3.98	119.2	474.4
CPL [8]	6.88	63.7	438.3
HFA [12]	3.71	116.8	433.3
Proposed	**3.92**	**109.9**	**430.8**

Based on the simulation results and comparison, designers can make informed decisions about which Full Adder implementation is most suitable for their specific application. Any design improvements or optimizations can also be made based on the findings before moving on to the physical fabrication process.

7 Conclusion

In this work, the use of a full swing logic-based full adder that incorporates the proposed full swing XOR gate offers significant advantages for low-power applications. This design aims to strike a balance between power efficiency, speed, and performance, making it well-suited for energy-constrained systems. The proposed full swing XOR gate demonstrates notable improvements in power consumption compared to conventional adders. It showcases competitive switching speeds in comparison to PTL and CMOS-based full adders. Its design principles emphasize fast signal propagation and reduced signal degradation, contributing to improved delay performance. It also excels in achieving a favorable Power-Delay Product. It balances power consumption and delay characteristics, offering an optimal compromise between energy efficiency and speed for low-power applications. These adders can be used for efficient and high-performance arithmetic circuits suitable for battery-powered devices, IoT applications, and other low-power electronic systems.

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