Space-Borne Multifunctional Integrated Hardware Processing Platform Design

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Abstract. This paper presents a design scheme of space-borne multifunctional integrated hardware processing platform. This platform is characterized by low power consumption, small size and light weight. At the same time, the scheme has the feature of reconfiguration, which maximizes the function of software. Different software is loaded according to different application to build hardware platforms for satisfying requirements in different environments. It provides a new way to solve the problem of traditional hardware specialization, which is the trend of hardware platform in the future.

Keywords: Multifunctional · Universal · Configuration · Hardware platform

1 Introduction

With the rapid development of microelectronics, computers, signal processing and other technologies, as well as the wide application in the field of satellite communications, the requirements for multifunctional and universal hardware platform have increased significantly [1–3]. The traditional hardware processing platform generally has the characteristic of specificity. It develops specific hardware platform for specific application scenarios, and its functions have been solidified to meet specific requirements. At the same time, when the functional requirements of users in orbit change, the product will not be replaced, and these problems have seriously restricted the development and application of the product. In order to solve these problems of satellite traditional hardware platform, it is necessary to study a hardware architecture platform with versatility, flexibility and freedom to upgrade. Secondly, it is necessary to build a high-performance digital signal processing platform that is suitable for a variety of needs. Third, the development of low power consumption, miniaturization, lightweight characteristics of hardware architecture. These requirements greatly heighten the implementation difficulty of the hardware platform.

At present, the concept of new software radio technology partly solve the problem that the functions can't be changed or upgraded, and gets rid of the traditional design method [4–8]. It is based on general and re-configurable hardware platform through loading software. Thus various functions can be implemented on a single platform. Although

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the new software radio platform has many advantages, such as re-configurable, openness and extensible feature, there are also some problems. The integration degree of platform is relatively low, the power consumption is high, and the volume is big. So the platform can not adapt to the characteristics of miniaturization and lightweight. How to design a more compact signal processing architecture is a very important issue.

In order to solve the above problems, this paper proposes a design scheme of space-borne mufti-functional integrated hardware platform to realize the characteristics of lower power, miniaturization and light weight. This platform also has the characteristic of reconfiguration which can load different software programs according to different functions. This paper provides a new idea and method which is the trend of future hardware platform.

2 Overall Design of New Hardware Platform

Traditional hardware platform include ADC, DAC, FPGA, DSP, CPLD, peripheral storage and interface chips. The main problem is that area and power consumption will be increased sharply. The overall design of traditional hardware platform is as follows (Fig. 1).

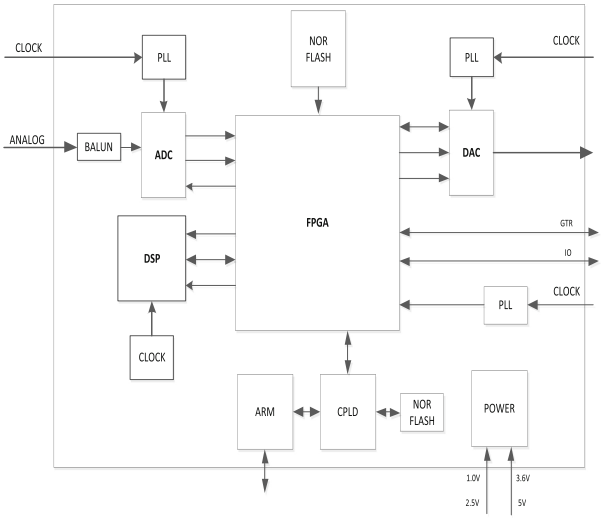

Fig. 1. Traditional hardware processing platform solution

This new space-borne mufti-functional integrated hardware platform is include RFSoc, DSP, DDR4, interface chips and so on. The overall design of new platform is as follows (Fig. 2).

The RFSoc chip selected for this hardware platform is equipped with dual-core ARM Cortex-A9 processor [9–12]. The processor has 6.25M logic units, more than 2000 DSP. In addition, four 16-bit DDR4 devices are integrated on the platform to provide high-bandwidth interfaces for ARM and FPGA logic resources in the RFSoc chip. And it can

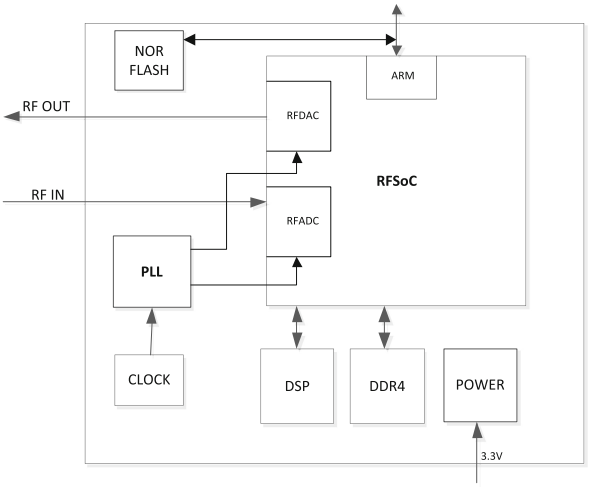

Fig. 2. Multifunctional integrated hardware processing platform

realize heterogeneous processing between ARM and FPGA. It is the most comprehensive and extensible hardware platform with the highest performance.

2.1 Direct RF Sampling Design of New Platform

The RF signal are converted to IF signal by one or two analog down-conversion which is traditional method. Then the IF signal is sampled by ADC. The traditional RF front requires a relatively complex design scheme with many discrete analog devices. And down-conversion circuits include mixers, oscillators, band-pass filters and so on, all of these requiring the specific design. Moreover, if the receiving frequency is variable and the bandwidth of filter can be set, the volume of the system will increase. This architecture can not satisfy the needs of miniature and lightweight.

In order to solve this problem, the new platform designed in this paper adopts the direct RF sampling technology. It moves the A/D and D/A as close to the antenna as possible. It has the advantages of less devices required, low cost, low power consumption and easy to obtain higher performances. It has great significance to the miniaturization, integration and low power consumption of equipment.

The selected RFSoc devices in the platform can directly sample the incoming and outcoming RF signals of frequency band below 6GHz. After the signal is digitized, digital signal processing technology is used to perform down-conversion and other signal processing in digital domain. Moreover, RF-ADC/RF-DAC integrated in RFSoc support a high sampling rate, which can better balance between dynamic range and SRN. The schematic diagram of integrated direct sampling subsystem in shown in Fig. 3. By eliminating the analog devices and adopting integrated method, the power consumption and packaging are reduced by nearly 50%–75%. At the same time, the development cycle of the whole system is greatly reduced.

Subsystem include mixer, CNC oscillator, extraction, interpolation, gain/phase compensation and other digital signal processing techniques for each channel. In addition,

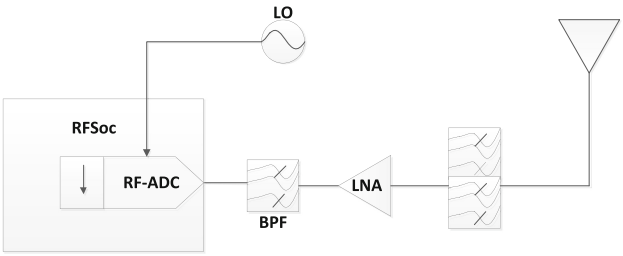

Fig. 3. RFSoc based RF sampling principle block diagram

RFSoc can meet the sampling requirements of different frequency points and bandwidth. In the RF range, the RF sampling clock can be tuned according to frequency. Therefore, the platform can respond quickly to changes in the external environment.

If other RF direct sampling chips on the market, such as AD9003 and AD9371, are adopted, the digitized signal are sent to FPGA must through JESD204B interface based on high-speed SERDES. This is because with the continuous improvement of the sampling rate of ADC/DAC, the data throughput is getting lager and lager. And the data throughput rate is often several Gbit/s. It is difficult to meet the design requirements with the traditional LVDS, so the manufacturers of high-speed ADC/DAC devices adopt JESD204B interface.

However, the IP core of JESD204B interface standard is not only expensive, but also has very high requirements for the design of high-speed data line of the circuit board. At the same time, it will increase the circuit delay and design complexity of up to 80 sampling cycles. Meanwhile, it is difficult to debug, and the power consumption is large up to 8 W. Therefore, in order to solve these problems, it is necessary to remove the JESD204B interface. The platform scheme proposed in this paper breaks through the bottleneck of JESD204B and solve these problems. Because RFSoc used in this scheme integrates high-performance ADC/DAC, it is unnecessary to use the IP core of JESD204B and it also reduces the complexity of wiring on the circuit board.

2.2 High Integration Design of the Platform

In this deign RFSoc has sixteen channel transceiver. It is obviously that the new platform does not need extra ADC/DAC, ARM controller and power conversion chips correspond to these devices. Therefore, it also reduces the difficult of distributing the printed board and difficulty of dividing the power plane layer.

RFSoc, the core chip of the whole processing platform, integrates processing system and programmable logic resources. The processing system includes application processing unit (APU), real-time processing unit (RTU), DDR controller, system controller, security module, platform management module and various common interface management. Programmable logic resources include RF signal chain, common I/O, storage module and DSP resources. The core idea of space-borne multifunctional integration platform is to integrate FPGA + ARM + RF sampling as much as possible.

2.3 Multi-core Processor Chip Selection

DSP processing chip uses TMS320C6678, including a total of eight DSP kernel. The chip uses the keystone structure which can carry out high-performance fixed-point operation and floating point operation. The kernel speed of TMS320C6678 can reach 1.25 GHz. Thus the whole chip can provide 10 GHz operating frequency.

TMS320C6678 not only provides powerful operation ability of up to 9600MIPS, but also integrates a variety of digital signal interface, including EMIF, GPIO and SRIO interface. SRIO can realize the high-speed data transmission between DSP and FPGA, which to some extent can meet the requirements of the high-speed real-time signal processing and transmission. TMS320C6678 is used to execute a one-million-point FFT under the operating frequency of 1 GHz. It takes only 6.4 ms for 8 cores to run simultaneously. Such high-speed DSP kernel can be fully used to perform high-speed real-time computation, such as radar and electronic warfare.

The development flow of platform based on TMS320C6678 in shown in Fig. 4 below. Specifically, the signal processing process is firstly built based on the signal processing requirements and set module parameters, connection parameters and hardware parameters. Then the signal processing module is mapped to the C6678 hardware platform to generate the C6678 code. After that, the project code is compiled, loaded and debugged. If it does not meet the requirements of the system design, the above steps are executed again.

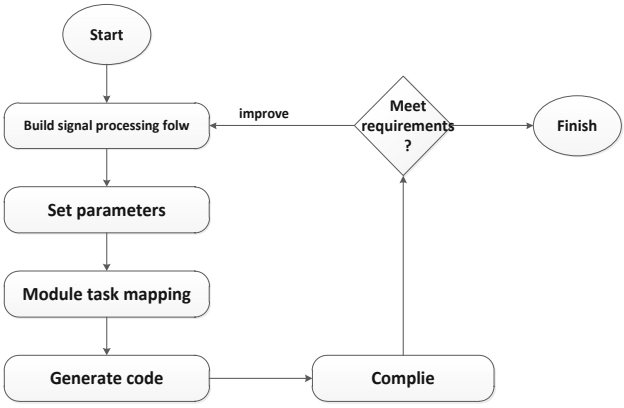

Fig. 4. TMS320C6678 based development process

2.4 Power Module Design of Platform

The power supply of RFSoc is the most complex part of the processing system. As shown in the Fig. 5 below, there are as many as fourteen power types. The selection and design of power module is an important factor that restricts the size and weight of the platform. For decrease the volume of platform, LINTER power modules are selected in this paper. LTM4650 has two power channels, each 25 A. And the two channels of LTM4650 can

parallel to obtain 50 A ability. The size of it is only 16 mm × 16 mm. Another power module of LINTER is LTM4644, which has four power channels, each 6 A. LTM4644 is also used in this new platform and the four channels of LTM4644 can parallel to obtain 24 A ability. The size of it is only 9 mm × 15 mm. The new platform has two LTM4650s and four LTM4644. These power modules can provide the complete power scheme for RFSoc, DSP, DDR4 and other chips.

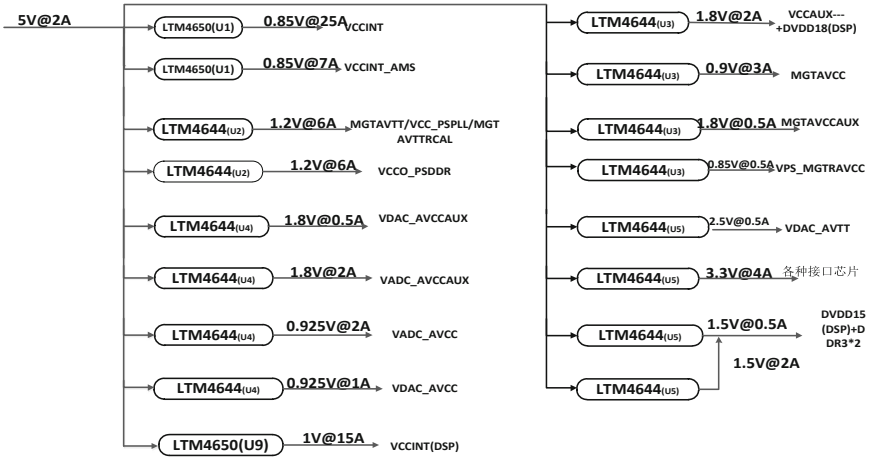

Fig. 5. RFSoc power supply type

3 Performance Analysis of Platform

3.1 Lightweight Analysis of Platform

The new platform already consider the module architecture, implementation of the different applications and various interfaces. And the platform choose high integration, low power consumption and strong processing capacity of the chip, in order to support the establishment of a lightweight.

At the same time, in order to make the processing platform universal, RFSoc is selected. RFSoc integrates RF-ADC, RF-DAC, ARM, FPGA and high-speed interfaces. So the hardware platform in nearly half the size. The input RF frequency of RFSoc can reach 6 GHz. If the input RF frequency is below 6 GHz, the mixer, oscillator, bandwidth is no needed. It greatly reduces the power consumption, size and development cycle of entire system.

3.2 Low Power Consumption of Platform

In the new platform, the power consumption of the DSP is estimated at about 10 W. And the core voltage of RFSoc is 0.85 V, the static current is less than 2.5 A, and the static

power consumption is less than 2.1 W. When the program runs, the power consumption of RFSoc is less than 25 W. So the total power consumption of processing platform is less than 35 W. When the power conversion efficiency is 90%, the total power consumption is less than 40 W.

Using Xpower of Xilinx, the current of RFSoc voltages can be calculated. When using XCZU49DR, for example, working at 25 °C, we can set the utilization rate of LUT to 70%, BRAM to 50%, DSP to 50%, parallel processing rate to 250 MHz, DDR3 interface to 36 bit, operating clock rate to 1333 Mb/s. Under this condition, RFSoc static consumption current is nearly 2.0 A. Operating at 25 °C, the temperature of thermal resistance is 69.6 °C and the power consumption of 22 W. RFSoc power consumption varies with the junction temperature. When the junction temperature changes from 10 °C to 100 °C, the chip's power consumption changes from 20.97 W to 25.01 W.

When using the traditional hardware platform, the power consumption is much greater than 40 W if the processing capacity is to be achieved similar to that of the new platform proposed in this paper. The power consumption of 16-channel ADC alone has reach more than 30 W.

3.3 Reconfiguration of Platform

RFSoc and DSP are the main components of hardware platform, which can realize different functions by loading different programs. By storing different software packages and corresponding control instructions, users can switch processing tasks.

The re-configurable characteristics of the hardware platform are shown in the Fig. 6 below. The numerical control method can adjust the frequency band of filter, and the SPI control method can change the gain amplitude of the RF signal. Sampling clock and NCO clock are adjustable.

The programmable logic devices and DSP devices are controlled and configured by the control unit to realize the desired functions. Algorithmic programs with different processing flows can be configured according to applications.

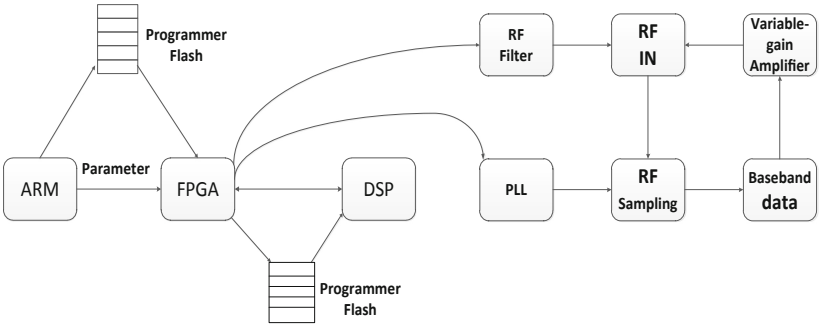

Fig. 6. Hardware processing platform re-configurable design

3.4 Deep Learning of Platform

In this design, the RFSoc is used to implement the deep learning algorithm. Firstly, the selected neural network structure type and deep learning framework are determined according to relevant tasks. Second, the network training is completed on the PC, so that the accuracy of the network meets the expected requirements. Third, the specific architecture of the deep learning model is determined and the neural network IP core is written by using high-level comprehensive tools. Fourth, a neural network computing engine matching the trained deep neural network is constructed on the RFSoc. Finally, the program running on the ARM within RFSoc is written to test the whole classifier.

According to the results analysis of hardware and software co-design during the implementation of deep learning algorithm model based on RFSoc, the acquisition of target data and weight data, the post-processing of the prediction results of deep neural network, the data scheduling and other control parts can be put into the processing unit (PS) part of the RFSoc hardware platform. The convolution of neural network, which contains a large number of multiplier and parallel computing, is implemented in the powerful programmable logic part (PL). The processing platform mainly includes external memory DDR4, processing unit (PS), on-chip cache, programmable logic (PL), and bus interconnection. Among them, the PS is responsible for data scheduling of the whole neural network and the PL is responsible for neural network acceleration. The overall architecture of deep learning model based on RFSoc is shown in Fig. 7.

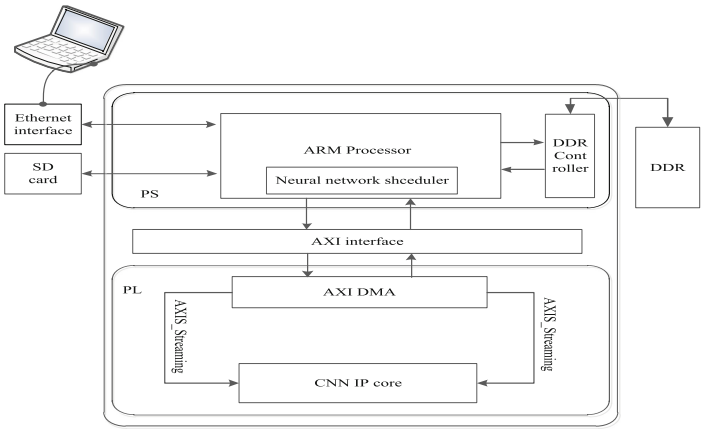

Fig. 7. The overall architecture of deep learning model

4 Conclusion

In this paper, a design scheme of space-borne multifunctional integration platform is presented. The platform has the ability of direct RF sampling and high-speed data processing. At the same time, the platform is characterized by low power consumption,

small size, light weight and reconfiguration. It provides a new way to solve many problems of traditional hardware platform. Therefore the designed platform can be widely used in aerospace equipment, which can greatly reduce the hardware cost of the upgrade system and can improve the data processing capacity.

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