Design of Cross Language Education Resource Sharing Platform Based on Hadoop Framework

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Abstract. The rapid development of information technology has promoted the modernization of cross language educational resource sharing. Educational resource sharing platform is the platform basis for carrying out distance education activities, which is of great significance to the development of modern distance education. Firstly, the hardware design of cross language education resource sharing platform is carried out, and the MCU controller is designed to play a powerful control function combined with FPGA system. The design is based on resource reconfiguration port and external input port to realize hardware connection. Then, the software design of cross language education resource sharing platform is carried out, the resource sharing algorithm based on Hadoop framework is optimized, and the multi line sharing ability of resource sharing algorithm is enhanced. The data model is designed to realize the design of shared platform. Finally, the platform test verifies that the response time of the platform is less than 4000 ms.

Keywords: Hadoop framework · Cross language · Educational resources · Resource sharing

1 Introduction

The ten year development plan for educational informatization (2011–2020) of the Ministry of education puts forward the guiding ideology of "narrowing the digital divide in basic education and promoting the sharing of high-quality educational resources", and puts forward the action plan of "action for the construction and sharing of high-quality digital educational resources", including the construction of a national public service platform for digital educational resources, the construction of all kinds of high-quality digital educational resources at all levels Establish a mechanism for co construction and sharing of digital education resources [1, 2]. However, in the informatization process of basic education, on the one hand, there is a serious shortage of high-quality educational resources in rural schools, and the contradiction between people's demand for educational resources and the insufficient supply of educational resources is prominent; On the other hand, in the existing resource sharing construction, the software and hardware resources are invested repeatedly, and the resource sharing is poor". The emergence of cloud computing technology provides a feasible solution to the problem of digital education resource sharing. Relying on thousands of cloud servers on the cloud education

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platform, it has extremely powerful computing functions, massive network resources, repeated construction, platform operation and maintenance, security and other problems existing in the existing resource sharing construction will be solved, It can save the cost of Digital Education Resource Sharing Construction [3, 4], promote the integration of urban and rural digital education resources and strengthen resource sharing.

Digital educational resources refer to multimedia teaching materials that can be operated under the multimedia computer and network environment after digital processing, such as media materials, question bank and test paper materials, teaching courseware, cases, literature, data catalog index, network courses and other forms of resources. According to the expression of information, digital education resources can be divided into digital slide, digital projection, digital audio, digital video, digital online teaching resources, etc. [5]. Through the investigation of the current situation of digital education resource sharing of basic education in Liaoning Province, it is found that there are the following problems: the distribution of digital education resources in urban and rural areas is unbalanced. Due to the unbalanced economic development in urban and rural areas, urban schools are often better than rural schools in the construction of digital education resources. Due to the lack of communication, schools in the province are often prone to repeated construction of resources in the construction of digital education resources. Due to the limited funds of schools, the construction of resources is often limited to the construction of commonly used teaching resources.

Because there is no unified organization, sharing plan and sharing goal, nor unified interface and effective digital education resource sharing platform, it is impossible to realize the efficient and reasonable sharing and use of resources. In order to better realize the sharing of educational resources, it is necessary to establish a sharing platform with stable performance, unified standards and perfect functions, use standard interfaces to unify the resources of schools and departments, and integrate heterogeneous and dynamic resources [6, 7], so as to establish an efficient and high-quality educational resource sharing mechanism. The digital education resource sharing platform based on Hadoop framework has the characteristics of interconnection, collaboration and sharing and simple operation. It has strong advantages in building a digital learning environment, promoting the popularization and sharing of high-quality education resources and promoting the diversified development of learners. The design of Hadoop platform is based on the principles of compatibility and sharing and openness. The main contents of the design include the overall structure design of the system and the structure design based on the system. Through literature research and teacher-student interviews, determine the demand analysis of cloud teaching and autonomous learning platform.

In view of this characteristic of cloud computing, combined with the current situation of educational resource construction in schools in Liaoning Province and the needs of Educational Resource Sharing Construction among schools [8], from the perspective of regional coordinators, a cross language educational resource sharing platform is constructed based on Hadoop framework, and the hardware part is optimized from three aspects: MCU controller, resource reconstruction port and external input port, The software part constructs the resource sharing algorithm based on gae cloud computing, designs the data model, and finally completes the performance analysis of the design platform through the platform test.

2 Hardware Design of Cross Language Education Resource Sharing Platform

The hardware part of educational resource sharing platform is a complex part. Different functions can be realized by using different functional modules, which requires very rich functional modules. At the same time, this also puts forward two requirements for the control platform: first, there are enough ports; Second, it has rich port types. At present, although the embedded processor has a high degree of integration and rich number of pins, the demand for ports on the education platform is changing. The fixed interface function of the hardware system leads to the limited open resources of the system to the outside, and the use method of the port is also single. In view of this problem and combined with the characteristics of the hardware system of the education platform, this paper puts forward the overall functional requirements of the hardware system of the education resource sharing platform of this subject, as follows:

(1) It has good interactive function and is convenient for students to share educational resources.
(2) Support port resource reconfiguration, and the corresponding relationship between the external output port of the controller and the I/O of the core processor can be reconfigured on site [9, 10], so that the same port can be compatible with the bus interface types of multiple modules.
(3) It has a variety of special external port types, such as SPI, IIC, ADC and motor/steering gear port.
(4) It supports the functions of graphical programming, port configuration and online download of upper computer software.

2.1 Design MCU Controller

The hardware control platform is the bottom and foundation of the whole hardware module. As shown in Figure 1, the whole education control platform is designed based on "MCU + FPGA" as the core control system, including MCU controller, FPGA controller, human-computer interaction part, communication interface part and external input and output port. The hardware platform shall meet the requirements of high modularity, strong reconfigurability and open hardware interface.

The core component of hardware control platform is MCU controller. Combined with the characteristics and demand analysis of educational resource sharing platform, the main factors considered in the selection of MCU controller are: processor running speed, integration, hardware resources, cost and power consumption. The running speed of the processor can improve the response of the system, increase the support of external devices, and quickly complete complex instructions. The consideration of low cost can improve the competitiveness of products, and low power consumption can prolong the service time of batteries.

In this paper, "MCU + FPGA" is used as the core control mode. Generally, the communication between MCU and FPGA can interact with instructions according to the predefined communication protocol. For the port resource reconstruction function of the education resource sharing platform, the MCU can send control instructions to

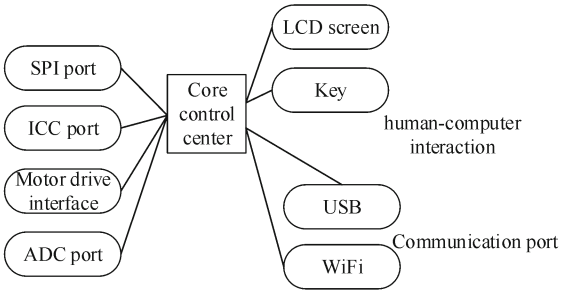

Fig. 1. Bottom layer and foundation of hardware module

the FPGA, and then the FPGA can generate serial port, interrupt, PWM wave and other functions to the external port according to the instructions. However, the implementation of this control method is complex and does not highlight the advantages of "MCU + FPGA" system. MCU itself is embedded with pin resources such as timer, serial port and external interrupt, while FPGA has more abundant wiring resources. The whole chip of FPAG is composed of an array of programmable logic units separated by wiring resources and surrounded by programmable uo units. The logic units arranged in the array are connected through the programmable internal wiring in the wiring channel to realize the logic function, The programmable switch can control the segmented metal wires to connect in any way to form the signal lines required between logic units. In the controller design of this paper, AVR single chip microcomputer ATMega128A is selected as the main control chip of the system. ATMega128A single chip microcomputer is an 8-bit single chip microcomputer with low power consumption and high performance produced by ATMEL company. It is widely used in many fields such as industrial real-time control, communication equipment, instruments and meters. The single cycle instruction execution time and advanced instruction set structure [11, 12] are adopted. Compared with other single chip microcomputer models in this series, it has better performance and higher data transmission rate. It is fully applicable to the design of the hardware control platform of this educational resource sharing platform. Its main characteristics are as follows:

(1) 8-bit microprocessor with high performance and low power consumption. It has a wide working voltage range and strong anti-interference ability of the power supply.
(2) RISC structure design ensures that many instructions are executed in a single clock cycle. The system is under the full static working condition of 16 MHz crystal oscillator, and the processing capacity can reach 16 MIPS.
(3) 8-channel 10 bit successive approximation ADC is integrated internally, and the sampling rate can reach 15 ksps under the highest precision.
(4) Rich IO resources meet system requirements. In addition, the pin resources also include second functions such as timer, counter, serial interface and so on. The I/O interface has a large driving current, and the maximum current can be as high as 40 mA, which can directly drive light-emitting diodes and small relays.
(5) It has 128 K flash storage space and 4 KB ram to meet the basic requirements of the system without additional extended program memory and data storage space.

"MCU + FPGA" is the core control mode. The MCU part was mentioned earlier. Now FPGA and MCU are combined. As a programmable logic device, FPGA provides four kinds of programmable resources: central programmable function unit of the chip, rich programmable IO pin resources, programmable wiring resources and on-chip memory RAM. The rich programmable pin resources and programmable wiring resources meet the functional design requirements of the hardware system of the educational resource sharing platform in this paper. Although CPLD and FPGA have a lot in common, considering the specific application requirements of the system, FPGA has more advantages:

(1) FPGA is more suitable for timing logic and trigger rich structure [13].
(2) FPGA is programmed by changing the wiring of internal wiring. Programming under the logic gate has greater advantages in programming flexibility.
(3) FPGA integration is better and CPLD integration is relatively low.
(4) Generally, the power consumption of FPGA is lower than that of CPLD.

In conclusion, considering that FPGA is used as the controller of resource reconstruction in this part, the chip model is cyclone series ep1c3t100c8. As a medium-sized product of atlera company, this chip is a low-cost FPGA chip, and rich I/O resources fully meet the system requirements. The system circuit mainly includes crystal oscillator clock, serial configurator circuit and download and debugging interface.

2.2 Design Resource-Based Reconfiguration Port

The main idea of port resource reconfiguration is to connect the hardware resource pin of ATMega128A with the external port through internal rewiring of FPGA, so as to realize the conversion of port resources. FPGA has abundant programmable wiring resources and pin resources to meet the system requirements. In terms of hardware design, there are three types of connecting pins with FPGA: connecting pins between ATMega128A and FPGA, connecting pins between internal modules of the system and FPGA, and connecting pins between reconfigurable ports and FPGA. The pin resources connected between FPGA and ATMega128A include 8 ordinary pins (PA2-PA3, PA6-PA7, PC2-PC3, PC6-PC7), two serial ports (RXDO, TXDO, RXD1, TXD1) and four PWM (OC3A, OC3B, OC1A, OC1B), one external interrupt (PDO (SCL)) The design is divided into default mode and reconfiguration mode according to the use mode of system resources. In the default mode, common pin resources are allocated to the reconfigurable port, and other resources are used by the default internal module; in the reconfiguration mode, serial port, interrupt, PWM and other resources are allocated to the reconfigurable port, and the corresponding internal module using the resource will stop working temporarily. According to this principle For the convenience of users, the system defines the port reconfiguration specification to indicate the resource allocation under different modes, as shown in Table 1:

It is pointed out here that the serial port resources connected to FPGA are ATMega128A, which is connected to FPGA after multiple selection switches. The specific details will be explained in the next section. The INH input pin of CD4052 chip is set low to enable multiple chip selection. The two input control pins a and B are

Table 1. Resource allocation of FPGA in each mode

Serial number	Hardware resource	Default mode		Reconstruction mode
1	common pin	Reconfigurable	Interface	–
2	Uarso serial interface	COM1/COM2/COM3/COM4		Reconfigurable ports COM1/com2
3	Uarts1 serial interface	Wifi module		Reconfigurable port COM31/COM4
4	Pwm0 timer output	–		Reconfigurable port COM1
5	Pwm1 timer output	Motor 1 channel a	Control input	Reconfigurable ports com2
6	Pwm2 timer output	Motor 1 channel Ba	Control input	Reconfigurable ports COM3
7	Pwm3 timer output	Motor 2 channel a	Control input	Reconfigurable ports COM4
8	Intro external interrupt/SCL	Motor 2 channel Ba	Control input	Reconfigurable ports COM1/COM3

controlled by one control signal line. Where P_ CTRL1, P_ CTRL2, P_ CTRL3 is connected and controlled by PE2, PE6 and PE7 pins of ATMega128A respectively. The A and B pins are set high through the pull-up resistance. Y3 channel is gated by default when the system is powered on to ensure the use of the basic functions of the system. Students can change the gating of different paths through programming, so as to realize different functions. As shown in Table 2, the application of each resource in different path selection.

Table 2. Resource allocation of multi-channel selector switch

Serial number	Hardware resource	First path	Second path
1	Uars0 Serial I/O interface	USB module	FPGA resource reconfiguration
2	Uars1 Serial I/O interface	LCD display module	FPGA resource reconfiguration
3	SPI serial I/O interface	Epcs 16 Serial Configurator	SPI dedicated port

In order to realize fast and simple assembly and flexible combination of various modules, the external ports must be standardized and diversified. According to this requirement, the external input and output ports of the system hardware design uniformly use the six wire universal interface of RJ11. The system has a total of 10 external ports. According to the type of ports, they are divided into two categories: dedicated ports and reconfigurable ports.

2.3 Design of External Input Port

The specific connection of each external port is as follows:

(1) SPI port: this port is connected to the multiplexer selection chip. When programming, ATMega128A controls the path selection and connects the port to the SPI function pin of PBO-PB3.
(2) IIC port: pin 5 of the port is connected with FPGA, and the other pins are connected with PD4, PD5 and PD1 (SDA) of ATMega128A respectively. In default mode, pin 5 corresponds to PDO (SCL) pin, which is used as IIC port.
(3) Motor/steering gear ports M1 and M2: two motor drive signals in each port are connected with the output pin of the motor drive chip to control the speed and forward and reverse rotation of the DC motor. PWM2_ 5 , PWM5_ S is directly connected to the timer output pins of pe5 and pb7 of ATMega128A to control the angle of the steering gear.
(4) AD acquisition ports ADC1 and ADC2: connected to pfo-pf7 pin of ATMega128A, providing 8 ad signal acquisition channels for sensor analog signal acquisition. USB is used to standardize the connection and communication between external devices and computers. As a standard external high-speed bus interface, USB is suitable for a variety of devices, such as MP3 players, cameras, high-speed data acquisition devices, etc. Compared with other communication interfaces, the biggest feature of USB interface is easy to use. The system can automatically configure all functions without user participation, and supports hot plug. However, ATMega128A hardware itself does not support USB communication function and requires peripheral circuit conversion. The circuit connection is shown in Fig. 3–17, where a_ Txdo and a_ RXD0 is the Y3 channel pin of the multi-channel selector switch. After path selection, it corresponds to the serial port pins PE3 (TXD0) and PE2 (RXDO).

This platform uses FT232RL as the USB interface conversion chip, which can realize the conversion between Serial uart interface and USB without specific USB firmware programming, and supports the data transmission format of serial interface 7 or 8-bit data and 1 or 2-bit stop bit. FT232RL chip integrates clock circuit, EEPROM, resistance and avcc filtering, which reduces the number of external components, 256 byte receiving buffer and 128 bytes Byte sending buffer can achieve high data throughput, which is very important in daily system data exchange or program download. Considering the power consumption and size of the control system, esp8266 WiFi module designed by Shenzhen Anxin Co., Ltd. is selected as the wireless communication module in the system. The control mode of serial communication reduces the occupation of pin resources, It

supports at instruction set and has strong advantages for subsequent secondary development. Esp8266 is characterized by high on-chip integration, so it can be used with only a few external circuits. As shown in Figure 2, the module utxd and urxd are connected with FPGA controller. In the default mode, FPGA connects the serial port of ATMega128A O The pins are assigned to the module. Esp8266 supports three working modes: AP, station and AP + station. The internal firmware integrates at instruction set and has many rich instructions, which is convenient for the secondary development of functions in the later module function design, so as to realize the wireless communication function between the controller and the computer or mobile device.

3 Software Design of Cross Language Education Resource Sharing Platform

Based on the hardware design, in order to further optimize the performance of the cross language education resource sharing platform in the process of resource sharing, optimize the Hadoop framework resource sharing algorithm, and build a data model to improve the efficiency of cross language education resource sharing.

3.1 Optimize Resource Sharing Algorithm Based on Hadoop Framework

Hadoop is an open source, distributed system infrastructure platform. It is an open source distributed computing and storage project implemented in Java. Hadoop is actually composed of multiple parts. Hadoop MapReduce is the core part, as shown in Figure 2:

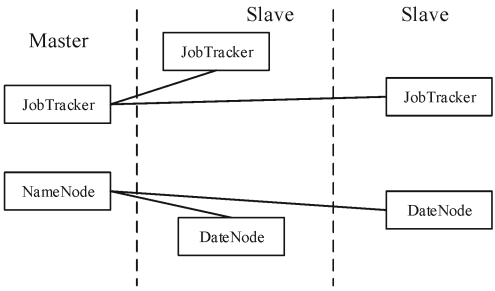

Fig. 2. Basic structure of Hadoop framework

Compared with traditional distributed systems, Hadoop system has the following advantages: Hadoop can run on large-scale clusters composed of Job Tracker and commercial computers, or on cloud computing servers such as Amazon's elastic computing cloud (EC2); Hadoop enables users to write parallel code quickly and efficiently through the subordinate structure(Slave); The data and backup mechanism in HDFS distributed file system and the task monitoring mechanism in MapReduce ensure the reliability of distributed processing; The scale of Hadoop can be linearly expanded by increasing the number of nodes in the cluster to solve the problem of big data processing [14].

Symbols $P(n), H_{k,n}^2$ *and* $f(C_n)$ represent the transmission power, channel gain and power required to receive data when transmitting data to user k on subcarrier n, respectively. And the mathematical relationship between them can be expressed as:

$$P_k(n)\frac{f(C_n)}{H_{k,n}^2} \tag{1}$$

It shows the relationship between transmission power and reception power required to share educational resource data with users on a subcarrier. Each subcarrier simultaneously transmits the same data for multiple users in the multicast group, so the transmission power $P(n)$ required on a subcarrier during multicast is related to the channel gain of all users served by the subcarrier. The exact mathematical relationship is as follows:

$$P(n)\frac{f(C_n)}{H_n^2} \tag{2}$$

In formula (2):

$$H_n = \min\left\{H_{k,n}|pk(n) = 1\right\} \tag{3}$$

In formula (3), xx is an indicator, which indicates whether subcarrier n is allocated to user k. It reveals that the transmission power required on the subcarrier during multicast depends on the worst channel gain of the users served by the subcarrier. And the detailed definition of indicator $pk(n)$ is as follows:

$$pk(n) = \begin{cases} 1, n \to k \\ 0 \end{cases} \tag{4}$$

The optimization objective of the model in this chapter is to minimize the total transmission power required by the system through reasonable and effective bit allocation and subcarrier allocation under the condition of limiting the total rate of the system, and mark the minimum transmission power required by the system as Pmin. Then the optimization model can be mathematically expressed as follows:

$$P_{\min} = \min\sum_{n=1}^{N} P(n) = \min\sum_{n=1}^{N}\frac{f(C_n)}{H_n^2} \tag{5}$$

$$P(n) \geq \frac{f(C_n)pk(n)}{H_{k,n}^2} \tag{6}$$

$$\sum_{k=1}^{k}\sum_{n=1}^{N} C_n pk(n) \geq 0 \tag{7}$$

$$pk(n) \geq 0 \tag{8}$$

$$P(n) \in \{0, 1\}, C_n \in B \tag{9}$$

The above formula (5) is the optimization goal of the algorithm to minimize the total transmission power required by the system. The transmission power on the subcarrier must meet the channel gain requirements of all served users; The total rate available to all users of the platform must be greater than the minimum rate requirement of the system; The transmission power on the subcarrier must be non negative: constraint 3 symbol 1 must be taken from positive integers 0 and $pk(n)$, and the number of bits allocated on the subcarrier must be taken from the number of bits set B that the system can provide.

3.2 Design Data Model

Relational database is the main tool in the design and implementation of application system. In the process of traditional database design, the author usually establishes the data model with data table structure. The relational database realized in the design process is the main goal and task of the system.

This paper is an application developed based on Google App Engine development environment. Gae does not support traditional data storage, that is, relational database storage. However, due to habitual considerations, we still use data tables to describe the data model information, and then transplant them into the data storage model recognized by gae through the data storage methods mentioned later. The main data tables involved in the system are shown in Table 3−Table 5.

Table 3. User basic information user data table

Field name	Data type	Remarks
userID	Long	Tag user ID
UserName	String	User name
Password	String	User password
Email	String	Email (Google account)
roleID	Int	User role

Table 4. Role data table

Field name	Data type	Remarks
roleID	Long	ID of the tag role entity
rolename	String	Including students, teachers and adminstrators
roleType	Int	1 (student), 2(teacher), 3(administrator)

After logging in, students can browse all groups under interest groups. On the interest group list page, students can view the name, founder account, founder name, creation time, topic, access times and other information of all interest groups. At the same time, they can filter and query the interest group list by conditions, and the filtering results

Table 5. Data sheet of education resource information

Field name	Data type	Remarks
fileID	Long	ID that marks the uniqueness of the resource
filename	String	Source title
filecontent	Long	Source content
Username	String	Asset publisher user name
useremail	Email	Resource publisher mailbox
upldadDte	Date	Resource upload time
description	String	Resource description
courseID	Long	Course to which the resource belongs
courseID	String	ID marking course uniqueness
courseInfo	String	Course introduction information
postID	String	ID that marks the uniqueness of the post
posttitle	String	Post on title
postcontent	String	Post content

Table 6. Platform operation hardware environment

Equipment	Model	CPU	Memory	Network bndwidth
Controller	HP	Intel(R)Core™i7-4790CPU@3.60GHz	64 GB	100Mbps
	ProDesk			
	498G2			
	MT			
Calculation node	HP	Intel(R)Core™i7-4790CPU@3.60GHz	64 GB	100Mbps
	ProDesk			
	498G2			
	MT			
Client	MT	HP ProDesk 498G2 MT	64 GB	100Mbps
	HP			
	ProDesk			
	498 G2			
	MT			

are still returned in the same form. Students can browse the group or apply to join the group according to their personal interests. They can become members of the group

only after being approved by the group leader. Students can create their own groups, view my group and group information related to me, and delete the groups they create. Share resources in the same group. Group members can upload resources for use by group members and leave messages in the group to communicate with others. Everyone can also delete their own uploaded files, and the team leader can delete all files in the group. Students can invite others to join or leave the group. The teacher's operation of the interest group is consistent with that of the students. The administrator has the function of managing the group, mainly including the addition, deletion, modification and query of group resources and messages, and the deletion of the group.

4 Platform Test

The design of cross language education resource sharing platform based on Hadoop framework studied in this paper integrates and virtualizes the existing hardware infrastructure and constructs a unified resource pool with the help of cloud computing technology. In order to test the practicability of the cross language education resource sharing platform, the public library resource integration and sharing methods pointed out in reference [14] are compared as the original platform, and a comparative test experiment is designed.

4.1 Test Software and Hardware Environment

The educational resource sharing platform built in this paper is based on the cloud platform built by openstack. Due to the limitations of the laboratory environment, the cloud platform in this paper is composed of a control node, a computing node and a client. One PC is used as the openstack control node, one PC is used as the control node, and the other computer is provided as the client. The control node is deployed on a PC. The hardware environment configuration list of this platform is shown in Figure 6:

The software environment for system development and operation in this paper is as follows: (1) The control node takes Ubuntu 14.04.3 server as the underlying operating system, the system version running on the client is windows 10 Ultimate, and the openstack project version is kilo. (2) The running environment of distance education platform, the application layer of this paper, is apache-tomcat-7.0.57 for the server, Oracle11g for the database, and JDK version 1.7.

4.2 Test Results

The testing tool used in this paper is Apache jmeterl42, which is a Java based tool designed and developed by Apache for stress testing. It can simulate the concurrent access of multiple users to the system and record the response time. Although the software can not simulate the real user access, it can control the user request to be sent evenly within a certain time. This chapter tests the response of users accessing the system, sets all requests to be sent within 1 second, sets the number of threads (i.e. the number of simulated users) to 50 to 500, increases 50 each time, and simulates 10 times at the most

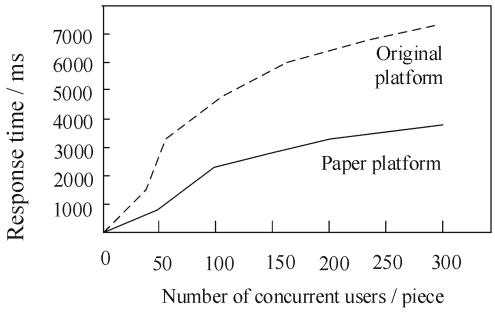

Fig. 3. Comparison of response time

ten sampling points, records the response time comparison each time, and draws the comparison diagram according to the test results, as shown in Fig. 3:

As can be seen from Fig. 3, cloud computing technology adopts virtualization, its own scheduling strategy and load balancing method. Compared with traditional methods, the response time is significantly reduced when the number of concurrent users is large, and has high response speed and service quality.

Use this platform and the original platform for standard resource sharing, then count the completion time of resource sharing, average waiting delay and resource download time, and finally make a comparative analysis. The statistical results are shown in Table 7.

Table 7. Evaluation results of sharing ability

Method	Resourec sharing	Average waiting delay	Resourec download time
	Completion time/s	/s	/s
Paper platform	5.62	1.36	3.66
Original platform	7.23	2.42	5.63

As can be seen from Table 7, when using the cross language education resource sharing platform based on Hadoop framework to share standard resources, the sharing completion time, average waiting delay and resource download time are shorter than those of the original platform, indicating that the sharing ability of the constructed platform is stronger.

5 Conclusion

Based on the research and summary of educational resource sharing platforms at home and abroad and the combined application of cloud computing and distance education, this paper constructs the cloud platform with the help of openstack open source project, and designs and implements each module in the platform. The main work of this paper is as follows:

(1) This paper analyzes the current situation of the existing platform, summarizes the problems of slow response time and long waiting delay of the platform, and designs a cross lingual education resource sharing platform based on cloud computing and Hadoop framework, combined with the advantages of cloud computing technology that can quickly integrate, share and transmit massive multi-source data.
(2) Study the relevant technologies needed to build a platform based on Hadoop framework.
(3) Conduct a detailed demand analysis of the platform and determine the design objectives. Combined with the existing application cases of cloud computing in distance education, this paper designs an implementation scheme of distance education platform based on cloud computing, and analyzes and designs the overall model, hierarchy and components of the platform.

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