Dynamic Performance Evaluation of Type-3 Compensator for Switch-Mode Dc-Dc Converter

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Abstract. This paper describes application of type-3 compensated error amplifier for switch-mode dc-dc converter using OrCad/Pspice simulation tool. For several decades power supply design has been showing a gradual movement away from the use of linear power supplies to the more practical switched mode power supply. The linear power supply contains a mains transformer and a dissipative series regulator that increase the size extremely and heavy 50/60 Hz transformers, and also very poor power conversion efficiencies approximated below 50%. These drawbacks are improved using switch mode power supplies that incorporates fast switching devices having estimated efficiency of above 80%, compact size and light in weight. These features are mainly due to the controller as a basic building block apart from the Dc-Dc converter, which is the heart of switch mode Dc power supply. Thus, in this paper application of type-3 compensated error amplifier for switch-mode dc-dc converter has been proposed and implemented using OrCAD/Pspice tool. Accordingly, dynamic and steady-state performance/evaluations have been performed for step changes input/output (load) side. The results revealed that the system has fast dynamic response and reduced steady-state error for input and output side disturbances.

Keywords: Switch mode dc-dc converter · Type-3 compensator · Dynamic response

1 Introduction

The ever increasing advancement in modern electronic systems needs high quality, efficient, portable size, light weight and reliable power supplies. Linear regulated power supplies are operating at low frequency, need large size transformer, large size inductors and have low efficiency. Thus, utilization of switch mode power supplies of ac or dc types are also growing at a faster rate to satisfy the need of modern electronic system [1–6]. Switch mode Dc power supplies comprises of basic blocks of the feedback controller and Dc-Dc converter along with PWM generation and gate driver circuit. The feedback control action also controls the Dc-Dc converter. The converters can be of isolated or non-isolated. The non-isolated converters include buck, boost and buck-boost converters [1, 7–9]. This papered focused on modeling and simulation of switch mode Dc-Dc buck converter suing OrCad/Pspice software tool. The tasks involved include

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design of Dc-Dc buck converter for a preset specification, design of the feedback loop controller/compensator, developing Pspice model of the whole system and perform simulations to see the steady state and dynamic performance of the system for disturbance of input and output side.

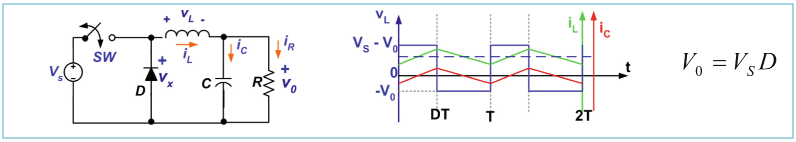
The contents of this paper are organized into six sections. Section 2 presented concise description of switch mode Dc-Dc converters, schematic representations and relations non-isolated switch-mode Dc-Dc converters. The third section presented specifications, design of the power converter and the feedback controller. The forth section presented OrCad/Pspice circuit model of the feedback loop Dc-Dc buck converter considered in this paper. Simulation results and discussions of dynamic and steady-state responses when the system is subjected to step changes in reference input voltage and step changes in external load are presented in Sect. 5 of the paper. Finally, summary of findings are presented in Sect. 6 of the paper.

2 Switch Mode Dc-Dc Converters

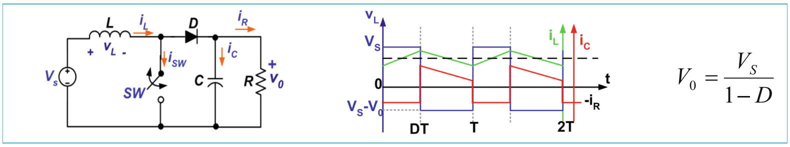
Switch mode converters use fast switching power electronic devices of the on and off states of the switches (the feature that makes switch mode converters achieve high efficiency). The high frequency operation of power electronic switches use high frequency and lighter weight transformers, filter capacitors and inductors. And operating at high frequency can achieve fast dynamic response to changes in load and reference voltage. The heart of switch mode Dc power supply is Dc-Dc converter circuit. The basic functions of dc–dc converters may be convert a dc input voltage to a dc output voltage, regulate the dc output voltage against load and line voltage changes, reduce the ac voltage ripple on the dc output voltage, provide isolation between the input and the load and protect the supplied system and the input source from electromagnetic interference [1, 9].

Availability of a large variety of Dc-Dc converters is presented in literatures. Among them, converters with isolation and without are some of them [1, 6–9]. Dc-Dc converters with no transformer coupling/isolation can be classified as step-down (buck) converter, step-up (boost) converter and step-down/step-up (buck-boost) converter. Analysis of the these converters for continuous conduction conditions is based on the assumptions that the circuit is operating in the steady state, the inductor current is continuous (always positive), the capacitor is very large, and the output voltage is held constant at voltage Vo, the switching period is T; the switch is closed for time DT and open for time $(1 - D)$ T and ideal components [6, 10]. The schematic diagrams, input/output characteristic and relations of Dc-Dc converters with not transformer coupling for continuous conduction mode are given in Fig. 1.

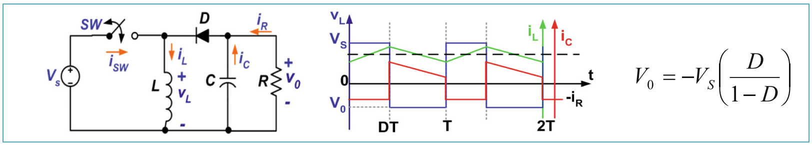
To achieve stable performance of the switch mode Dc-Dc converters, feedback loop controller to adjust the duty ratio of switches is usually applied. The variation in the duty ratio is in response to disturbances from input/output side to keep the output parameter same as the reference value. Usually, voltage and current mode feedback loop controls are used. In voltage mode control, the output voltage is sensed and input to the error amplifier. The difference between the output and reference voltage is feed to the voltage controller. The voltage controller comprises of the controller, comparator having inputs



(a) Buck-converter



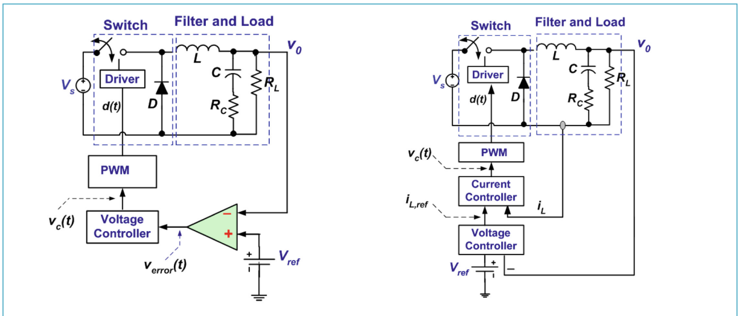
(b) Boost-converter



(c) Buck-Boost-converter

Fig. 1. Switch-mode non-isolated Dc-Dc Converters, characteristics and relations

of control signal and saw tooth waveform generator to produce PWM signal which is fed to drivers of controllable switches in the dc-dc converter. This mode of control has an advantage of simple and flexible in implementation, however, this mode has delayed line voltage regulation. The schematic diagram in Fig. 2(a) shows basic components of voltage mode control [6, 11, 12]. In current mode control, an additional inner current loop to feedback the inductor current is used. This signal is converted to voltage and replaces the saw tooth waveform. This mode of control has better dynamic performance relative to voltage mode control. However, large number of components and implementation complexity are major disadvantages of this mode of control. Figure 2(b) shows schematic representation of current mode of control [1, 6].



(a) voltage mode control (b) current mode control

Fig. 2. Schematic diagrams of common control modes for a buck converter

3 Designing Switch-Mode Dc-Dc Converter

The Dc-Dc converter circuit is the heart of a Dc switch mode power supply. In this paper, buck converter operating in continuous-current conduction mode is considered as main part of the switch mode supply. The basic building blocks of the regulated buck converter includes the switch, drive circuit, output filter, compensator (error amplifier), and a pulse-width modulating circuit. Voltage mode control is designed and implemented. The output voltages of dc power supplies are regulated to be within a specified tolerance band in response to changes in the output load and the input line voltages by modulating the duty ratio to compensate for variations in the input or load. A feedback control system for power supply control compares output voltage to a reference and converts the error to a duty ratio. The design specifications, parameters, and control requirements are given in Table 1. Selection of converter specifications is based on the assumptions that for electronics laboratory purpose, the DC voltage is usually ±5 V or ±12 V or ±15 V. Thus, assuming tolerance of 5 V, output voltage may vary up to 20 V. Switching frequency is selected above 20 kHz which is the human hearing threshold.

Table 1. Design specifications

Input voltage	50 [V] to 200 [V] dc
Output voltage	Maximum 20 [V] dc
Load current	5 [A]
Switching frequency	200 [kHz]
Ripple voltage	<0.5
Change inductor current (Δi_L)	<0.8 [A]

3.1 Converter Design

The design of buck converter considers only selecting component values according to the design specifications. Switch selection and thermal (heat sink) design is not considered because the scope of paper is modeling and simulation regulated switch mode buck converter. The values for inductance for a specified peak-to-peak inductor current and capacitance can be determined using expressions in Eq. (1).

$$\begin{cases} L = \left(\dfrac{V_S - V_0}{\Delta i_L f}\right) D = \dfrac{V_0(1-D)}{\Delta i_L f} \\ C = \dfrac{1-D}{8L(\Delta V_0/V_0) f^2} \end{cases} \tag{1}$$

Substituting the given values, L = 75 uH. For continuous conduction add 25% of L and then L = 93.75 uH and the capacitance, C = 46.66 uF. The value of internal resistance of capacitor, RESR = 0.3 and for the inductor, very small value is considered.

The feedback controller to regulate the output voltage must be designed to meet the objectives of zero steady state error, good dynamic response and low noise susceptibility [13, 14].

3.2 Compensator Design

The controller/compensator can be realized using PID controller, lead-lag compensators or using compensated error amplifiers of different types, sliding mode control, etc. [15–17]. In this paper, compensated error amplifier of type-3 is considered because the frequency response can provide sufficient phase angle difference to meet the stability criterion of a minimum phase margin of 45° [6]. The schematic diagram of type-3 compensated error amplifier is given in Fig. 3.

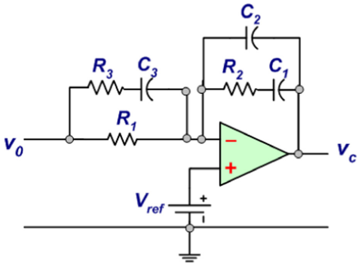


Fig. 3. Compensated error amplifier.

The small-signal transfer function given in Eq. (2) is expressed in terms of input and feedback impedances Zi and Zf.

$$G(s) = \frac{\tilde{v}c(s)}{\tilde{v}o(s)} = -\frac{Zf}{Zi} = -\frac{\left(R_2 + \frac{1}{sC_1}\right)||\frac{1}{sC_2}}{R_1||\left(R_3 + \frac{1}{sC_3}\right)} \tag{2}$$

Rearranging the expression in Eq. (2) can be expressed as Eq. (3).

$$G(s) = -\frac{R_1 + R_3}{R_1 R_3 C_3} \frac{\left(s + \frac{1}{R_2 C_1}\right)\left(s + \frac{1}{(R_1+R_3)C_3}\right)}{s\left(s + \frac{C_1+C_2}{R_2 C_1 C_2}\right)\left(s + \frac{1}{R_3 C_3}\right)} \tag{3}$$

Assuming C2 << C1 and R3 << R1, expression in Eq. (3) can be simplified to Eq. (4)

$$G(s) \approx -\frac{1}{R_3 C_2} \frac{\left(s + \frac{1}{R_2 C_1}\right)\left(s + \frac{1}{R_1 C_3}\right)}{s\left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{1}{R_3 C_3}\right)} \tag{4}$$

In the design of the compensated error amplifier, first choose R1 and Table 2 gives expressions to compute other component values [6].

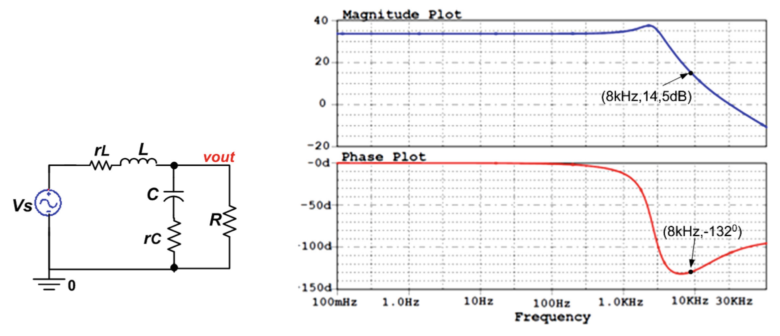
Table 2. Expressions to determine component values

R$_1$ choose first	$C_1 = \frac{\sqrt{K}}{\omega_{co} R_2}$
$R_2 = \frac{\lvert G(j\omega_{co}\rvert R_1}{\sqrt{k}}$	$C_2 = \frac{1}{\omega_{co} R_2 \sqrt{K}}$
$R_3 = \frac{1}{\omega_{co} \sqrt{K} C_3}$	$C_3 = \frac{\sqrt{K}}{\omega_{co} R_1}$

Controller is designed in frequency domain using OrCAD Pspice tool. For the controller to have stable response a phase margin of at least 45° is a commonly used criterion for stability [6, 18]. The crossover frequency of 8 kHz and a phase margin of 60° is considered. Accordingly, the frequency response of the buck converter to see the phase and gain margins is given in Fig. 4. Figure 4(b) shows the frequency response of the buck converter ac equivalent circuit model given Fig. 4(a). From the frequency response plot, at the crossover frequency of 8.0 kHz and a phase margin of approximately 65°, the Pspice ac frequency sweep shows that the output voltage is 14.5 dB and the phase angle is −131.98°. Thus, the required phase angle of the amplifier will be 191.980. Accordingly, the corresponding values of K and other component values are computed.

4 Pspice Model of Regulated Buck Converter

Pspice circuit models used for simulation purpose may vary according to the goal of simulation. To evaluate the current and voltage waveforms with detail variations such as peak-to-peak values needs a circuit model with a switching device or model of the switch with basic characteristic of actual switching device.



(a) buck-converter ac equ. ckt

(b) frequency response

Fig. 4. Ac equivalent circuit and frequency response plots of the buck converter

The simulation model that considers switches has the transient time for the overall system large than switching period that increase execution time of the program. The most widely used simulation goals to predict the dynamic behavior of converters consider average values of switching waveforms. The transient behaviors of the system can analyzed by considering linear circuit that the responses will be averaged values of switching waveforms [19, 20]. Figure 5 shows averaged Pspice models of closed loop dc-dc buck converter considered in this paper. RL1+ and RL2+ are external loads added to see step responses when the regulated converter is subjected to step changes in load.

5 Results and Discussions

To evaluate the dynamic and steady-state performances of the system a number of simulation tasks have been performed. The simulation tasks and different cases considered include (i) step-response of averaged and switched models, (ii) response of step change in input reference and (iii) response to step change in external loads.

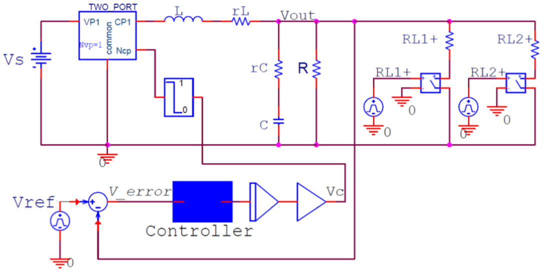


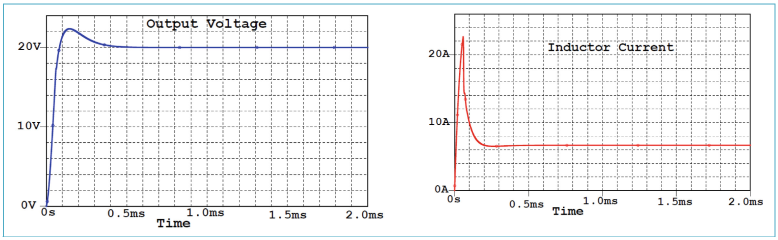
Fig. 5. Averaged Pspice models of regulated buck converter

5.1 Step-Responses of Averaged and Switched Models

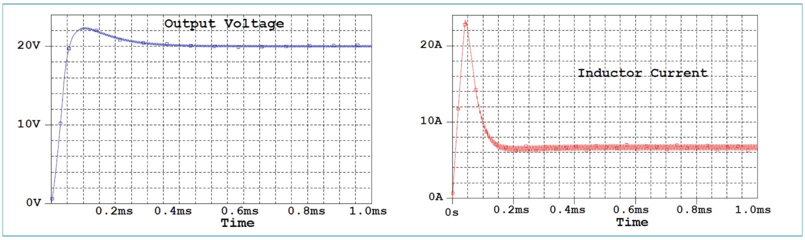
Step response of both switched and averaged models for step input reference voltage of 20 V is recorded in Fig. 6. Switched model response is considered to see the detail transient responses of peak-to-peak change in inductor current ac ripple voltage of capacitor. The switched averaged model has output voltage ripple and inductor current changes from average value. The simulation result of steady-state response in Fig. 6(c) show that the peak to peak ripple voltage (output voltage) is ($20.161 - 19.872 = 0.289$ V). This magnitude is very much less than peak-to-peak voltage value (<5 V) set at the specifications table during design stage. And for the inductor current, peak-to-peak inductor current is, $7.0757 - 6.2541 = 0.8216$ A which within the specification given at designed stage (<0.8 A). The simulation results in sections below consider only.

5.2 Responses for Step-Change in Reference Input

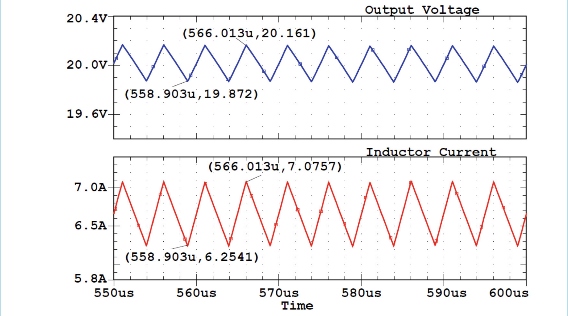
Step change in reference input voltage at time $t = 1$ ms (from 10 V to 20 V) is applied. The responses in Fig. 7 show very small overshoot and short settling to the reference input for the averaged Pspice model in Fig. 5. The result shows that whenever there is change in reference input voltage, the controller tries to keep the output voltage the same as the reference input with fast dynamic response.



(a) step response for average model

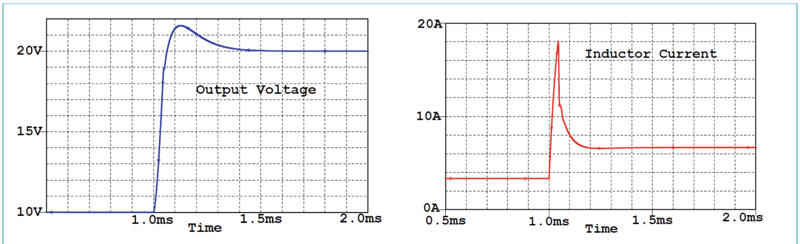


(b) step response for switched model



(c) switched model steady-state response

Fig. 6. Pspice Probe outputs of averaged and switched models of the system

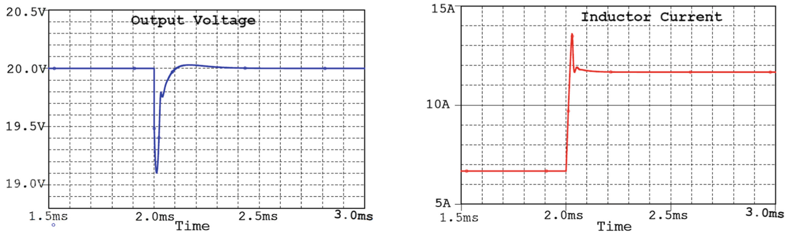


(a) Output voltage (b) Inductor current

Fig. 7. Transient responses

5.3 Responses for Step Change in External Loads

Case-1: A step change in external load of RL+ = 3 Ω is connected in parallel with the existing 3 Ω at time t = 2 ms during the simulation period of 3 ms for the averaged Pspice model in Fig. 5. The transient responses given in Fig. 8 shows responses for output voltage and inductor current for step-change in external load. The results show fast dynamic responses to achieve the specified output for the reference input of 20 V. The inductor current shows an increase from 6.66 A to ≈11.7 A in response to added external load.



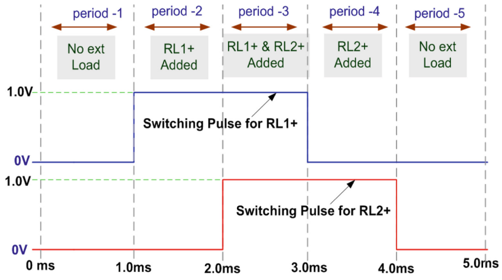
(a) Output voltage (b) Inductor current

Fig. 8. Pspice model Probe outputs for a step change in load

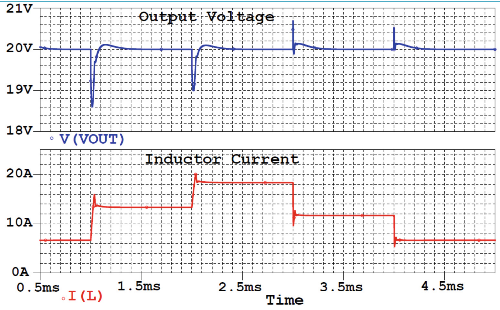
The output is to be regulated at 20 V for the reference input voltage of 20 V. The phase margin of this circuit is 60° when the load is 3 Ω and slightly greater than 60° when the load changes to 3||3 Ω. A step change in load occurs at t = 2 ms. If the circuit were unregulated, the output voltage would change as the load current changed because of the inductor resistance. The control circuit adjusts the duty ratio to compensate for changes in operating conditions. The simulation results show that the system considered kept stable for step changes in external loads.

Case-2: The second case considered step-change in external loads to be connected in parallel to the 3 Ω load at different time instances of the simulation period. Accordingly, RL1+ = 2 Ω and RL2+ = 3 Ω are connected at time instances of 1ms and 2 ms respectively. The switching periods and pulses of external loads is given in Fig. 9(a). For the indicated four periods, the output voltage shows fast move to achieve the reference input voltage, 20 V. The inductor current shows step increase from 6.66 A to ≈12.7 A again to ≈18 A for the simulation period up to 3 ms in response to addition of external loads and again back to ≈11.8 A and again reduced to 6.66 A for simulation periods of 2 ms in response to step removal of external loads.

For all input reference input voltage values, the output voltage is nearly the same as input. In this paper, since the voltage levels considered is small level and averaged model is considered, the output and input reference are approximately equal. Actually, if switched model is considered, switching and conduction losses may contribute losses even though not as such significant. This shows, the conversion efficiency of switch mode power electronic converters is above 95%.



(a) switching pulses for added external loads



(b) responses for added external loads

Fig. 9. Pspice Probe outputs for a step change in external loads

6 Conclusions

The major tasks completed this paper include design, modeling, simulation and performance evaluation of type-3 error amplifier compensated switch mode dc-dc buck converter. The system considered is tested for input reference and external load step changes at various times of the simulation period. The dynamic and steady state responses revealed that performances of switch mode dc power supply has efficiency of greater than 95%, fast dynamic response, reduced overshoot and very small steady-state error using type-3 compensator proposed.

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