Non-inverting Buck-Boost DC-DC Converter with Three-Mode Selection Circuit

Van Tuan Nguyen, Quoc Bao Bo, and Xuan Thanh Pham(✉)

Hanoi University of Industry, Hanoi, Vietnam
thanhpx@haui.edu.vn

Abstract. For battery-powered applications where high current conversion efficiency and long battery life are required, non-inverting Buck-Boost converters are considered the best option. However, during mode switching, ripples in the output current and voltage can significantly affect the efficiency of the chip. The novel Non-inverting Buck-Boost DC-DC converter proposed in this study with a three-mode selection circuit selects the different operating modes (three modes) by comparing V_{IN} and V_{OUT}. By this way, the DC-DC converter can reduce the output ripple and instability during operation. The proposed chip was developed and implemented on the CMOS 0.18 μm process. In addition, a high peak efficiency of 97% can be achieved under the conditions of a wide input range of 2.5 V - 5 V.

Keywords: Three-Mode Selection Circuit · DC-DC Converter · Integrated Power Management

1 Introduction

With the rapid proliferation of battery-powered devices, effective power management solutions have become an important part of the design to ensure long battery life [1, 2]. Since they offer a wide operating range of input and output voltages, non-inverting Buck-Boost converters are a good choice to better utilise battery capacity [2–8]. There are three options: Boost, Buck and Buck-Boost. The level of the input and output voltages determines these modes. If V_{IN} is lower than V_{OUT}, the converter operates in Boost mode. The converter switches to Buck mode when the V_{IN} exceeds V_{OUT}. The converter enters Buck-Boost mode when V_{IN} approaches or equals V_{OUT}. On the other hand, these converters need to sustain a consistently high-power conversion efficiency across all three modes. However, certain converter architectures, such as those explained in [9–11], as a result of the integration of several converter pairs, phase difference management, and many internal oscillators, the demand on the controller grows. As a result, these complexities lead to inconsistent operation and interruptions in the operation of the converter. Alternative techniques, such as the reverse Buck-Boost approach presented in [12, 13], have already been presented. However, the high switching current resulting from continuous operation in Buck-Boost mode puts significant stress on the device. In

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contrast, the Buck-Boost converter in [14] does not employ the Buck-Boost mode. However, switching between Buck and Boost modes causes substantial ripple in the output voltage and hence reduced efficiency. Another method detailed in [15] employs digital control of the converter. This converter switches between Boost and Buck modes. The proposed solution to duty cycle over-lap control decreases voltage ripple and unstable output voltage behavior. However, improving the efficiency of this architecture remains an important goal. This paper presents a DC-DC Buck-Boost converter that achieves good efficiency in all three modes with varying input voltage levels. The proposed converter aims to improve conversion efficiency by switching quickly and with minimal delay between Buck, Buck-Boost and Boost modes with minimal delay to keep the circuit operating continuously [16]. This allows smooth transitions between the three modes and minimizes switching and conduction losses. Therefore, the proposed circuit for selecting the three modes helps to quickly detect changes in input voltage and output voltage with low latency and determine the appropriate mode.

2 Circuit Design

2.1 Proposed System

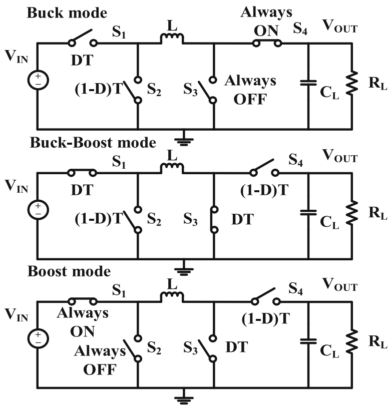

Fig. 1. The Buck-Boost converter's operational principles.

A non-inverting Buck-Boost converter is a switching power supply that can raise (Boost) or decrease (Buck) an input voltage to produce a regulated output voltage, even if the input voltage fluctuates drastically. Figure 1 shows the structure of a non-inverting Buck-Boost converter. The converter runs in Boost mode when the input voltage V_{IN} is lower than the output voltage V_{OUT}. Switch S_1 is always on, while switch S_2 is always off. The control of the power switches S_3 and S_4 leads to this operating mode. On the other hand, the converter operates in Buck mode. When V_{IN} is greater than V_{OUT}, switch S_4 is always ON and switch S_3 is always OFF. The output voltage is kept stable by switching switches S_1 and S_2. The last mode is when V_{IN} is equal or close to V_{OUT} and the converter is set to Buck-Boost mode. In this mode, all switches (S_1-S_3) and (S_2-S_4) are controlled in two groups to regulate the induction cycle (charging and discharging). According to the previous description, the switching behaviour of the power switches and the control circuit allows the converter to adapt to changing input conditions and provide a regulated output.

Figure 2 depicts a visual depiction of the proposed system's block diagram. A power stage and a control circuit are the main components of the converter. The power stage is comprised of four on-chip power switches ($S_{1,2,3,4}$); the transistors used for the switches are larger in size compared to the control circuit. This deliberate choice results in a reduction of the detector current and resistance (R_{ON}) of the transistors to improve efficiency. The control circuit includes a ramp generator, a pulse generator, a soft-start circuit, and a three-mode selection circuit. The operating modes are automatically and quickly determined by using the proposed three-mode selection circuit, which relies on comparing V_{IN} to V_{OUT} and simultaneously outputs the control signals HS_I, LS_I, HS_O, and LS_O, depending on the operating mode. This allows smooth transitions between the three modes and reduces switching and conduction losses. In cases where V_{OUT} is lower than V_{IN}, the converter is set to Boost mode. On the contrary, when V_{OUT} exceeds V_{IN}, the converter is set to Buck mode. When V_{IN} is equal to or close to V_{OUT}, the converter will use Buck-Boost mode.

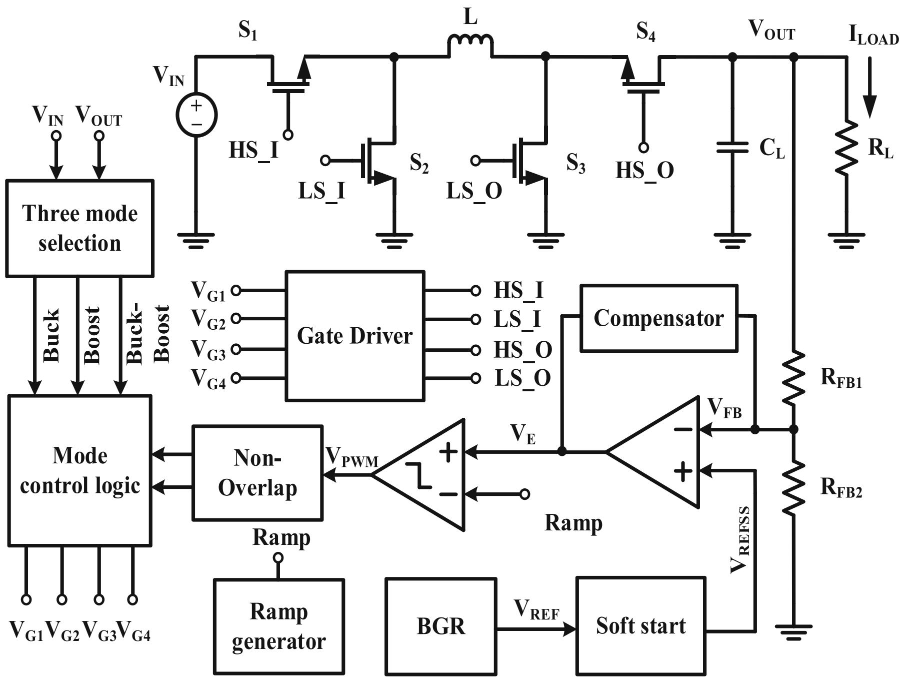

Fig. 2. The proposed Buck-Boost converter with Three-mode Selection.

2.2 Three-Mode Selection Circuit

In practice, the input voltage waveform has a small slope and may fluctuate. The bandgap reference's output voltage is likewise prone to variations, resulting in an unstable condition during transitions between operating modes. This instability during mode switching could result in increased leakage current through the switching transistor, which could lead to lower efficiency or malfunctions that adversely affect output voltage regulation. To eliminate the instability during mode switching and improve the overall performance of the converter, reference [17] presents an approach that uses a fixed output architecture. However, this architecture is not suitable for non-fixed output architectures, which limits the flexibility of the converter. Another technique presented in reference [15] uses a digital controller to monitor the operation of the converter. However, this approach can't work when faced with the challenge of handling high load currents.

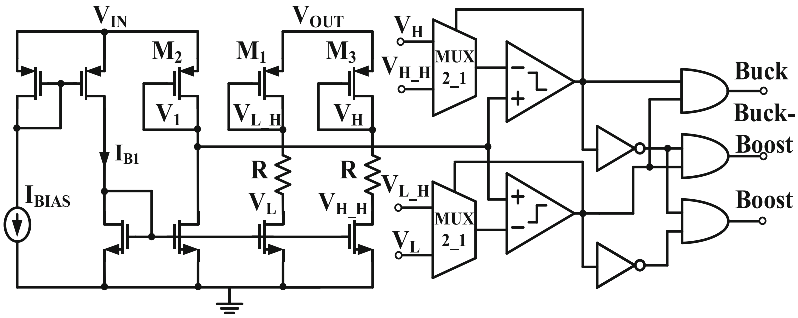

Fig. 3. The proposed three-mode selection circuit.

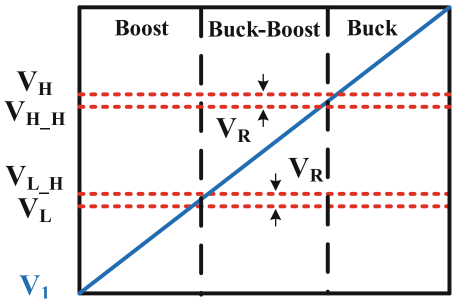

Fig. 4. Three-mode operation diagram.

To achieve the dual goal of operating with a wide load range while achieving high performance, the three-mode selection circuit described in Fig. 3 is proposed as a solution. The core of this three-mode selection circuit consists of two separate blocks. The first block generates a comparison signal from the magnitude values of V_H, V_L and V_1; V_L is designed to be lower than V_H. On the other hand, Conversely, the second block furnishes the signals required to enable the selection among three operational modes:

Buck-Boost, Buck and Boost. As can be seen in Fig. 4, V_{OUT} is converted to V_H, V_{H_H}, V_L and V_{L_H}; similarly, V_{IN} is converted to V_1. For the converter to go from Buck-Boost to Buck mode, the input voltage V_1 must exceed V_H. To return from Buck mode to Buck-Boost mode, V_1 must fall below V_{H_H}. When the converter transitions between Boost and Buck-Boost modes, the same thing happens. The integration of this circuit greatly improves the adaptability and flexibility of the adapter and provides an optimal solution for handling changing load conditions while maintaining optimum performance.

3 Results and Discussions

The proposed chip was developed and implemented on the CMOS 0.18 μm process. The converter utilises off-chip components with a 1μH inductor and a 44 μF capacitor. The function of the converter was verified with an adjustable V_{IN} of 2.5 V to 5 V, V_{OUT} of 3.3 V and a 1 MHz switching frequency. The layout of the proposed chip shows in Fig. 5. The chip has a total area of 455 μm × 380 μm.

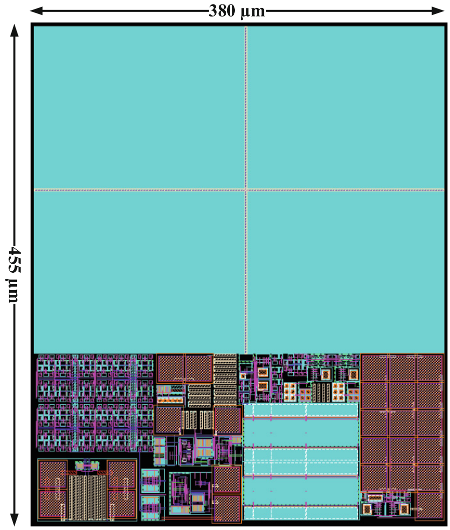

Fig. 5. The layout of the proposed converter.

The simulation results are shown for three modes: Boost, Buck-Boost and Buck. Figure 6 depicts the control voltage of the various transistors in the Buck mode. As mentioned in the previous section, with Buck mode, transistors S_4, S3 is always ON, OFF respectively, and transistors S_1 and S_2 switch over. The output of the converter is 3.3 V, even if V_{IN} is 5 V. Figure 7 depicts the control voltage of the various transistors in the Buck-Boost mode and the respective V_{IN} and V_{OUT}. V_{IN} is close to or equal to V_{OUT}, the Buck-Boost mode is enabled, all transistors switch to control V_{OUT} to 3.3 V. Figure 8 depicts the control voltage of the various transistors in the Boost mode. When the Boost mode is selected,

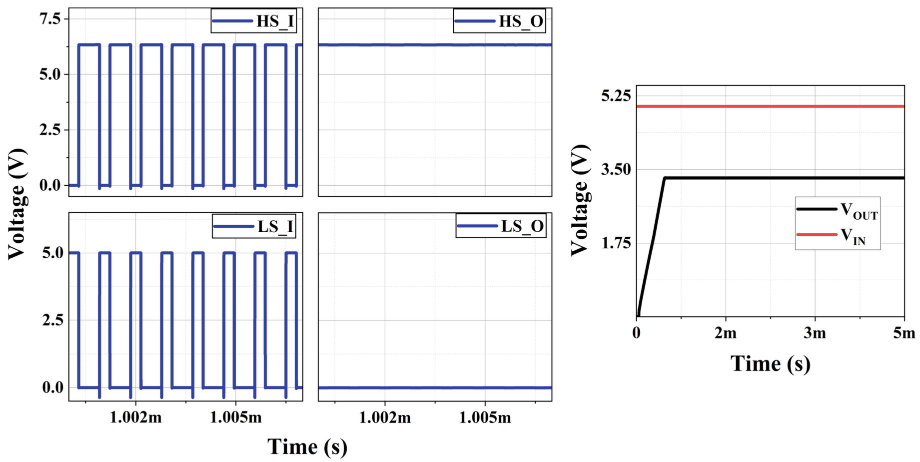

Fig. 6. The simulation results with $V_{IN} = 5$ V, the converter works in Buck mode and $V_{OUT} = 3.3$ V.

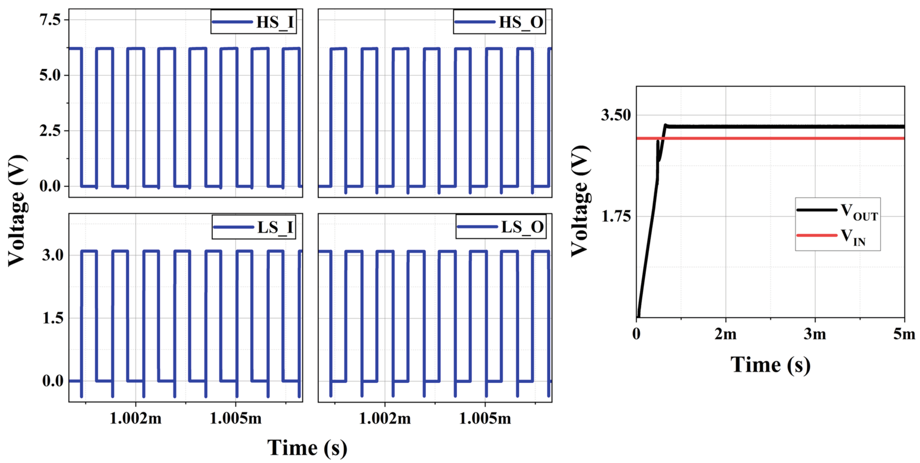

Fig. 7. The simulation results with $V_{IN} = 3.1$ V, the converter works in Buck-Boost mode and $V_{OUT} = 3.3$ V.

transistor S_1 is always ON and S_2 is always OFF and transistors S_3 and S_4 switch over. The input of the converter increases from 2.5 V to the desired output of 3.3 V. The converter's simulation results reveal that V_{IN} is 2.5 V, the converter is in Boost mode, with a V_{OUT} of 3.3 V and a duty cycle of 24.2%. Figure 9 depicts how the converter functions in three modes throughout the whole input voltage range of 2.5 V to 5 V: Boost, Buck-Boost and Buck, with voltage ripple values of 4 mV, 29 mV and 21 mV respectively. The output voltage has an overshoot of 75 mV during the mode change. Figure 10 shows the proposed converter's power conversion efficiency in three different operating modes. The results show that the power level remains consistently high in

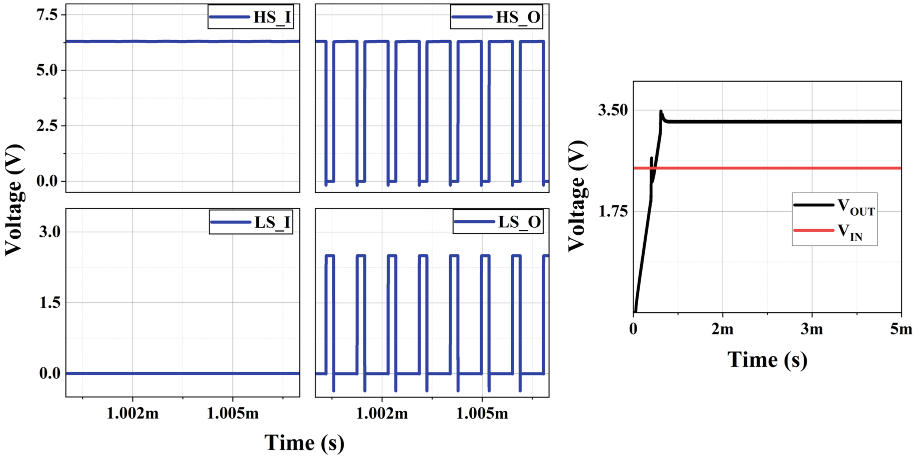

Fig. 8. The simulation results with V_{IN} = 2.5 V, the converter works in Boost mode and V_{OUT} = 3.3 V.

the different modes, even at different load currents from 100 mA to 800 mA. Table 1 gives a detailed overview of the proposed converter's performance compared to previous studies.

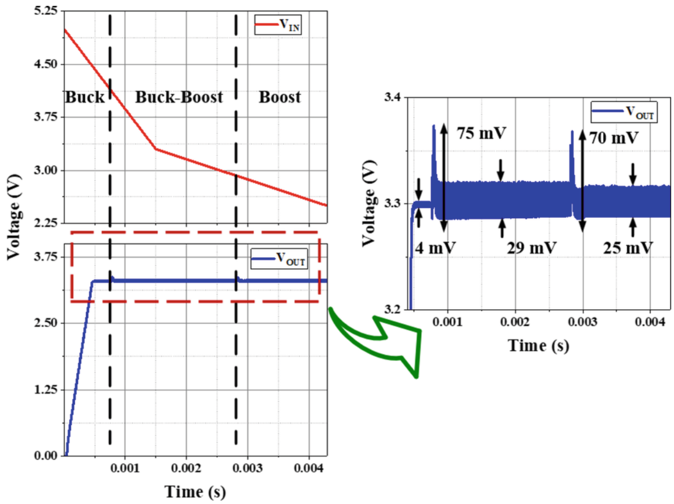

Fig. 9. Converter operation with V_{IN} range from 2.5 V to 5 V.

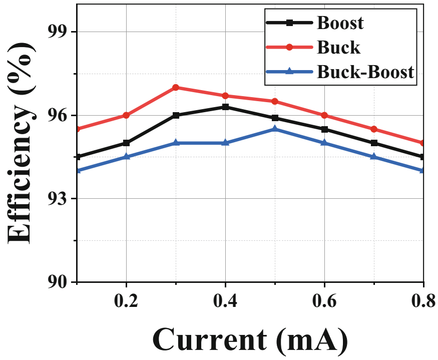

Fig. 10. The proposed Buck-Boost converter's power conversion efficiency.

Table 1. Comparison of performances with other works.

	[13]	[16]	[15]	[14]	[18]	This work
Tech. (μm)	0.18	0.18	-	0.25	0.18	0.18
Modes	A	B	A	A	B	B
Efficiency (%)	89.3	94.8	85.5	91	91	97
Freq (MHz)	0.5	3.2	1	5	2.5	1
Input Range (V)	1.8	3–8	2.5–4.5	2.5–4.5	2.7–5.5	2.5–5
Output (V)	−4	5	3.3	2–4	2–5	3.3
Max. I_{LOAD} (A)	0.005	0.5	0.5	0.4	2	0.8

A: Mode Buck-Boost; B: Mode Buck/Boost and Buck-Boost.

4 Conclusion

The architecture proposed in this article is the optimal choice for battery-powered applications that require high energy conversion efficiency and longer battery life. With the design of a three-mode selection circuit, the converter is adaptable and can easily switch between the three modes: Buck, Buck-Boost and Boost without significant performance degradation. In addition, the use of a soft-start circuit helps to limit the inrush current, which increases reliability and protects sensitive components. The proposed chip was developed and implemented on the CMOS 0.18 μm process. The converter regulation maintains a stable V_{OUT} of 3.3 V over V_{IN} range of 2.5 V to 5 V, while providing an output current range of 100 mA to 800 mA. The maximum efficiency is 97%. The total area of the chip is 455 μm × 380 μm.

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