An Embedded Digital Multi-channel Analyzer for Radiation Detection Based on FPGA

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Abstract. In recent years, digital processing algorithms have been widely applied in spectrum processing applications. Besides, FPGA technology, thanks to its undeniable advantages in flexibility, high integration, and cost-effectiveness, is seriously considered as a practical platform for the realization of embedded digital signal processing (DSP) systems.

This work conducts a study on the practical implementation of Digital Multi-channel Analyzer (DMCA) based on reconfigurable hardware (FPGA). We proposed a modular reconfigurable DMCA design that is ready to be integrated into portable radiation detecting equipment and is still capable to handle high-speed signal sampling as well as could be extended to further functions such as remote sensing and classifying. This module could be integrated into the real-time radiation monitoring system. The algorithms of pulse shaping filter, detecting peaks and spectrum histogram processing are optimized and implemented entirely using available FPGA logic resources.

The design is experimentally verified in a system using Lanthanum Bromide Scintillation Radiation LaBr3(Ce) detector. The results are compared with commercial products (DSPEC of ORTEC), where isotopes ^{137}Cs and ^{60}Co gamma-ray spectra show that its performance partially is superior to the DSPEC in terms of full width at half maximum (FWHM), received and lost count rate, integral nonlinearity. This prototype system is highly promising for the multi-DMCA system in considering performance, cost, and form factors. Regarding resource utilization and performance, the whole design utilizes only 5% LEs, 24% memory resources of 10M50SAE144I7G FPGA from Intel and the DMCA core is capable to handle up to 97 MSPS sampling rates.

Keywords: Digital multi-channel analyzer (DMCA) · DPP · FPGA

1 Introduction

1.1 The Development of Digital Pulse Processing

In recent years, studies of digital pulse processing (DPP) algorithms have shown a valuable benefit over analog signal processing systems. Indeed, the digital approach

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offers designs with high accuracy and good performance, hence, DPP has been widely applied in many applications such as recording, radiation spectrum analysis [1], isotope identification [2], dose rate measurement [3], and so on. Particularly, the DPP approach is well suited for radiation detection algorithms, and it currently is primarily adopted in the nuclear electronics study.

Recent applications of DPP are showing significant improvements over traditional models, various DPP algorithms, such as pulse-shaping filters, peak detector, or amplitude spectral analysis, have been recommended [3–6]. The incorporation of DPP techniques into Digital Multichannel Analyzer (DMCA) allows transforming 512 to 8192 the number of channels [4, 5]. Besides, the adoption of digital improves the system's anti-interference capabilities and increases the sampling rate for real-time processing [5].

The enhanced capability of DPP algorithms essentially comes with an increase in computationally complexity and diversity, thus a high-performance hardware platform is required. In this context, there is a timely need to promptly reform DPP's mapping strategy into the hardware platform and support scalable and modular hardware customization for specific applications without sacrificing design functionality and performance. Among the available platforms, FPGA is the widely applied selection in addition to using the traditional off-the-shelf DPPs implementations.

1.2 Reconfigurable Hardware-Based Approaches for DMCA Accelerators

Technology vendors and researchers constantly put enormous efforts to improve FPGA integration, functionality, and performance. State-of-the-art FPGA undoubtedly is an ideal platform for embedding multi-task, heavy-computing, and customized algorithms on the same single chip. FPGA-based multichannel analyzers, in particular, have become increasingly popular thanks to their high reconfigurability, fast response time, and very high energy efficiency [6]. ZENG Weihua et al. in work [6] implemented a 1024-channel DMCA system on EP3C40Q240 FPGA from Intel, which occupies only 30% of the total logic resources. They experimentally showed that ^{137}Cs nuclear signals detected by NaI(Tl) detector have a resolution of ~ 8% and 0,8% integral nonlinearity. Research by Dang et al. [5] successfully implemented 8192-channel DMCA, with 0,23% integral nonlinearity, on EPM7160E FPGA from Intel (32-bit value resolution) for HPGe Detector using 14-bit 62.5 MSPS ADC.

This work presents a design and implementation of the real-time and high-resolution DMCA, specialized for scintillation detectors, based on moderate off-the-shelf FPGA. The combination of the finite impulse response (FIR) for shaping filter, detecting peaks, and spectral histogram processing is optimized to increase throughput, energy resolution, and minimize logic resources of FPGA.

The main contributions of this work are summarized as follows.

- A very resource-efficient and high-performance FPGA-based embedded DCMA design. (combining software for rendering gamma spectra). Our DCMA core could run signal processing and filtering algorithm with the sampling rate up to 97 MSPS and deliver relatively good peak detection efficiency using only 5% logic elements,

24% memory resources on Intel 10M50SAE144I7G FPGA, i.e., significantly better than implementation on [5] and [6].
- This design experimentally tested with a LaBr3(Ce) detector using ^{137}Cs and ^{60}Co radiation sources and has been compared to the results from a commercial detector from DSPEC. The initial results show that obtained results from our low-cost FPGA-based DMCA exhibit almost the same accuracy as DSPEC and is partially superior in terms of full width at half maximum (FWHM), received and lost count rate, integral nonlinearity.
- The proposed DMCA is highly scalable and reconfigure (i.e., using FPGA) and is ready for deploying a full multi-DMCA system-on-chip and/or further extending to complex features such as classification and recognition.

The remainder of this paper is organized as follows: Section 2 introduces the basic background of DMCA. Section 3 presents the results of the simulation system performed on the software. Section 4 proposes a generic design for the digital pulse processing problem on the hardware and describes our FPGA-based implementation details upon this proposed design. Section 5 concludes the paper.

2 Background

Digital Multi-Channel Analyzer (DMCA) includes two parts, the first one is ADC, the main component of radiation measurements and the second is nuclear analysis instruments. The main function of the DMCA consists of three parts [7]: (1) Data acquisition and (2) Data processing, which are performed by hardware, (3) Control and indicator, which are usually performed by software running on computer communicated via standard interfaces such as USB, Ethernet or Serial port.

Signals from the detector in analog spectroscopy systems are being shaped, filtered, and amplified by pulse amplifier module and digitized by the ADC at the end of the processing sequence. Some basic limitations on these systems are the correction and expansion of filter functions, the impact of interference on analog electronic components such as resistors, capacitors, inductors, analog connectors, and high energy consumption.

The digital signal processing system (DSP) is an effective solution to overcome these limitations. In these systems, the signal from the detector is pre-amplified and filtered before being digitalized and subsequent processing are done in the digital domain. Digital processing algorithms are used to filter and optimize the digitized and sampled data. Data are processed by numerical methods to find the peak value and transfer it to the MCA memory for analysis and indication. The functional block diagram of a DMCA is shown in Fig. 1.

Some of the DMCA's outstanding advantages are high processing speed, high throughput, improving resolution and temperature stability, along with its highly configurable capacity, FPGA provides the ability to build and expand filtering functions without changing hardware. Comparable resolution features coupled with significantly smaller overall processing times can be provided by efficient filtering and processing algorithms. This result improves the ability to process high throughput without reducing resolution as in analog spectroscopy systems.

Besides, in DSP-based systems, processing in the digital domain minimizes the uncertainty of shifting and instability normally associated with analog processing. Spectrometers developed based on DSP can provide the ability to load frequencies exceeding 100000 pulses per second with sufficient resolution to obtain a good gamma spectrum [17].

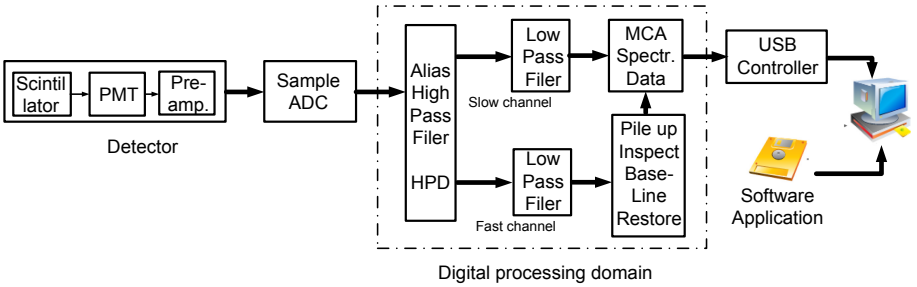

Fig. 1. The functional block diagram of a DMCA

3 DMCA Function Design and Verification

This section describes in detail our DMCA design, which starts with the mathematical model that is rigorously verified by MATLAB-Simulink before actually implemented on hardware (i.e. FPGA).

3.1 The Analytical Model of DMCA

One of the most important factors affecting the quality of the DMCA and a digital gamma spectrometer is the algorithm that shapes (filters) the digitized pre-amplification input signal into a suitable signal form for precisely determines the input signal amplitude. There are three most widely employed algorithms: Gaussian deformation algorithm [9], bipolar pulse deformation algorithm "cups" [10], and the isosceles trapezoidal pulse deformation algorithm, isosceles triangle [10–12]. Each algorithm has certain advantages and disadvantages, in which the optimal and most practically applied algorithm is the trapezoidal pulse transformation algorithm due to the advantages on the signal-to-noise ratio (peak resolution), which is close to optimal for many practical digital spectroscopy systems [8].

In this work, we also applied an isosceles trapezoidal filter, considering that it is well-suited for processing radiation signals and the feasibility for embedded hardware implementation. The filter transfer function can be factorized as follows:

$$F_{TPZ} = \left(1 - \beta z^{-1}\right) * \left(\frac{1 - z^{-R}}{1 - z^{-1}}\right) * \left(\frac{1 - z^{-(R+M)}}{1 - z^{-1}}\right) * \left(\frac{z^{-1}}{R}\right) \quad (1)$$

where constants R specify the rise time duration of trapezoidal pulse and M specify the flat-top duration of the trapezoidal pulse. β is the time constant depending on the input

signal and clock period. After the input samples are filtered and delivered in the form of trapezoidal-shaped signal, its peak amplitude is detected and statistically accumulated for constructing the final histogram. Correspondingly, the DMCA functional diagram is depicted in Fig. 2. In which, the three key components in the digital domain are the Energy filter, the Peak detector, and the Histogram builder. Detailed functional implementations of those components will be described in the following Subsection.

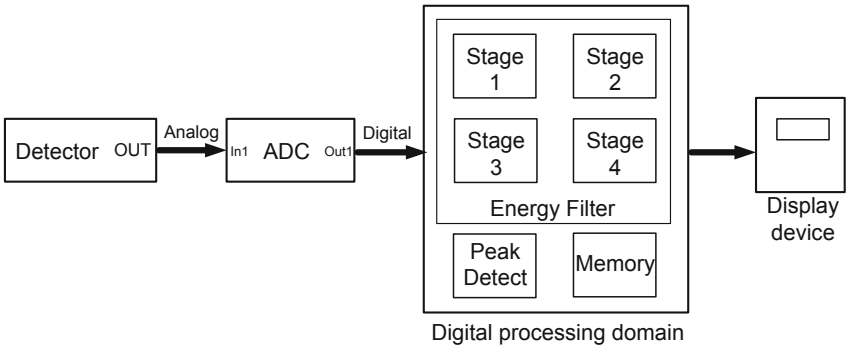

Fig. 2. The structural diagram of a DMCA system

3.2 Design the DMCA Model on MATLAB-Simulink

We further implemented the whole processing DMCA algorithm on MATLAB-Simulink (R2019a version used in this work) for evaluating DMCA-based models and that is being used as the reference design for the subsequent hardware implementation phase.

Based on the model of the digital pulse signal processing system, we proceed to build the DMCA model with three functional blocks, Energy filter, which is used to increase the signal to noise ratio (SNR), minimize the baseline drifts and reduce pileup [14]. The peak detector for measuring the signal amplitude and the Histogram builder for constructing the final amplitude spectrum. The trapezoidal pulse shaping block with the transfer function in the complex frequency domain z is represented by formula (1). We divide the Energy filter into 4 sub-filters with the corresponding transfer function. An example of 4-stage filter outputs is illustrated in Fig. 3. The results show that input the signal from the pulse generator on a relatively large noise background, after going through the filter the noise is effectively phased out and the final signal is shaped into an isosceles trapezoidal. The final signal shape greatly reduces the complexity as well as increases the accuracy of the subsequent block.

Peak detector: As from the name, this block uses a threshold discriminator to treat the trapezoidal signal after the filter. Once the peak level is detected, this block creates a logic pulse for measuring the amplitude and sends this value to the histogram builder.

Histogram builder: In the histogram builder the detected peak value is accumulated and stored into a histogram memory. Specifically, when there is an event that needs to be stored, the pulse amplitude is used as the address for access and increases the current

value in the memory cell by one. i.e., the contents of the cell are retrieved, added by one, and saved back to the same address. This process is performed for sufficient time (in this case, ~ 1 ms) the histogram will be constructed and stable. Figure 4 shows an example of the final histogram using a DMCA model on MATLAB-Simulink.

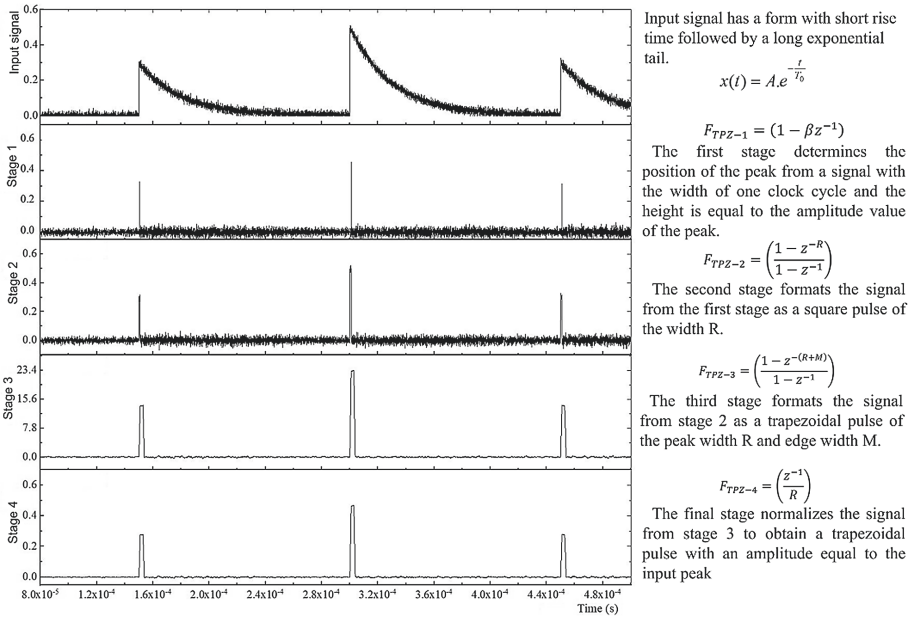

Fig. 3. Simulated signal transformation corresponding to four filter stages.

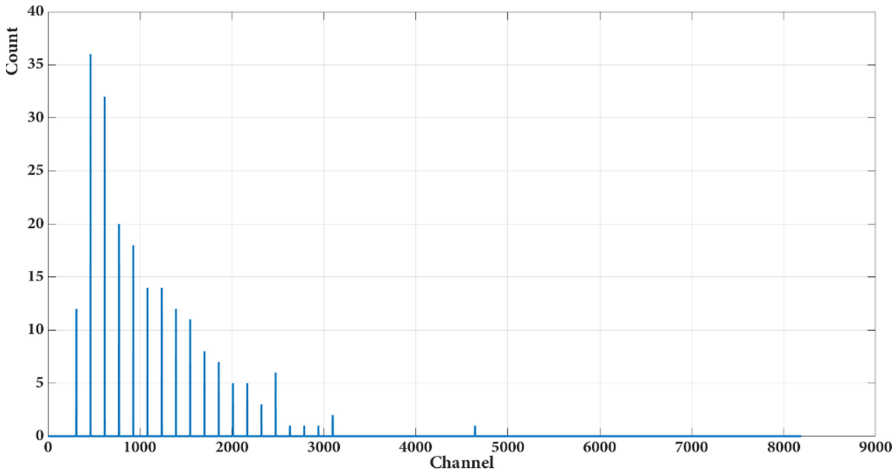

Fig. 4. Histogram of simulation signals.

4 Design of DMCA System

4.1 The Structural Design of the DMCA System

Based on the functional block in the previous section, the hardware implementation block diagram is constructed in detail (see Fig. 5). As can be seen from the figure, signals from the preamplifier (usually integrated inside the detector) are transferred to the sampling circuit and digitized by a fast ADC [13]. The ADC output signal will be processed by digital circuits entirely embedded in FPGA. This circuit consists of Energy Filter, Peak detector, and the Histogram builder. The output signal of the Energy Filter is transferred to peak-detection circuits, consist of a differentiator, a level discriminator, a peak counter, and a pile-up detector block and finally used to create the energy spectrum in Histogram builder. The latter consists of pulse height analyzer, controlling interface, and memory.

All those processing is encapsulated in VHDL/Verilog. The whole design is simulated by (Altera Quartus) functionally verified before porting to FPGA for experimental measurement. Finally, for presenting the result, we added a USB driver circuit on FPGA to communicate and transfer the final histogram to a PC. This part in the practical scenarios can easily replace by a more compact alternative (e.g. integrated LCD) or data can be wirelessly transferred to the end-user components or even to the cloud. The latter scenario is particularly necessary when the sensing area is not accessible due to radiation hazards.

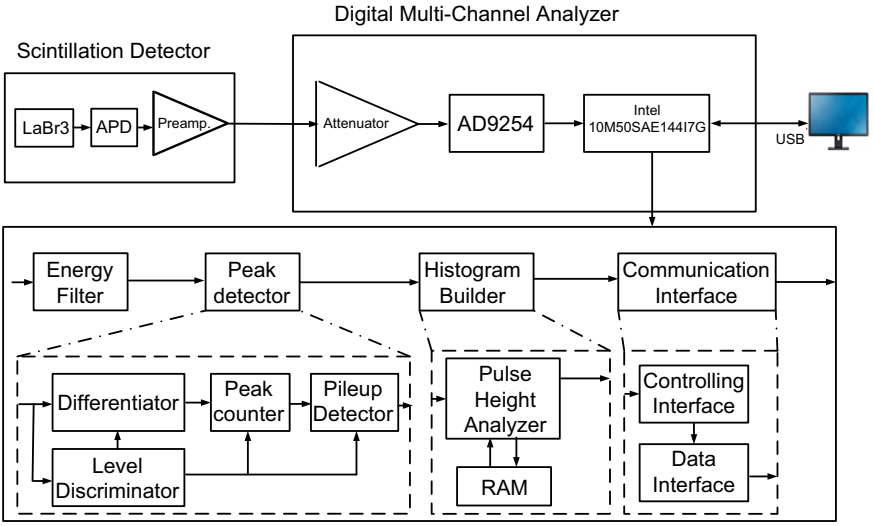

Fig. 5. Block diagram of the DMCA system.

4.2 Scintillation Detector and the Analog Frontend

The scintillation detector [15] consists of a scintillation crystal, an avalanche photodiode (APD) to convert the light from the scintillation crystal into electrical pulses, which is

amplified by an integrated pre-amplifier circuit. In this work, we employed a detector with LaBr3(Ce) crystal with a size of $10 \times 10 \times 30$ mm, APD type S8664–1010, charge-sensitive pre-amplifier type eV5093. For the analog frontend, we adopted commercial 14-bit AD9254 ADC from Analog Device [16], which has a maximum sampling rate of 150 MSPS. The ADC converts analog signal amplitude from $-1 \div +1$V, the 14-bit parallel output which is directly fed to FPGA inputs.

4.3 Pulse Processing System Design

The incoming signal from the detector is digitized by ADC and the digital samples are passed directly to the digital pulse processing circuit inside FPGA. Especially to the input of the pulse-shaping filter of the Energy filter. After the energy filter, the signal is shaped into a series of trapezoidal and passed through the threshold discriminator to create a logic pulse for controlling subsequent functional blocks, including differentiator, peak counter, pileup detector, and pulse height analyzer. The differentiator is used to reveal peaks and detect pileup. While the signal larger than a given threshold, the peak counter counts the number peak in one pulse cycle by using a logic pulse from a differentiator. Spectral storage memory is configured from Dual Port Random Access Memory-DPRAM, which is built into the FPGA. The memory is organized with 13 bits address bus, capacity 8192 locations; 32 bits data bus, recording range $0 \div 2^{32}$–1 count; and includes memory select signals, read/write data control bus.

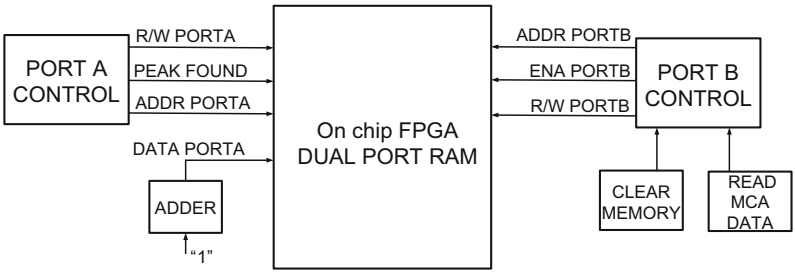

Fig. 6. Block diagram of memory and interface.

Block diagram of memory and interface is shown in Fig. 6. When there is an event that needs to be stored, the pulse amplitude is used to generate the memory address, the contents of the cell are retrieved to add a count before updating to the same location. The above operations are performed with port A. The memory clear operations, reading spectrum analysis results are performed independently via port B through the interface between this port and the computer.

4.4 FPGA Implementation and Experimental Results

The design in previous Sections after functional evaluation by logic simulation has been fully ported into a commercial FPGA board using Intel Max 10 FPGA. We also

developed an in-house software program on PC to communicate with the board for reading the final histogram and plot it on the computer. The hardware implementation on FPGA is summarized in Table 1.

Table. 1. Analysis and synthesis summary.

	This work	[5]	[6]
Chip Family	Intel MAX 10	Intel MAX 7000	Intel Cyclone III
Device	10M50SAE144I7G	EPM7160E	EP3C40Q240
Logic resources	2,380/49,760 (5%)	1,050/3,200 usable gates	11,880/39,600 (30%)
Total pins	24/101 (24%)	–	–
Total memory bits	423,936/1,677,312 (25%)	–	–
Multiplier	3 / 288 (1%)	–	–
Max frequency	97 MHz	62.5 MHz	65 MHz

The results obtained found that the hardware resources used by the logic elements, memory elements, RAM, and DSP are reasonably small, i.e., occupies only 5% (2,380 LEs on 10M50SAE144I7G), which is much smaller than the DMCA design in [6][1]. The result indicates that our design is capable to extend to multiple channels (i.e., multiple ADCs and detectors). The maximum frequency of this design can up to 97 MHz, which allows to speed up the algorithm with real-time tasks.

Furthermore, we conducted the experimental tests on the implemented DMCA. In this test, we use the available LaBr3(Ce) detector in our Institute of Chemistry and Environment. The detected signal is passed through the AD9254 daughter board before processing in FPGA. The final recorded spectra are sent to the computer via a USB interface. We use isotopes ^{137}Cs and ^{60}Co as the calibration sources for experimenting. Figure 7 (a) shows the histogram of the natural background (no active radiation), (19, 20) shows the recorded gamma spectra of ^{137}Cs and ^{60}Co, respectively. The graph shows that the spectrum obtained is consistent with the radioisotopes reference sample results (Fig. 8).

Finally, the functionalities of the DMCA were compared to an ORTEC commercial digital system (DSPEC). The output of the detector has simultaneously connected to DMCA and DSPEC. The interaction rate in the detector was adjusted by using ^{137}Cs and ^{60}Co sources in a different activity and also by adjusting the distance between the source and the detector to achieve the desirable count rates.

An important characteristic of a multi-channel analyzer is the width of the total energy peak. It is usually measured on the full width half maximum (FWHM) [18]. In an ideal case, pulses caused by monoenergetic radiation would all be the same height, and the multichannel analyzer would display a single line that would represent the radiation

[1] We did not compare resource utilization of our work with [5] since that work used CPLD device that is not based on Logic Element primitives.

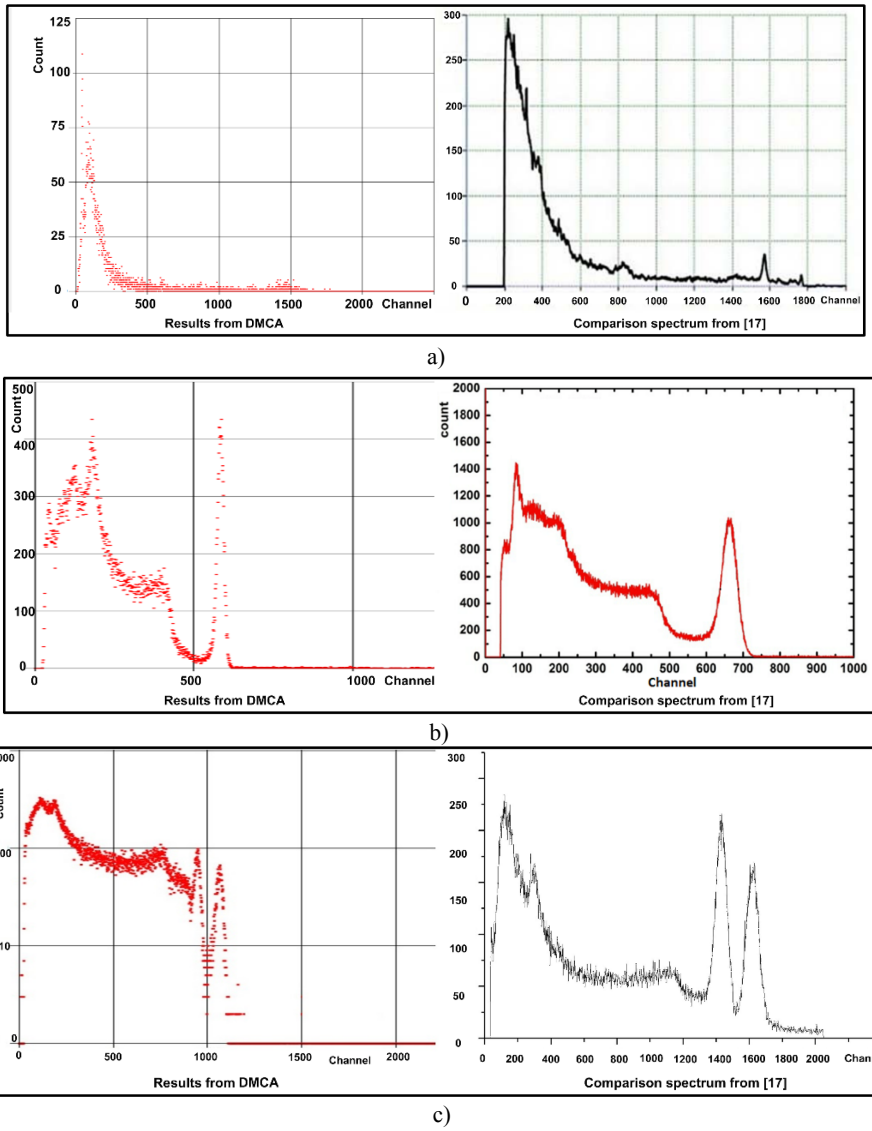

Fig. 7. The display of the spectrum on the computer (left) and comparison spectrum (right) [17], a) Naturally occurring background radiation, b) Gamma spectrum of ^{137}Cs source; c) Gamma spectrum of ^{60}Co source.

energy. In practice, a peak with a measurable width is observed. To evaluate the quality of the DMCA, the FWHM must be as small as possible.

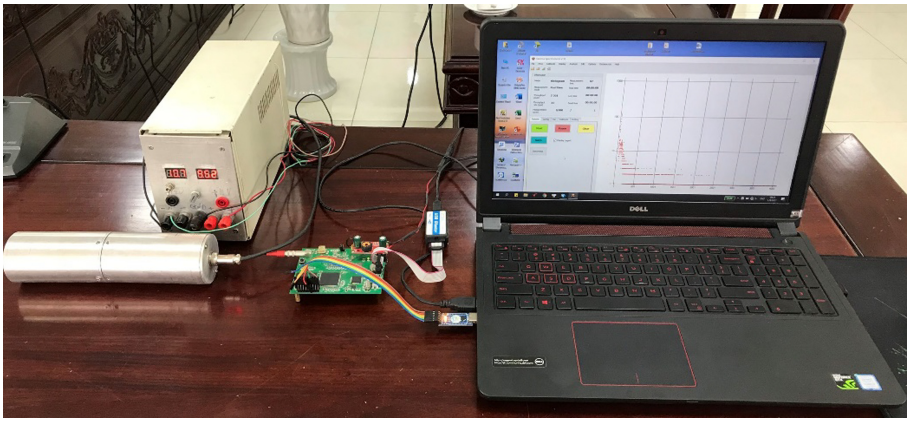

Fig. 8. Design testing on FPGA board

The spectra and spectroscopic parameters of ^{137}Cs and ^{60}Co sources collected by DMCA and DSPEC are shown in Fig. 9, the upper part is different spectra which were measured simultaneously at count rates of 25kcps, 30kcps, and 35kcps; and the lower part is the difference of spectroscopic parameters. The graph shows that the spectrum obtained between two digital multichannel amplitude analyzers does not differ much in terms of spectrum shape. However, DMCA's FWHM is about 10% better than DSPEC jr. 2.0, 15% better at peak elevation. The peak area of ^{60}Co obtained by DMCA was about 5% more, while the peak area of ^{137}Cs was about 7% more than DSPEC jr. 2.0 at counts of 25kcps and 30kcps.

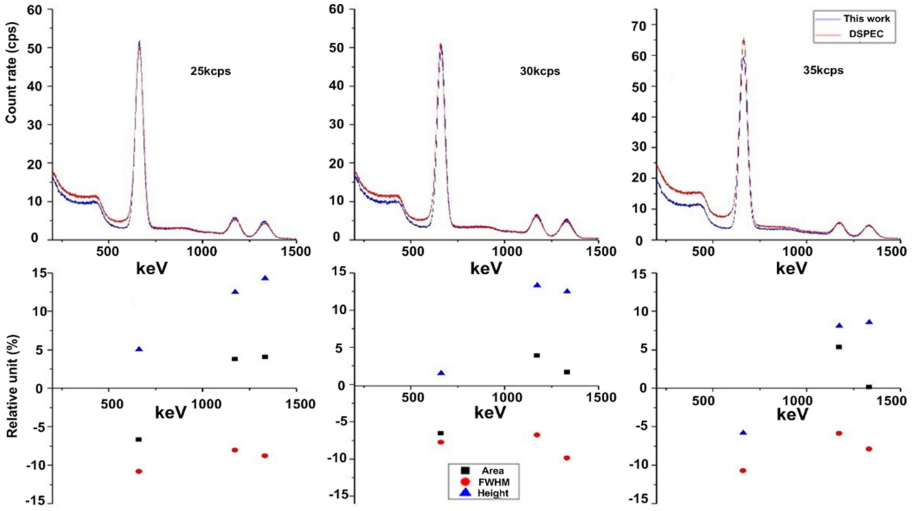

Fig. 9. The spectra of ^{137}Cs and ^{60}Co sources were collected by DMCA and DSPEC.

Another important DMCA parameter examined is integral nonlinearity ($INL = CH_{max}/CH_{total}$) [5], where CH_{max} is the maximum difference (channel unit) of the spectral peak position relative to the theoretical linear line over the entire measuring range; CH_{total} is the number of channels of the DMCA. Using Gwintek standard pulse generator GDS 303587, the survey results of the spectral peak position dependence when changing input signal amplitude are shown in Fig. 10. According to the experimental data, the integral nonlinearity of DMCA is 0.1367%.

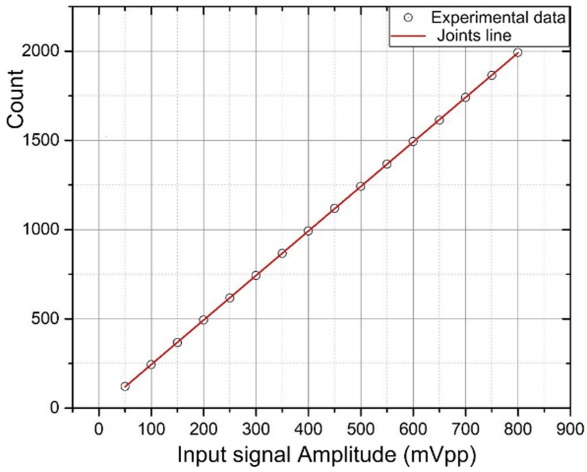

Fig. 10. Spectral peak position dependence on the input signal amplitude.

5 Conclusion

This study presents an embedded reconfigurable DMCA that has been systematically designed and experimentally verified in conjunction with the LaBr3(Ce) scintillation detector. The major results indicate that our design exhibits the almost equivalent performance of the commercial off-the-shelf DSPEC jr. 2.0 DMCA while experimenting on standard isotopes of ^{137}Cs and ^{60}Co.

Our working prototype has been fully developed on FPGA that offers a small form factor, low-cost, and low-energy DCMA, thus, being ready embedded in practical systems. Also, regarding resource utilization, our design not only superior some prior arts in the area-efficiency but the reconfigurable platform (FPGA) allows further deploying more features using complex data processing algorithms such as on-device classification and recognition. The latter paved the way for design a new class of smart DCMA where intelligent computing tasks can be performed right at the analyzer. It is also feasible to adopt this design for different application scenarios, e.g., by integrated wireless module, this device can interact in the radiation-/bio- hazard environments or the devices can push the detected data directly to the cloud as an IoT device for storing and further analyzing and processing at a larger scale.

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