University Innovation and Entrepreneurship Education Resource Sharing System Based on Cloud Service Platform

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Abstract. There may be situations of resource dispersion, information isolation, and duplicate construction among different universities, resulting in low efficiency and uneven quality of resource utilization. Therefore, studying how to establish a resource sharing system for innovation and entrepreneurship education in universities is of great significance. The conventional university innovation and entrepreneurship education resource sharing system mainly uses the Web Server system to process service requests, which is susceptible to the impact of service binding and retrieval, resulting in long system query time. Therefore, it is necessary to design a new university innovation and entrepreneurship education resource sharing system based on the cloud service platform. The hardware part is designed with FPGA chips, IDE controllers, and PIO transmitters. The software part is based on the cloud service platform to build an education resource sharing scenario, construct an education resource sharing architecture, and design an innovation and entrepreneurship education resource function module to shorten the time for education resource sharing. Integrating hardware and software to achieve resource sharing of innovation and entrepreneurship education in universities. The system testing results indicate that under the preset testing environment, the performance of the university innovation and entrepreneurship education resource sharing system designed in this article based on the cloud service platform is good, and all functional modules have passed the system testing, proving that the designed education resource sharing system has a certain degree of reliability and has made a certain contribution to promoting the development of university innovation and entrepreneurship.

Keywords: Cloud Service Platform · Universities · Innovation · Entrepreneurship · Sharing of Educational Resources

1 Introduction

The research background of the resource sharing system for innovation and entrepreneurship education in universities lies in the current problems of dispersed, isolated, and repetitive construction of innovation and entrepreneurship education resources among universities [1]. To address these challenges, establishing a resource sharing system is of

G. Gui et al. (Eds.): eLEOT 2023, LNICST 543, pp. 139–155, 2024.
https://doi.org/10.1007/978-3-031-51465-4_10

great significance. This system can integrate innovation and entrepreneurship education resources from various universities, providing comprehensive resource support, including high-quality teaching content, entrepreneurship cases, and mentor guidance [2–4]. Through resource sharing, the cultivation of innovation and entrepreneurship abilities can be promoted, and the diversity of teaching quality and methods can be improved. At the same time, resource sharing systems can also improve resource utilization efficiency, avoid duplicate construction and resource waste [5]. In addition, the system also promotes innovation and entrepreneurship research and practice, providing a broader platform for academic exchange, cooperation, and incubation and transformation of innovation and entrepreneurship projects [6]. In summary, studying the resource sharing system for innovation and entrepreneurship education in universities is of great significance for improving the quality of innovation and entrepreneurship education, promoting the cultivation of students' innovation and entrepreneurship abilities, and promoting innovation and entrepreneurship research and practice.

Reference [7] proposed a teaching resource sharing system based on Microservices architecture, and built an education resource cloud sharing architecture based on Microservices architecture. On this basis, Design education resource collection module, education resource attribute annotation module, education resource storage module and education resource retrieval module, provide users with education resource collection, upload, storage and retrieval services, and realize the operation of university education resource cloud sharing system. Reference [8] proposes an education resource sharing system based on the VEM framework, which consists of four levels: preprocessing, feature extraction, classification, and sharing of teaching resources through collaborative work. In the preprocessing stage, redundant information is removed to reduce system storage space. The feature extraction module uses the semantic Adjacency matrix to calculate the feature value of the vocabulary in the resource and select the vocabulary with larger feature value. In the classification module, the Hyponymy and hypernymy is used to build a classification framework, calculate the relationship strength between each word pair, and achieve classification according to the different strength. Store the resource numbers that have completed the classification separately, and teachers can directly search for the completed resource sharing. Although the above two systems can achieve the sharing of educational resources, they have the problem of long sharing time and are difficult to meet the user's usage needs.

A university innovation and entrepreneurship education resource sharing system based on cloud service platform is proposed to address the problems existing in the existing education resource sharing system. By combining FPGA chips, IDE controllers, and PIO transmitters, the sharing function of the system is achieved. The software part achieves rapid sharing of educational resources by building sharing scenarios and building a cloud platform sharing architecture.

2 Hardware Design

2.1 FPGA Chip

Educational resource sharing system uses FPGA chip as processing chip.In addition to the FPGA configuration chip and the memory chip necessary to run the SOPC system, peripheral interfaces related to system functions are added to the peripheral devices [9]. Most processing tasks and peripheral drivers in SOPC system can be implemented in FPGA chip, and its composition block diagram is shown in Fig. 1 below.

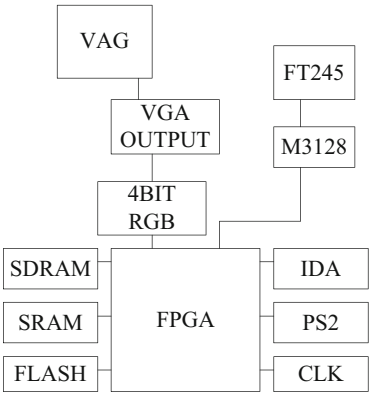

Fig. 1. FPGA chip composition block diagram

As shown in Fig. 1, FPGA is the core processor, and all designs in this paper are based on FPGA.EPCS4, M3128, FT245 and USB BLASTER form the configuration circuit of FPGA.EPCS4 stores the load file of FPGA. After the system is powered on, the system will transfer the load file into the FPGA to generate logical circuits. FLASH is used to store the running code of NIOS II in case of power failure. When the system is powered on, NIOS II starts from FLASH and loads the code into memory. SDRAM and SRAM are the memory of NIOSII soft core runtime. The IDE adapter cable converts the signal sequence to the sequence required by the IDE hard disk and connects it to the hard disk. VGA and PS2 are used for data display and external control of the system to complete human-computer interaction [10].

This paper uses the FPGA development board DE1 as the development platform. The DE1 development board is a multi-functional FPGA development board developed by Youjing Company. The FPGA model it uses is the EP2C20 of Cyclone II series. There are abundant peripheral interfaces on the DE1 development board, which can connect a variety of external devices, including audio interface, VGA interface, RS232 interface, SD card interface and PS/2 interface. In addition, the DE1 development board also provides two sets of 40 pin general GPIO interfaces, which enables it to expand a variety of functions. In addition, the crystal oscillator on the DE1 development board can provide 50 MHz, 27 MHz and 24 MHz clocks, which can meet the requirements of general design.

The FPGA adopts Cyclone II EP2C20 of Altera Company, which has about 18000 logic units, 240000 bit on-chip memory, four phase-locked loops and 52 9-bit hardware multiplier memories. Its logic resources are rich and cost-effective. The main modules involved in this design are NIOSII. CPU, various peripherals in SOPC system, IDE interface controller and VGA controller. After testing, the total logic resources used in these four parts account for about 50% of all FPGA resources, so the logic resources of FPGA can meet the system requirements and leave a large space for expansion.

Another important parameter of FPGA is the capacity of on-chip memory. The on-chip memory of Cyclone II series is generally insufficient. Because of the need to open up memory for two CPUs, and the implementation of NIOS II CPU also requires a lot of on-chip memory. Therefore, off chip SDRAM and SRAM are required. The SRAM used by the DE1 development board is 512 K bytes, and the SDRAM is 8M bytes, which can meet the system requirements.

2.2 IDE Controller

IDE interface is a hard disk interface protocol jointly defined by CDC, Compaq and Western Digital and finally recognized by the American National Standards Institute, also known as ATA/ATAPI interface protocol. Due to the continuous development of technology, people have higher requirements for the transmission speed of stored data, which leads to many problems in the use of ATA/ATAPI interface protocol. After continuous improvement, a total of 7 versions have been produced, namely ATA/ATAPI-1 to ATATAPI-7.Among them, ATATAPI-7 has not been widely used, and only Maxtor has launched a series of hard disks adopting ATA/ATAPI-7 standards. To maintain product compatibility, each new version is based on the old version and can support subsequent versions.

ATA/ATAPI - 6 is also called ATA/ATAPI 100 because it can theoretically make the transmission rate of the hard disk reach 100MB/s. It can use 40 pin and 80 pin transmission cables, and ATA/ATAPI-6 protocol still supports lower versions. Devices using ATA/ATAPI-4 and ATA/ATAPI-5 protocols do not need to update the version, but can directly use the ATA/ATAPI-6 interface. This not only makes users who have already invested no longer have to waste money to update their equipment, but also enables equipment manufacturers to update product versions without losing their original customers. In this way, their enthusiasm for using new technologies has been greatly improved. This has greatly promoted the development of ATA/ATAPI protocol “.

The minimum unit of hard disk data storage is sector, that is, at least one sector must be read or written every time data is read or written. The addressing mode of hard disk sector includes physical addressing mode (CHS addressing) and logical addressing mode (LBA addressing).Physical addressing refers to addressing using the physical storage form of hard disk. The physical address consists of “track number - head number - sector number”. Logical addressing refers to numbering the sectors in the hard disk from 0, and the sector number is the logical address.

ATA/ATAPI-6 protocol adopts LBA addressing mode. The conversion of head and track in physical addressing will take a long time. LBA addressing can avoid this problem. LBA addressing speed is faster when carrying out mass data transmission. ATA/ATA-6 protocol specifies the mechanical parameters of IDE interface, and the connection interface of IDE controller is shown in Fig. 2 below.

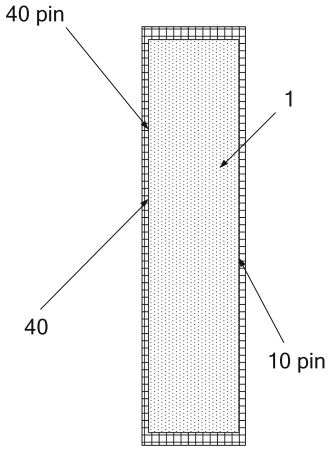

Fig. 2. IDE controller connection interface

It can be seen from Fig. 2 that the left part is the signal line, with a total of 40 pins, of which 20 pins are not connected. The right part is the hard disk jumper, with ten pins in total. The jumper is used to set the number of the hard disk in the PC to determine whether the hard disk is the primary hard disk or the secondary hard disk. The connection of the hard disk jumper of different manufacturers is different. Only one hard disk is used in this article, so the hard disk is set as the main hard disk. The hard disk used needs to be shorted with jumper caps for pin G and pin H to indicate that the hard disk is the main hard disk. If you want to set the hard disk as a slave hard disk, you need to use a jumper cap to short the C and D pins.

The host sends commands and relevant parameters to the disk device controller through registers, and controls the disk device controller to execute relevant commands. The host can master the command execution of the disk device controller by reading the contents of the register.CS0, CS1, DA2, DA1, DA0 are the address signals of the I/0 register, and the storage parameters are shown in Table 1 below.

Table 1. Deposit Parameters

CS0	CS1	CS2	CS3	CS4
N	A	N	N	A
A	N	A	A	A
A	N	N	N	N
A	N	A	A	N
A	N	N	N	A
A	N	A	N	A
A	N	A	N	N
A	N	N	A	A
A	N	N	A	N
N	N	X	X	X

Table 1 shows that there are as many as 63 commands defined in ATA/TAIP-6 protocol, and some of them are only applied in specific transmission modes. Here we only introduce the four main commands used in this article: READ SECTOR (S), WRITE-SECTOR (S), READ DMA, and WRITE DMA. The command codes of the four commands are 20H, 30H, C8H, and CAH. To execute the above commands, the system needs to first write the required parameters to the relevant registers, and then write the command values to the command registers.

IDE hard disk has two transmission modes: PIO and DMA. DMA transmission mode can be divided into two types: multi word DMA transmission mode and serial DMA transmission mode. Register transmission must use PIO transmission mode, and data transmission can use both modes. Each transmission of PIO mode group data needs to achieve a complete preparation timing and end timing. The actual time of data transmission is only a small part of the whole time sequence. A small amount of data in PIO mode has little impact on the speed, but it will greatly reduce the transmission efficiency when a large amount of data is transmitted. And every transmission requires CPU participation, which will take up a lot of CPU time, reducing the overall efficiency of the system.

PIO transmission mode can be used when the amount of data is small.DMA mode only needs to realize the preparation timing and end timing once for each group of data transmission.Its preparation timing and ending timing are more complex than PIO mode.The advantages of DMA transmission are not obvious when the amount of data is small, but the efficiency and speed of transmission will be greatly improved when the amount of data is large.According to the above discussion, the system adopts the mixed use of PIO mode and DMA mode.This is because the design task is to store a large amount of data to the disk, while reading data only needs to be completed in the PC.Therefore, when storing data to the hard disk, the amount of data is large, and DMA transmission mode is adopted.When reading data from the disk, the amount of

data is small, and PIO transmission mode is adopted. The structure block diagram of IDA controller is shown in Fig. 3 below.

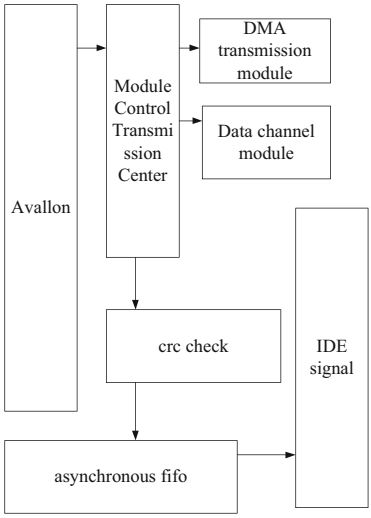

Fig. 3. IDA Controller Structure

It can be seen from Fig. 3 that the synchronization design makes the timing control of the whole system more simple, and it is easy to avoid many timing problems. If multiple clocks are used, the same clock source and cabling resources cannot be used for cabling during system integration. Different clock sources provide clocks at different times, which will lead to different clock delays between different modules, causing problems with data retention time and reducing data transmission speed. In this design, the whole system uses the same clock, avoiding the clock matching problem caused by using mixed clocks. In addition, the trigger resources of FPGA are very rich, while the combinational logic resources are relatively small. The synchronous design can make full use of the advantages of FPGA.

Avalon bus interface is responsible for communication with NIOS II CPU. This article uses it as an interface for custom peripherals. It is used to receive the control commands and related parameters of the CPU, respond to the read operation of the CPU, and provide the running results of the IDE controller to the CPU. The IDE controller data is converted to the Avalon bus format for transmission. The module control and PIO transmission module is responsible for interpreting CPU commands and controlling the operation of the entire IDE controller. It converts CPU commands into operations that need to be executed. For example, after receiving DMA read commands and sector addresses, it sets the registers that need to be read and written to execute DMA read commands, stores the relevant parameters in the registers, or reads the contents of the relevant registers and judges the operation of the IDE interface controller. As PIO transmission is closely related to the above contents, PIO transmission will also be realized in this module. It includes the realization of register transmission timing and PIO

transmission protocol. After realizing the signal timing required for PIO transmission, it transmits the signal value to the IDE interface module, and controls the transmission outside the IDE interface module.

2.3 PIO Transmitter

The timing used for PIO transmission is the same as that used for register transmission except for the width of the data line. The PIO transmission data line is 16 bits, and the register transmission is 8 bits. The PIO implementation circuit and module control circuit all use register transmission timing. In order to reduce FPGA resource consumption, this design uses the method of module reuse to implement them in one module. In this way, half of the logic resources can be saved, and the transmission speed will not be affected. The module block diagram of the PIO transmitter is shown in Fig. 4 below.

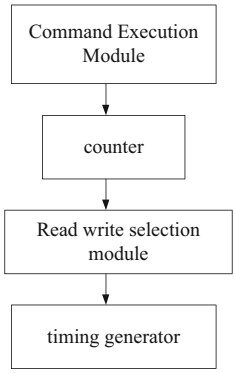

Fig. 4. PIO transmitter module block diagram

As shown in Fig. 4, the module receives information from the following three registers: w_r_ flag is used to receive disk device initialization, PIO read, PIO write, DMA transfer and other operation commands;file_ reg_ _addr is used to receive the address of the register to be operated: addr__reg is used to receive the sector address of the data to be read or written. The command execution module receives CPU instructions and sector address values from the Avalon bus interface, and implements the PIO read, PIO write protocol, and DMA transfer protocol command parameter writing. This module is based on the_r_The CPU command received by the fag register prepares the relevant register parameters required, and controls the timing generation module to store them in the corresponding register or read the contents of the register. The read/write selection module is used to select the data transmission direction. The transmission conversion conditions at this time are shown in Table 2 below.

Table 2. Command transmission conversion conditions

Conversion conditions	Content description
1	The host starts PIO transmission
2	Activate the disk and write PIO transmission commands and parameters
3	Disk device is fully turned on
4	BSY = 0,DRQ = 0
5	BSY = 1
6	BSY = 0,DRQ = 1
7	Interrupt enable is closed and data register reading is completed
8	Data register read incomplete
9	Data register reading completed, execute all commands

It can be seen from Table 2 that combined with the above command transmission conversion conditions, the commands issued by the system can be executed to improve the operating reliability of the system.

3 Software Design

3.1 Building Educational Resource Sharing Scenarios Based on Cloud Service Platform

In the education resource system, it mainly includes two subjects: user group and resource group. The user group is mainly composed of students, teachers and other members of the public, while the resource group mainly refers to a large number of digital education resources existing in the education resource system, such as teaching materials, coaching materials, handout courseware, books and journals, teaching audio and video, exercise books, examination questions, etc. The cloud service platform is a large-scale virtual and extensible platform, which can use infrastructure as IaaS, platform as PaaS and software as SaaS. Therefore, according to the characteristics of the cloud service platform, this paper has built an educational resource sharing scenario, as shown in Fig. 5 below.

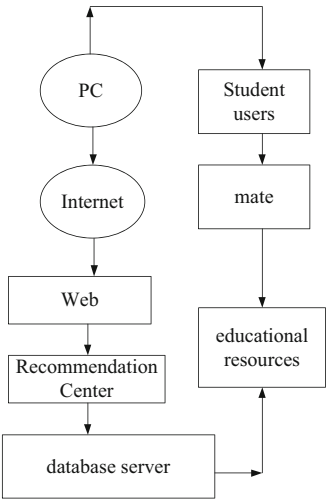

Fig. 5. Educational resource sharing scenario

It can be seen from Fig. 5 that student users are the main body of the education resource system, so they are also the main group using education resources. If you want to recommend resources to students more accurately, you must design a resource recommendation scheme specifically for the characteristics of student user groups. Student users are learners. It is precisely because they need to increase knowledge that they need educational resources, so there is a demand for learning. Different students have different characteristics in terms of learning background, learning style, learning ability, etc., while different educational resources have different characteristics in terms of background information, material type, difficulty, etc. Paying attention to students' personalized characteristics and selecting appropriate resources for them can more effectively improve students' learning efficiency, stimulate students' interest and improve students' learning pleasure, Make students enjoy the learning process more.

Just like the diversity of students' demand for resources, the types of educational resources are also very diverse. The resource model we have established should not only distinguish the differences of resources, but also reflect the basic characteristics of resources. The characteristics of educational resources mainly include background information, material types, difficulty, etc.

The effective information of resources to students is calculated through a series of matching algorithms. We can think that when the amount of effective information of educational resources for student users is relatively high, the student user will be more matched with the educational resources. Students can meet their needs better by learning the resources, so we can recommend the resources to the students. On the contrary, if the amount of effective information of educational resources for student users is relatively low, the matching degree between the two is also relatively low. It is considered that this resource cannot meet the needs of students, so it is unnecessary to recommend this resource. The resource matching similarity can be calculated according to the above sharing scenarios and resource allocation principles $\cos\theta$, , as shown in (1) below.

$$\cos\theta = \frac{b \cdot c}{|b| * |c|} \tag{1}$$

In formula (1), b and c respectively represent resource matching vectors in different Vector space. At this time, in order to measure the correlation between resources, Pearson correlation coefficient $p(x, y)$ needs to be calculated, as shown in (2) below.

$$p(x, y) = \frac{\sum x_i * y_i - n\overline{x_i y_i}}{(n-1)} \tag{2}$$

In formula (2), x_i and y_i respectively represent the correlation vector, n represents the matching dimension, and Hamming distance refers to the total number of different bits of characters at the corresponding position of two strings of the same length. It can also be used to calculate the difference between two vectors. Formula D is shown in the following (3).

$$D = \sum_{i=0}^{n} x_i \oplus y_i \tag{3}$$

In formula (3), the values of each one-dimensional feature of two vectors are character based. It is difficult to calculate the similarity between two vectors with character based values using traditional methods. Here, we introduce an encoding method that represents the strings of each dimension of the vector using the corresponding binary encoding. Therefore, we can assume a binary vector. The calculation equations SI and RI are shown in (4) and (5).

$$SI = \{S_0, S_1, ..., S_N\} \tag{4}$$

$$RI = \{r_0, r_1, ..., r_N\} \tag{5}$$

In formulas (4) and (5), $S_0, S_1, ..., S_N$ represents the resource matching vector before using binary encoding, and $r_0, r_1, ..., r_N$ uses the resource matching vector after using binary encoding. Based on the analysis of the similarity calculation methods of the above vectors, it can be seen that the Pearson correlation coefficient calculation requires at least two overlapping parts of the two vectors. When the overlapping parts are less than two, the Pearson correlation coefficient cannot be calculated, This is very unfavorable for calculating the correlation between two vectors; Although cosine similarity can be used to calculate the similarity of any two n-dimensional vectors, its solving process is very complex; The calculation of the Hamming distance of the two vectors is very simple, and the accuracy of the results is also very high. Therefore, this paper uses the calculation of the Hamming distance as a measure of the similarity of the basic information vector. $D(SI/RI)$ is calculated as follows (6).

$$D(SI/RI) = \sum_{i=0}^{n} S_N \oplus r_N \tag{6}$$

The above education sharing scenario can effectively improve the system throughput and make the system run more smoothly.

3.2 Building an Educational Resource Sharing Architecture

The overall function of the educational resource sharing platform studied in this paper is divided into two parts: the Web end and the client end. The Web end includes the educational resource sharing platform, personal real name cyberspace and the background management system of the sharing platform. Clients include PC client, Android client and IOS client. Ordinary users and administrators can upload and share various educational resources on the sharing platform. Resources can only be viewed, downloaded and displayed in the foreground and client software after being reviewed and released by the administrator.

This paper mainly studies the unified management, standardized processing, distributed storage and real-time retrieval of uploaded resources under the support of Hadoop technology, so that users can use various resources more quickly and conveniently for learning and communication. The users of the educational resource sharing platform mainly include six categories: students, teachers, parents, super administrators, ordinary administrators and tourists who have not registered with the system. The continuous expansion of the scale of educational resources, the variety of types, and the different ways of expression make the sharing of educational resources become the bottleneck of the development of distance education and online education. In order to unify and standardize the information representation and storage among educational institutions, so as to retrieve the resources needed by users more efficiently and accurately, it is necessary to design and develop a resource sharing platform suitable for massive educational resource storage and retrieval. The platform is composed of three systems: resource sharing platform, real name cyberspace and client software. Users can freely jump between the three systems to carry out personalized learning, collaborative learning and communication. The designed educational resource sharing architecture is shown in Fig. 6 below.

It can be seen from Fig. 6 that the resource sharing platform is divided into two modules: front and back. The front desk provides access for ordinary users and tourists, and the back desk is the interface for administrators to manage the system. The front desk provides users with multi-functional basic education resource services, such as curriculum resource ranking, resource retrieval, resource upload and download, resource online demonstration, resource sharing and other functions. At the same time, the platform also adopts an effective integral incentive mechanism to encourage users to actively share all kinds of high-quality teaching resources and achieve the convergence of high-quality resources. The background provides a good interface for administrators to manage the whole system. Administrators can manage users, roles, resources, logs, exams, and credits by category.

Real name cyberspace mainly provides learning, social and management services, and provides effective learning and social environment for teachers, students and parents, such as online learning, lesson preparation and office, social interaction, etc. Users can not only work and study in their own learning space, but also enrich their after-school life on the social platform. The client software is an effective expansion of resource sharing platform and network real name space, providing support for online teaching and communication of teachers, enriching teaching forms and improving the traditional teaching mode. Teachers, students and parents can also conduct instant messaging, file exchange

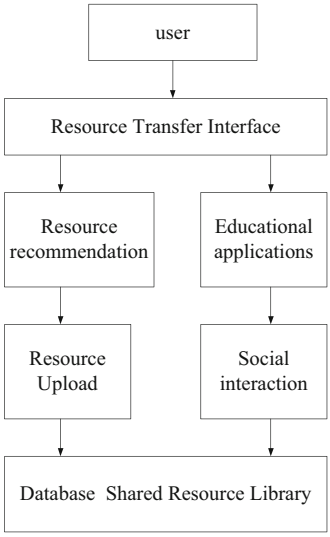

Fig. 6. Educational resource sharing architecture

and mutual learning through the client, which greatly promotes the communication and cooperation among users.

3.3 Design Innovation and Entrepreneurship Education Resource Function Module

The resource sharing platform is mainly responsible for the effective organization of basic education resources and user resources, the centralized collection and construction of basic education resource database, and the provision of educational resource sharing, resource evaluation, resource display, social interaction, online learning, mutual learning, online office and other functions for basic education authorities, teachers, students and parents. The cross platform instant messaging capability is provided through the client software to facilitate users to access the platform through multiple terminals at any time, anywhere, and provide the background management system to manage various resources and maintain the application system to ensure the stable and efficient operation of the entire platform. According to the platform architecture, the entire educational resource service platform includes three parts: the resource sharing platform Web end, personal real name cyberspace and client software. Its specific functions are as follows:

(1) Web front desk: including login, resource ranking, resource search, resource details view, resource upload, resource display, resource evaluation and resource download;
(2) Web end background: including portal management, user management, role management, space management, resource management, exam management, score management and log management;
(3) Personal real name cyberspace includes teacher space, student space, parent space and their common functions, providing users with online office, online learning, social interaction and other functions.

(4) The client software is an extension of the resource sharing platform and personal real name cyberspace functions. It not only includes the main functional interfaces provided by the first two parts, but also adds instant messaging, lesson preparation, homework and other functions, and provides support for online teaching, specifically including the PC side, Android side and IOS client. The top-level structure of the functional module is shown in Fig. 7 below.

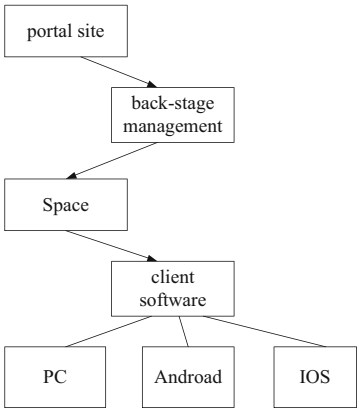

Fig. 7. Top structure of function module

It can be seen from Fig. 7 that the Web end is mainly divided into two modules: portal and background management system. The foreground function module is mainly the platform for ordinary users and tourists to carry out relevant operations, while the background management system provides interfaces for various administrators to monitor and manage the entire system. The super administrator is mainly responsible for the management of key functional modules, and grants various roles and permissions to corresponding ordinary administrators. It details the responsibilities of administrators, precisely controls the permissions of administrators at all levels, facilitates dynamic addition and expansion, and provides the most favorable guarantee for the good operation of the platform.

4 System Test

In order to verify the running performance of the designed university innovation and entrepreneurship education resource sharing system based on cloud service platform, this paper builds a test platform, runs the system designed in this paper, and conducts system testing, as follows.

4.1 Test Preparation

This education resource sharing system includes clusters and three types of servers. One is the database server, which installs Oracle10g database, followed by the Web server,

which deploys eight Tomcat6 servers, uses load balancing strategies to improve the performance of the entire platform, and finally is the application server, which contains multiple client software servers, including the client master server, resource server, HTTP search server, file transfer server, chat server, desktop sharing and whiteboard server.

The virtual environment built by the system consists of two physical machines and four virtual machines. A management machine manages other machines through VMware Vcenter. The specific hardware configuration of the environment required for application server, database server and client software is shown in Table 3 below.

Table 3. Test Environment

to configure	application server	database server
hardware configuration	CPU: Intel(R)Core(TM) 90@3.6 GHz i7–47 Memory: 16 GB (Samsung DDR3 1600 MHz) Hard disk: Seagate ST1000DM003-1H162 (1TB/7200 rpm)	CPU: Intel(R)Core(TM)i7–47 90@3.6 GHz Memory: 16 GB (Samsung DDR3 1600 MHz) Hard disk: Seagate ST1000DM003-1H162 (1TB/7200 rpm)
software configuration	Windows Server 2008	Windows Server 2008
network environment	100M LAN	100M LAN

Table 3 shows that the Java EE container on the test server side uses Tomcat 6.0.23. Tomcat server is an open source web server jointly developed by Apache, Sun and other companies. It meets the test requirements. After the above test environment is configured, subsequent system tests can be carried out.

4.2 Test Results and Discussion

Under the above configured testing platform, system testing can be carried out by adjusting the testing instructions, importing different numbers of resource files, comparing and verifying the system with reference [7] system and reference [8] system, and recording the query time of resource files for the three systems. The test results are shown in Table 4.

From Table 4, it can be seen that the file resource query time of the system in this article is the shortest among the three types, proving that the designed system has good operational performance, reliability, and certain application value. This is because the system in this article optimizes queries from both hardware and software aspects, thereby shortening query time.

Table 4. Test Results

Number of resource files	The query time of this system (s)	Query time of reference [7] system (s)	Query time of reference [8] system (s)
20	1.5	9.6	7.8
40	1.6	10.2	9.6
60	1.7	11.4	10.4
80	1.8	12.3	11.2
100	1.9	13.2	13.5
120	2.0	14.2	14.9
140	2.1	15.1	15.7

5 Conclusion

The integration and collaborative sharing of innovation and entrepreneurship education resources can not only effectively avoid the idleness of internal resources and the duplication of resources among universities, but also strengthen the complementary advantages of resources among universities. Only scientific and reasonable integration of innovation and entrepreneurship resources and improvement of the utilization rate of innovation and entrepreneurship education resources can comprehensively improve the quality of innovation and entrepreneurship education and cultivate high-quality innovation and entrepreneurship talents that adapt to economic and social development. Combined with the current innovation and entrepreneurship background, this paper uses the cloud service platform to build an effective university innovation and entrepreneurship education resource sharing system, and carries out system testing. The results show that the designed innovation and entrepreneurship education resource sharing system has good operation performance, reliability, and certain application value, and has made certain contributions to promoting the development of university innovation and entrepreneurship.

The university innovation and entrepreneurship education resource sharing system based on cloud service platforms has many advantages, but there are also some limitations. Firstly, establishing such a system requires corresponding technical support and infrastructure, including requirements for cloud computing, network, and data storage. This may impose certain restrictions on some universities with limited resources or poor technical conditions. Secondly, in the process of sharing educational resources, it is an important challenge to ensure that the personal information and sensitive data of teachers and students are fully protected, and to strengthen data security and privacy control. In addition, the use and management of the system require relevant technical training and support to ensure that users can fully utilize the system's functions.

The future development direction can further expand and improve the university innovation and entrepreneurship education resource sharing system based on cloud service platforms. Firstly, it is possible to enhance the intelligence and personalization of

the system, providing users with more accurate recommendations and customized teaching content through technologies such as data analysis and machine learning. Secondly, various innovation and entrepreneurship resources can be further integrated, including innovation and entrepreneurship projects, investors, and corporate partners, to build a more complete innovation and entrepreneurship ecosystem. In addition, it is possible to strengthen the connection with other universities, enterprises, and social resources, promoting deep integration of industry university research cooperation and innovation and entrepreneurship practices. Finally, through an open platform architecture, third-party developers can be encouraged to participate, enrich the system's functions and applications, and provide more diverse educational services and support.

Aknowledgement. The CPC Construction brand building project of "Locomotive Project in the new era" of Wuhan Railway Vocational College of Technology: On Strengthening and Improving the Work Path of CPC Construction Running ahead Construction of the Chinese Communist Youth League in Higher vocational colleges in the new era (Project number: 2022Z001).

Students ideological and political education special topic of Wuhan Railway Vocational College of Technology: An Empirical study on class culture construction in Higher Vocational Colleges in the new era (Project number: 2022SZ03).

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