A Design of Digital High Multiple Decimation Filter in Intermediate Frequency Domain

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Abstract. An important task of digital down conversion is to reduce the sampling rate. In order to carry out undistorted decimation, decimation filtering must be carried out before decimation to prevent spectrum aliasing. Based on the design idea of hierarchical cascade filter, an implementation method of 100 times decimator filter is given. The sampling factor and frequency response of each filter are analyzed in detail, and the theoretical analysis and practical logic implementation methods are given. The practical application results prove the correctness and feasibility of the design of high multiple decimator filter. This multi-stage decimation method not only enhances the stability of the system, but also greatly reduces calculation and saves resources.

Keywords: Decimator · Aliase · Filter

1 Introduction

Digital IF processing is one of the key technologies of software radio. It is an important component connecting the AD IF digital stream with the baseband data stream demodulated at the back end. The development of software radio puts forward higher and higher requirements for digital IF processing technology. Its performance index directly determines the ability of software radio signal processing. Taking a software radio radar receiver as an example, its parallel processing channel is up to 32 channels, with 55 MHz bandwidth as the step interval, and the wide band RF signal is scanned linearly. Among them, IF processing performance index of single channel is as follows:

(1) Working clock 120 MHz;
(2) AD input data bit width is 16 bits;
(3) AD sampling rate 120 M;
(4) Input data bandwidth 60 kHz;
(5) The decimator multiple is 100, and the final output rate is 1.2 M;
(6) Output data bit width 24 bits;
(7) Decimator of anti-aliasing inhibition is greater than 100 dB.

The decimator factor of the machine is as high as 100, and the anti-aliasing inhibition is more than 100 dB. Common filter types for decimator, such as CIC filter wave and half-band filter, cannot meet the requirements of anti-aliasing suppression. In the process of real - space design, the combination of CIC filter, half-band filter and polyphase filter

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must be integrated to gradually reduce the decimator rate and cascade to achieve aliasing suppression performance index [1, 2].

2 Design of Decimation Filter Bank

High multiple decimation processing is realized by the cascade combination of filters as shown in Fig. 1.

The filter bank is composed of four cascade filter groups, and the sampling rate of digital signal is reduced step by step.

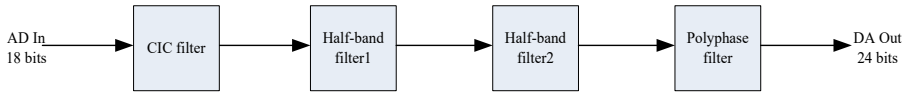

Fig. 1. High multiple decimator filter function diagram

CIC Filter of Stage 1. CIC filter structure is relatively simple, the implementation occupies less logical resources, but the frequency response transition band is large, the frequency band characteristic changes are relatively flat slow. The CIC filter can be used to achieve low-multiple logic decimator, and the signal sampling rate can be reduced in the initial step, and the timing margin of time-division multiplexing can be provided for other types of subsequent filters, so as to save logic resources.

In this design, CIC realizes 5 times decimator. To ensure decimation anti-aliasing suppression is not less than 100 dB, the frequency band amplitude response of the filter in the $[f_s/10, f_s/2]$ interval (f_s is the data sampling frequency) must be more than 100 dB relative to the main lobe peak.

Half-Band Filter of Stage 2/Stage 3. When the input signal sampling rate of digital IF equipment is reduced to 1/5, the sampling rate is changed to 24 MHz. Since the effective band width of the signal is 500 kHz, the order of FIR filter should be about 400 (24 MHz/60 kHz) if the subsequent FIR multiphase filter is directly adopted to achieve the decimator of signal bandwidth. High-order filter will take up a huge amount of multiplier resources, and the frequency response is very difficult to do sharp.

In this design, the two-stage half-band filter cascade is used to further reduce the data sampling rate by 1/4, so as to ensure that the low-order FIR multiphase filter can be adopted and the time-division multiplexing margin of the subsequent filter can be further guaranteed.

Polyphase Filter of Stage 4. After the CIC filter and the two-stage half-band filter, the signal sampling rate is reduced to 1/20 of the original AD input sampling rate, that is, 6 MHz. Because the ratio of data sampling rate to data bandwidth is relatively low, it is convenient to use low-order FIR filter to realize effective selection of data pass-band. In order to achieve the requirement of 100 times overall decimator rate, the multiphase filter structure is adopted in the 4th stage FIR filter, and the 60 kHz pass-band and 5 times decimator are realized simultaneously.

2.1 CIC Filter Design

The CIC filter achieves 5 times decimator. In order to ensure that the decimator anti-aliasing suppression is not less than 100 dB, the frequency band amplitude response of the filter should be in the range of [f_s/10, f_s/2] (f_s is the data sampling frequency) and the suppression of the zero frequency point must be greater than 100 dB.

The amplitude-frequency response function of the single-stage CIC filter is shown in formula (1) [3].

$$H(jw) = \left| \frac{\sin(\frac{wDM}{2})}{\sin(\frac{w}{2})} \right| \tag{1}$$

w represents the angular rate, the design parameter D is the differential delay, and M is the decimator factor.

The stop-band attenuation performance of single-stage CIC filter is poor. As can be seen in formula (1), when DM >> 1, the level of the first side lobe is $2DM/3\pi$, and the difference between the peak level and the main lobe is:

$$20\log(\frac{\frac{DM}{2DM}}{3\pi}) \tag{2}$$

In engineering applications, the multi-stage CIC cascade is generally adopted to achieve better stop-band suppression performance under the condition of high decimator rate. The design parameters of the multi-stage CIC filter in this design are shown in Table 1.

Table 1. CIC hogenauer filter parameters.

Differential delay D	6
Decimation factor M	5
Cascading order N	5

The amplitude response of the multi-stage CIC filter is shown in Fig. 2 (the horizontal axis in the figure has been normalized by f_s/2).

As can be seen from Fig. 2, the normalized frequency point is located at [0.2, 1] interval, the stop-band suppression is not less than 130 dB, which meets the anti-aliasing suppression requirement of 5 times decimator.

2.2 Half-Band Filter Design

The pass-band and stop-band of the half-band filter are symmetric, and the filter's coefficients are symmetric, and all the coefficients of even order terms are 0 except the center point. The actual half-band filter coefficient that needs to be stored is about 1/4 of the order, which can reduce the resources of the mass storage and multiplier and reduce the operation Quantity [4].

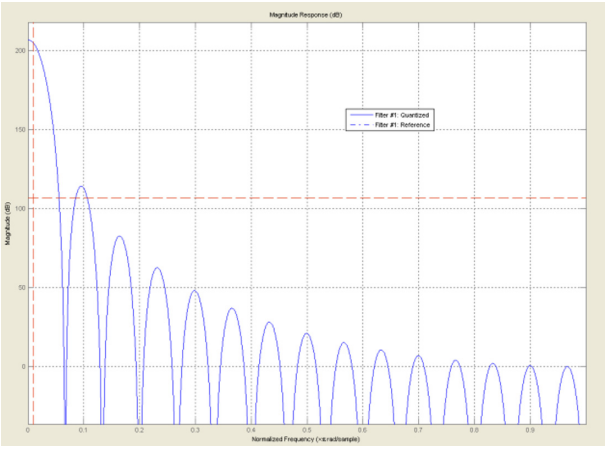

Fig. 2. Amplitude response for the CIC hogenauer filter

Table 2. Half-band filter parameters.

Order number	32
Coefficient of quantitative	16

The design parameters of the half-band filter in this design are shown in Table 2.

The amplitude response of the half-band filter is shown in Fig. 3 (the horizontal axis in the figure has been normalized with $f_s/2$, where f_s is the signal frequency input to the half-band filter).

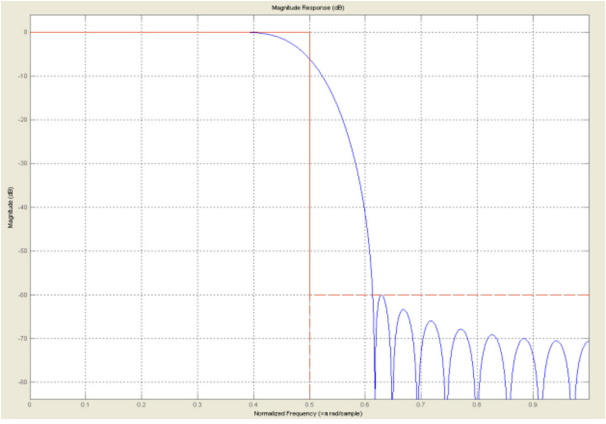

Fig. 3. Amplitude response for the half-band filter

As can be seen from Fig. 3, the stop-band suppression is at least 40 dB. Since the pre-stage CIC filter has suppressed the stop-band by nearly 100 dB, the superposition of the two also meets the requirement of aliasing suppression greater than 100 dB.

It should be noted that when the half-band filter is used for 2 times decimator, although there is no aliasing in the pass-band and stop-band, there is aliasing in the transition band. The pass-band and stop-band of the half-band filter are symmetrical. Frequency response characteristics after 2 times decimation are shown in Fig. 4. The transition band has obvious aliasing after 2 times decimator. Therefore, a higher order FIR filter must be used in the post-filter to improve the performance indicators such as pass-band, transition band and stop-band attenuation, so as to ensure that the transition band aliasing of the half-band filter is suppressed.

The second stage and the third stage half-band filter adopt the same coefficient, the total with the realization of 4 times decimator.

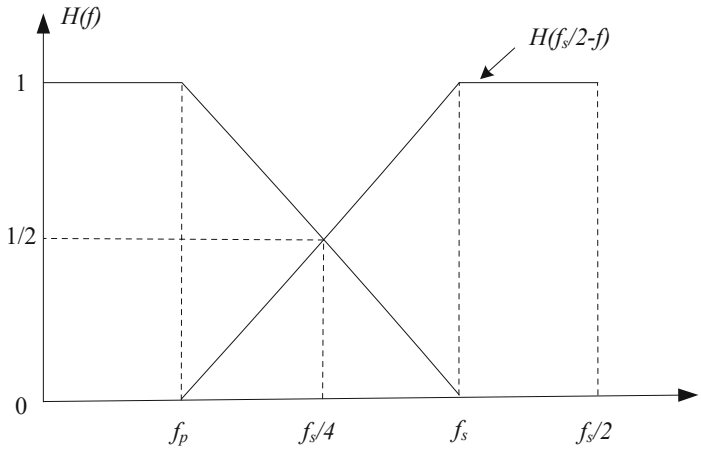

Fig. 4. The alias diagram of the halfband filter [5]

2.3 Polyphase Filter Design

Polyphase filter is a commonly used method in the process of digital down conversion decimator [6]. Compared with the ordinary FIR filter, the conversion relationship of signal sampling rate can be effectively used to remove the unnecessary operation in the process of data rate conversion, thus greatly improving the speed of operation.

Figure 5 shows the structure of FIR filter based on polyphase decomposition [7]. The filter is divided into three subbands, and each subband is extracted by M times. After decimator, it enters the subband filter for filtering. Since the decimator rate of each subband is reduced to 1/M, the subband filter can reduce the resource utilization by time division multiplexing.

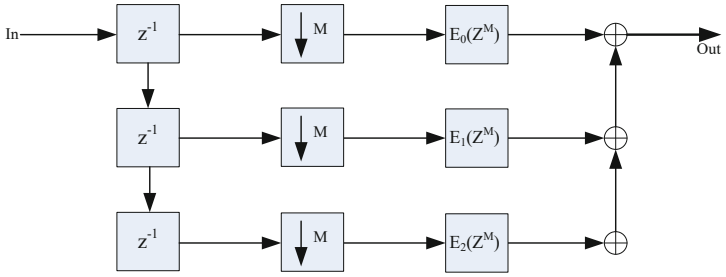

Fig. 5. The aliase diagram of the half-band filter

In the design of this paper, polyphase filter is used to achieve 5 times decimator and 60 kHz data bandwidth acquisition. After the pre-stage CIC filter and the two-stage half-band filter, the data sampling rate into the polyphase filter is 6 MHz (120 MHz/5/2/2). The design parameters of the polyphase filter are shown in Table 3.

Table 3. Polyphase decimator filter parameters.

Order number	128
Coefficient of quantitative	16

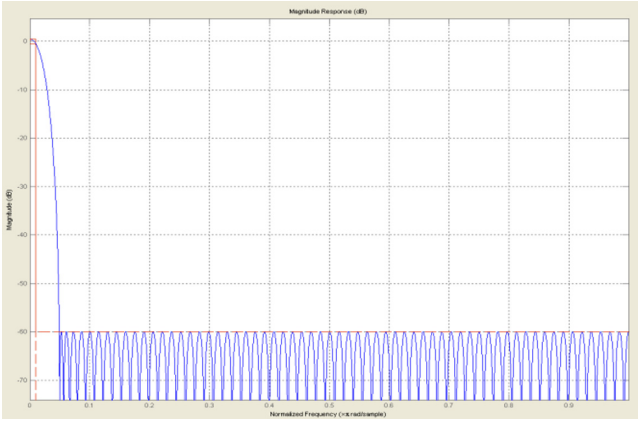

Fig. 6. The amplitude response of the polyphase decimator filter

The amplitude response of the polyphase filter is shown in Fig. 5 (where the horizontal axis has been normalized with fs/2, where fs is the signal frequency of the input multiphase filter). As can be seen from Fig. 6, the stop-band suppression is up to 60 dB, and the pass-band is 6 kHz. After 5 times of decimator, the anti-aliasing inhibition can

also reach 60 dB when it is located in the stop-band. Considering the stop-band suppression of the pre-stage CIC filter and the half-band filter, the superposition performance of the cascade filter bank meets the requirement of the whole body aliasing suppression greater than 100 dB.

3 Conclusion and Outlook

The four-step cascade of CIC, half-band and polyphase filter banks proposed in this paper has the following characteristics in design:

(1) The design method of decomposing the anti-aliasing index and the decimator factor index into multiple filters reduces the design performance of each filter and improves the design realizability;

(2) As the CIC filter and half-band filter are used to effectively reduce the front-end working frequency, the order of the key FIR filter at the back end is reduced as much as possible, and the usage of logical resources is reduced. The filter transition band can be designed to be smaller, which ensures the SNR of the output signal.

The verification results in a radar receiver show that the digital IF decimator achieved by FPGA can achieve a high multiple decimator of 100 times, the signal bandwidth can reach 500 kHz, and the anti-aliasing index of the whole machine can reach 110 dB, which meets the design requirements. The experimental results show that the design method of high multiple decimator index decomposition has the characteristics of high design performance, simple use and less resource consumption, and is worthy of popularization and application in design practice.

If the high multiple decimator filter is implemented by single-stage filter, it will lead to the filter has to adopt higher order and larger quantization error, which will affect the performance index and stability of the multiplefilter. In practical engineering, the suitable design method is to adopt multi-stage filter cascade, and gradually reduce the sampling rate through the lower order filter. In the future, more efficient multi-stage filter will be considered, so as to meet the requirements of the design index and reduce the use of resources.

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