Differential Cascode Voltage Switch Logic (DCVSL) Level Shifter with Logic Error Detection

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Abstract. Lowering the supply voltage proves highly effective in reducing dynamic power consumption within system-on-chip architectures, given its direct proportionality to VDD^2. A Level Shifter, also referred to as a Voltage Level Translator, is an electronic circuit specialized in converting signals between different voltage levels. The suggested LS design adopts the Cross-Coupled pFET Level Shifter approach. However, CPLS encounters contention issues during transitions due to its cross-coupled pFET structure. In this configuration, an nFET powered by VDDL needs to surpass a pFET powered by VDDH for positive feedback to trigger the operation. Consequently, as the voltage difference (VDDH–VDDL) increases, contention intensifies, potentially leading to operational failures. To mitigate this challenge, Differential Cascode Voltage Switch Logic (DCVSL) serves as an alternative to the single cross-coupled flip-flop. The circuit design, implemented using the Cadence Virtuoso tool, underwent comprehensive comparative analysis against existing level shifters. The utilization of DCVSL notably improved noise immunity, speed, and robustness while resulting in a 50% reduction in Static Power consumption.

Keywords: Level Shifter (LS) · System-on-chip (SoC) · Cross-Coupled pFET LS (CPLS) · DCVSL · Logic Error Detection

1 Introduction

In response to the growing demand for energy-efficient technologies, there is a critical imperative to design electronic systems that minimize power consumption, particularly in battery-powered devices and Internet of Things (IoT) applications. This imperative arises from the need to prolong battery life, reduce environmental impact, and optimize resource usage. As electronic devices become increasingly pervasive in various aspects of daily life, the drive toward energy efficiency becomes paramount for sustainable and cost-effective technological solutions.

X. Cheng (Ed): BROADNETS 2024, LNICST 601, pp. 74–82, 2025.
https://doi.org/10.1007/978-3-031-81168-5_8

The significance of ensuring the accuracy and reliability of Level Shifter (LS) systems cannot be overstated, especially in applications where errors in logic operations could have severe consequences. Critical domains such as aerospace, medical devices and automotive safety systems demand flawless performance to guarantee the safety and functionality of the overall system. By integrating advanced logic error detection mechanisms into LS systems, the reliability of these systems is significantly enhanced. This proactive approach to error detection not only safeguards against potential malfunctions but also reinforces the integrity of electronic systems operating in mission-critical environments.

Reducing the supply voltage stands as an immensely effective strategy for mitigating dynamic power consumption in system-on-chip designs [14, 15]. Dynamic power consumption, which is associated with transistor switching, decreases significantly as the VDD2 decreases. Operating circuits near the threshold voltage of transistors, known as near-threshold operation, offers particular advantages, potentially resulting in a nearly tenfold reduction in dynamic power consumption compared to standard operation at nominal voltage levels.

For a deeper exploration of the technical details, there exist two traditional forms of low-swing (LS) architectures—the cross-coupled pFET and the current mirror-based LS. These structures are recognized elements within integrated circuit design. Their specific characteristics and configurations are pivotal in optimizing power consumption, mainly for near-threshold operation. But these two conventional LS structures are having limitations which were further solved by various schemes refer to papers [5–13]. By employing these conventional LS structures, engineers can further enhance the efficiency of the system, ensuring that the reduction in supply voltage translates into a substantial reduction in dynamic power consumption for the overall system-on-chip.

With the proliferation of electronic devices across industries and households, the cumulative energy usage of these systems has become a significant contributor to overall energy consumption. By prioritizing energy-efficient design principles, we not only address immediate concerns such as battery life but also contribute to the long-term sustainability of our planet.

Moreover, the optimization of power consumption in electronic systems goes hand in hand with advancements in renewable energy technologies. As the world shifts towards renewable sources of energy such as solar and wind power, the importance of energy efficiency in electronic devices becomes even more pronounced. By minimizing power consumption, we can maximize the efficiency of renewable energy systems and further reduce reliance on fossil fuels, thereby accelerating the transition to a cleaner and more sustainable energy future.

2 Literature Survey

The [1] introduces an innovative level shifter design boasting a wide conversion range and emphasizing both speed and energy efficiency. It employs a unique architecture utilizing the multi-threshold CMOS technique, alongside a mixed-threshold current mirror circuit to address swing issues and auxiliary bias circuits to reduce power consumption during idle states.

[2] Presents an energy-efficient level shifter (LS) with a wide conversion range, featuring a logic error detection circuit (LEDC). Based on a current mirror-based design (CMLS), it addresses static current limitations by integrating a feedback pFET, unlike Wilson's CMLS (WCMLS) which struggles with low-to-high voltage conversion. The proposed LS utilize the LEDC to achieve full conversion from VDDL to VDDH. Post-layout simulation using a 7-nm finFET model demonstrates a propagation delay of 0.21 ns and energy consumption of 20.43 fJ at 0.4/1.2 V and 1 MHz, showcasing its effectiveness in reducing delay and energy usage under specific conditions.

[3] Presents a voltage level shifter, also referred to as a voltage level translator, tailored for analog and digital integrated circuits (ICs). This shifter effectively transforms voltage levels from the sub-threshold range to the super-threshold domain, all while minimizing propagation delay. Simulations conducted across various CMOS technologies, including 45 nm, 65 nm, 90 nm, and 180 nm, highlight significant enhancements over recent designs. Particularly in the context of 90 nm CMOS technology, the proposed shifter demonstrates a remarkable 69.12% reduction in propagation delay, while 45 nm technology shows a 67.07% improvement. Corner analysis consistently indicates superior performance compared to recent techniques, suggesting promising advancements in key performance metrics like propagation delay across diverse CMOS technologies.

The paper [4] delves into the critical concern of energy efficiency in modern System-on-a-Chip (SoC) designs. While reducing power supply voltage effectively minimizes power consumption, it can detrimentally affect speed performance. Time-sensitive sections operate at VDDH for optimal performance, while less critical areas function at VDDL to enhance power efficiency. In scenarios demanding low power, sub-threshold operation is considered for certain sections. Utilizing multiple-supply circuits requires the optimization of costs associated with voltage domain conversion, achieved through the implementation of level shifter (LS) circuits.

3 Design and Implementation

The objective encompasses several key components aimed at enhancing the performance and versatility of the Differential Cascoded Voltage-Switched Logic (DCVSL) Level Shifters.

Firstly, the focus is on designing and implementing a DCVSL Level Shifter that prioritizes energy efficiency. This involves careful consideration of voltage-switching mechanisms and circuit configurations to optimize power consumption, aligning with contemporary standards for energy-conscious design [1–4].

Secondly, an emphasis is placed on integrating advanced logic error detection mechanisms within the Level Shifter (LS) system [2]. This addition serves the crucial role of promptly identifying and rectifying errors, contributing to the overall accuracy and reliability of the system's output. By incorporating error detection at the logic level, the system becomes more robust and resilient, minimizing the impact of potential errors on its performance.

Furthermore, the designing of the LS system was done in a scalable manner [3]. This scalability aspect ensures that the Level Shifter can be seamlessly integrated with other systems or modules. This adaptability is vital for accommodating diverse applications and varying requirements, facilitating easy expansion and enhancing the overall flexibility of the system.

The basic elements were implemented on the cadence virtuoso tool using 90 nm technology and were verified by their transient response. Figure 1 below illustrates the schematic diagram of the Existing Project incorporates mixed-threshold current mirror, as well as auxiliary bias circuits. However, the convention problem arose due to the current mirrors.

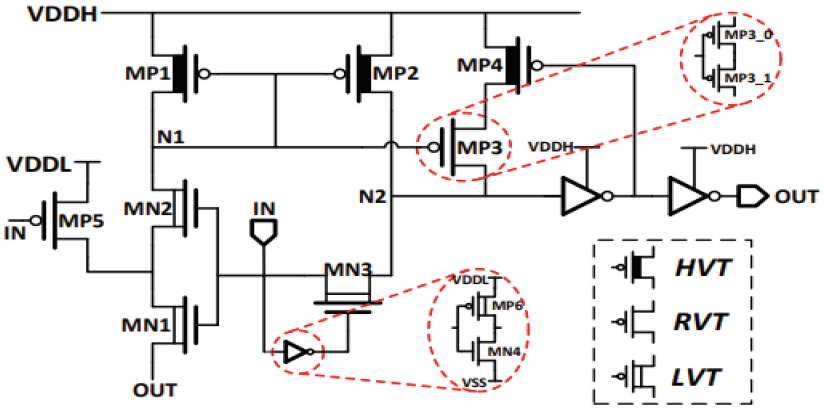

Fig. 1. Diagram of Existing project Level Shifter (LS)

4 Results and Discussions

4.1 Schematic Diagram of Proposed LS

Figure 2 is the implementation of a Schematic Diagram of the proposed Level Shifter in the cadence virtuoso tool using 90 nm technology.

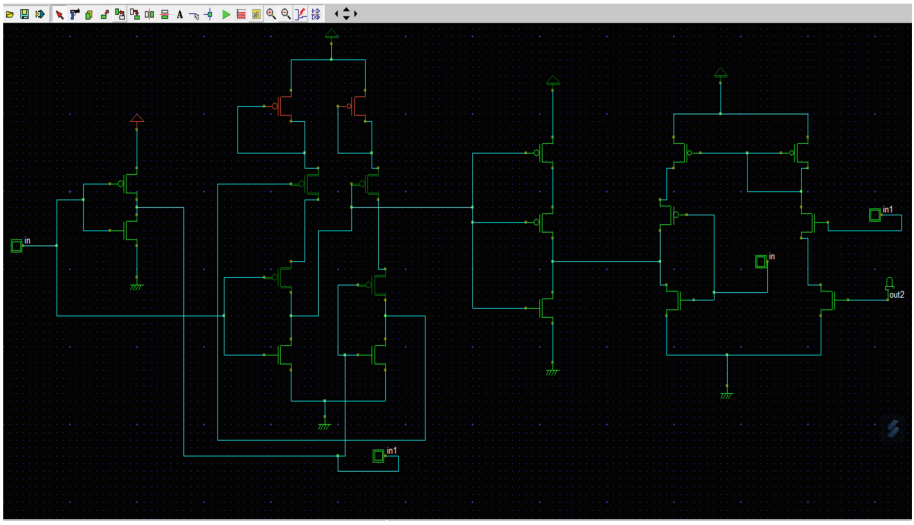

Fig. 2. Proposed project Level Shifter schematic diagram

4.2 Proposed Level Sifter Layout Implementation

Figure 3 is the implementation of proposed project layout in the cadence virtuoso tool using 90 nm technology.

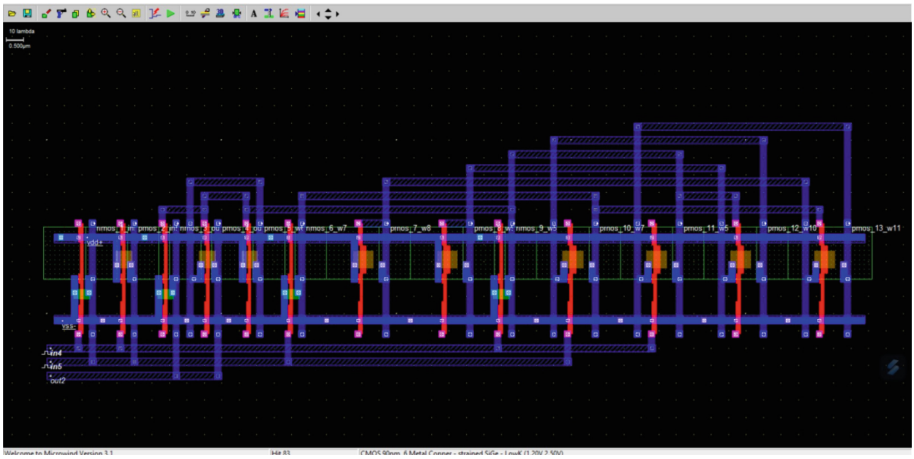

Fig. 3. Layout of proposed project Level Shifter

4.3 Various Combination of Input Diagrams

Figure 4 is the Proposed Level Shifter Schematic diagram implementation having Low Input.

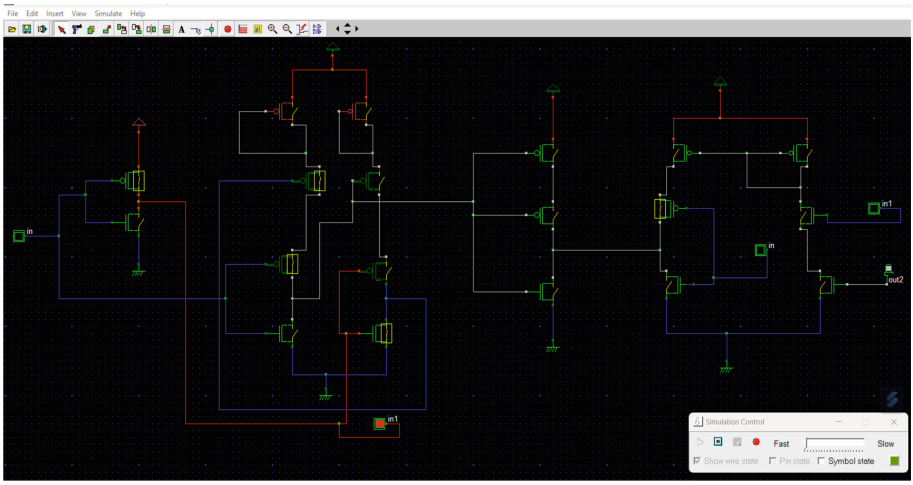

Fig. 4. The Low Input

Figure 5 is the Proposed Level Shifter Schematic diagram implementation having High Input.

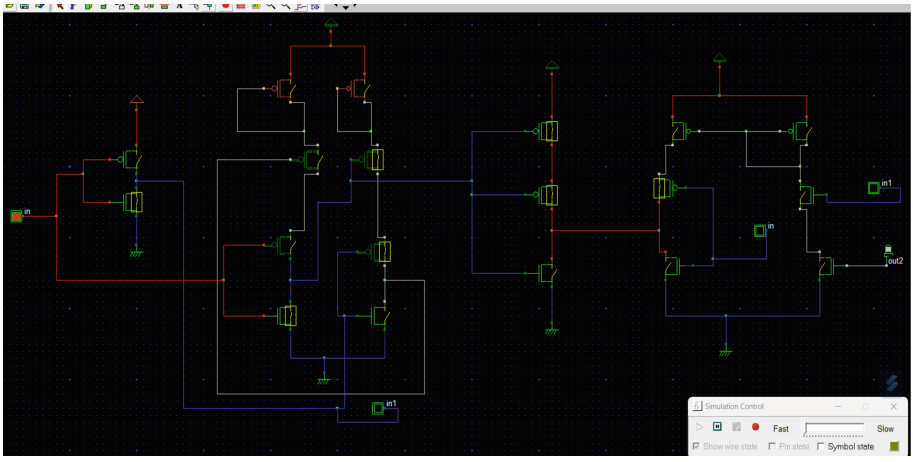

Fig. 5. The High Input

4.4 Transient Response

Figure 6 is the Transient response of the proposed project in the cadence virtuoso tool using 90 nm technology.

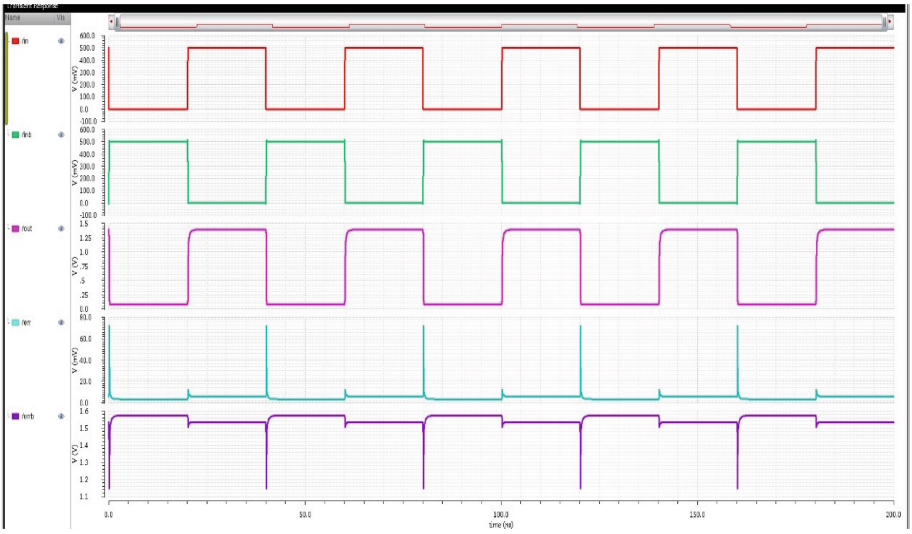

Fig. 6. Output Transient Waveform

4.5 Comparison of Parameters

Table 1 displays a comparative analysis of specific parameters between the existing project and the proposed one.

Table 1. Parameter Comparison

Parameters	Existing Project	Proposed Project
Technology used	90 nm	90 nm
Time/Duration of signal	0–200 ns	0–200 ns
VDDL	300 m V	375 m V
No. of Transistors used	14	19
Delay of o/p w.r.t i/p	17.86 ns	25 ns
Static Power	4.37 n W	2.15 n W
No. of stages used energy	26.59 f J	30 f J

The comparison between the existing and proposed projects, both utilizing a 90 nm technology, reveals nuanced differences. While the proposed project boasts a higher supply voltage (VDDL) at 375 mV compared to the existing project's 300 mV, it also incorporates a more intricate design with 19 transistors, surpassing the 14 transistors in the existing project. Despite exhibiting a longer processing time with a 25 ns delay in comparison to the existing project's 17.86 ns, the proposed project showcases notable improvements in static power consumption, recording a lower 2.15 nW compared to the

existing project's 4.37 nW. Furthermore, the proposed project achieves enhanced energy efficiency with 30 fJ per stage, compared to the existing project's 26.59 fJ. These trade-offs underscore the need for a comprehensive assessment considering specific project goals and constraints.

5 Conclusions

In conclusion, the reduction of supply voltage emerges as a highly effective strategy for mitigating dynamic power consumption in system-on-chip architectures. This is particularly significant given the direct proportionality between dynamic power consumption and VDD^2. The focus of this paper has been on the design and optimization of a Level Shifter (LS), specifically addressing the contention issue associated with the Cross-Coupled pFET LS (CPLS). The proposed solution leverages a Differential Cascode Voltage Switch Logic (DCVSL) as an alternative, effectively enhancing noise immunity, speed, and robustness. The implementation of this design, analyzed through the Cadence Virtuoso tool, demonstrated notable improvements, including a 50% reduction in Static Power, marking a substantial advancement in the efficiency of level shifting within SoC architectures.

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