An Energy-Efficient 8-Tap FIR Filter Design in 22nm DTMOS Technology

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Abstract. The field of Integrated Circuit (IC) technology has seen amazing developments over the last few decades, resulting in a constant reduction in the size of circuit features. This continual tendency has demanded the introduction of IC-741-based circuits into each Integrated IC, reflecting the electrical design's continuous progress. During the complex process of digital circuit design, special attention is paid to new circuits that use Dynamic Threshold Metal-Oxide Semiconductor (DTMOS) technology. Because of its unique capacity to produce higher efficiency while consuming less power, DTMOS-based circuits have gained major importance. These circuits mimic the behaviour of CMOS transistors while using only two transistors to maintain good performance and resilience. The proposed study focuses on the design, modelling, and implementation of a Finite Impulse-Response (FIR) filter using DTMOS logic in conjunction with basic building blocks. Within the purpose of this inquiry, an 8-Tap FIR structure based on DTMOS chambers is constructed. The study's findings highlight the benefits of incorporating DTMOS logic into an eight-tap FIR architecture, providing significant increases in both power efficiency and overall performance. This study adds to the ongoing investigation of cutting-edge technologies that improve the capabilities of digital circuits.

Keyword: 8-Tap FIR Configuration · 22 nm Technology · DTMOS Methodology in Circuits

1 Introduction

The Finite Impulse-Response (FIR) units are the fundamental building blocks in Digital Signal Processing (DSP) design. These units are essential in a wide range of sectors and digital systems [1] from automotive to mobile wireless headphones, phones, laptops, and speech synthesis. Two critical considerations highlight the need to develop modern electrical systems: technology progress and consumer needs.

Cyber Physical Systems typically involve a combination of hardware and software components that interact with each other and with the physical environment. Examples include smart grids, autonomous vehicles, medical monitoring systems, and industrial

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automation systems. The goal of CPS is to improve efficiency, reliability, and safety by tightly integrating computational and physical processes.

Surprisingly, a gap in the literature on Dynamic Threshold Metal-oxide Semiconductor (DTMOS) technology is revealed, suggesting an undiscovered region within the domain of DSP. The lack of earlier research or projects aimed at applying DTMOS technology in DSP applications presents an opportunity for ground-breaking inquiry at the confluence of these two domains. The fundamental blocks can now be efficiently manufactured with just two transistors. These benefits drive the most recent study to DTMOS into the design of FIR filters, resulting in a strategic fusion of new aspects.

This project focuses on creating an 8-Tap FIR filter using DTMOS logic. This filter is important for cyber-physical systems (CPS), which blend computer algorithms with physical processes like smart grids and autonomous vehicles. The FIR filter helps CPS by processing signals, reducing noise, and enhancing data. By using DTMOS logic, the filter becomes more efficient and consumes less power, crucial for CPS applications, especially those with limited resources or requiring long battery life. The study leverages the TSPICE software of PTM 22nm CMOS [2] Technology to create and develop these blocks, including the FIR filters, emphasising a thorough and technologically advanced methodology. To evaluate the performance of the developed system, output parameters such as Delay, Area (MOSFETS), Power, and Power Delay Product (PDP) are carefully calculated.

The investigation then concludes with a thorough comparison of the collected data with those from the previous system, providing a thorough grasp of the gains made. The study's subsequent sections dig into a full literature review, the methodology used, the presentation of data, that will synthesis the findings and implications of this groundbreaking research.

2 Literature Review

In the year 2021, the author embarked on the creation of a model with the primary goal of building and analysing an instrumentation amplifier, with a particular emphasis on the incorporation of 45nm technology [3]. This deliberate selection of "45nm technology" represents not only a jump into sophisticated semiconductor manufacturing methods, but also a commitment to investigating cutting-edge methodologies in electrical design. However, like with any innovation, this approach had several limitations, including high power consumption and space utilisation issues.

In 2018, the author spent a significant amount of time developing a model centred on the design and actual implementation of a 16-tap Finite Impulse-Response (FIR) filter. The goal of this study went beyond theoretical design, with the goal of demonstrating the filter's actual utility in Digital Signal Processing (DSP) applications. Despite the admirable emphasis on real-world applications, the model was limited by its inability to be applied in real-time circumstances. High hardware complexity, low tap resolution, and significant power consumption were identified as concerns, highlighting the difficulties in turning theoretical prowess into practical usefulness.

In 2017, the author's focus switched to the construction of a low-power one-bit full-adder circuit with an out-crossed architecture. This particular design was intended to

contribute to energy-efficient arithmetic applications, which aligned with the broader issue of power efficiency in electronic circuits. Despite these good intentions, the model fell short of expectations in terms of speed, noise sensitivity, and interoperability with standard libraries.

In 2014, the author focused his efforts on constructing a model centred on the design of a low-power FIR filter—a critical component in digital signal processing. To attain the requisite low-power features, this model adopted a different approach, employing 6T complete adders. However, the practical implementation of this paradigm resulted in lower speed performance, degraded resolution, and operating range constraints, emphasising the delicate balance between energy efficiency and total system performance.

3 Methodology

3.1 DTMOS Logic

Figure 1 displays the fundamental circuit diagram of DTMOS (Dynamic Threshold-voltage MOS), an approach used in the design of the 8-tap FIR filter. Within Gate Diffusion Input (GDI) technology [4], this technique is used to dynamically regulate the threshold voltage of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET). The use of DTMOS introduces a means for dynamically altering this threshold voltage during operation. This feature improves flexibility in power management and performance optimisation within integrated circuits. DTMOS's dynamic adjustment capabilities are critical in obtaining higher performance metrics and reducing leakage current in specific conditions.

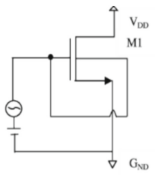

Fig. 1. General DTMOS circuit diagram

3.2 Proposed Full Adder

Figure 2 depicts a 10T (Transistor) GDI Logic & DTMOS-based adder [5, 6] demonstrating its power-efficient and high-performance characteristics. To improve noise tolerance, the 10T GDI Logic [7] employs ten transistors. Simultaneously, the adder utilises DTMOS transistors for body biasing, opening up the possibility of significant power savings [8] and performance increases in adder circuits, as referenced in sources.

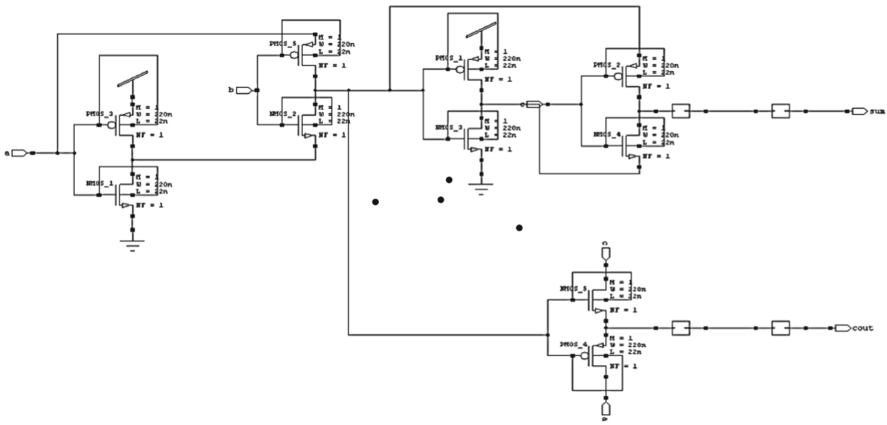

Fig. 2. Circuit diagram of proposed full Adder

3.3 Proposed D-Latch

The use of a D-Latch is noted in Fig. 3 below due to its importance in retaining the component's state. The design concept for an 8-tap FIR Filter comprises four bits, reflecting the filter's inherent ability to produce a linear phase, resulting in only four coefficients. It's worth noting that D-Flip-Flops [9] are used to add a delay in the value, establishing an 8-bit register for each component and serving as a memory retention mechanism.

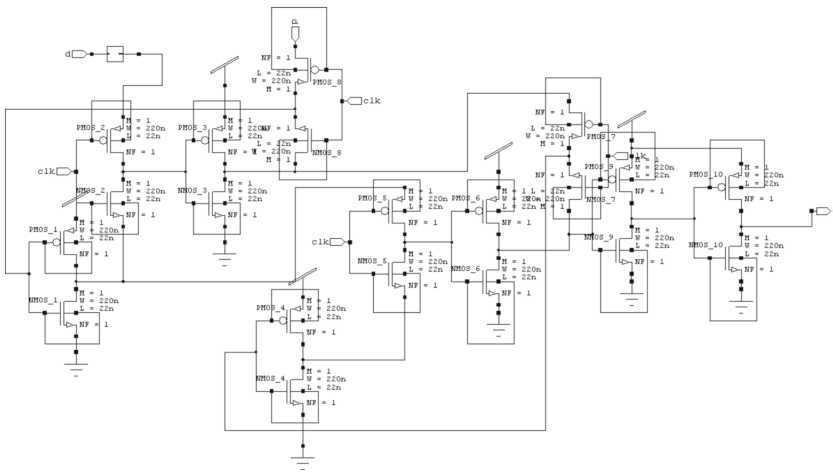

Fig. 3. Circuit diagram of Proposed D-Latch unit

3.4 Proposed 4-bit Array Multiplier

Figure 4 depicts the addition of a 4-bit array multiplier to the current architecture's 2-bit [10, 11]. By providing a one-to-one mapping relationship between array multiplication and user-defined multiplication, the design simplifies implementation. As mentioned in source the usage of an array multiplier is inspired by its inherent simplicity and superior performance [12].

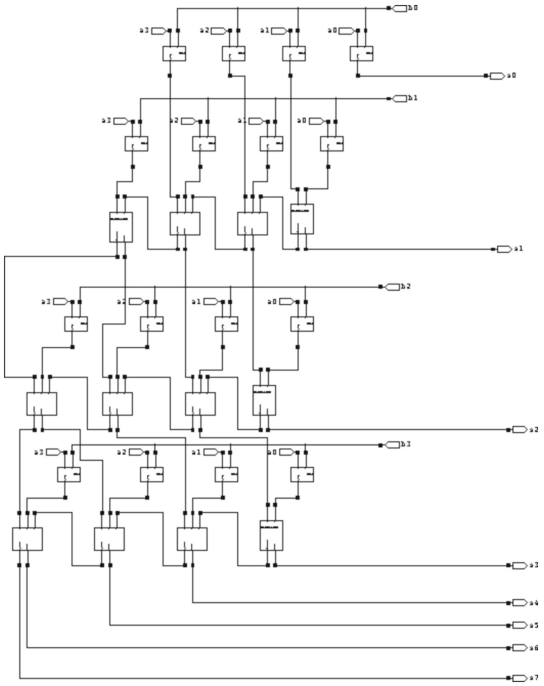

Fig. 4. Block diagram of Proposed 4-bit Array Multiplier

3.5 Proposed 8-Tap FIR Filter Design

Figure 5 depicts a Direct Form FIR Filter highlighting each tap's integration [13] of the proposed D-Latch unit, multiplier unit, and complete adder unit. The design of the FIR filter allows for a 4-bit input and output. The multiplier unit, in particular, is designed with two 4-bit inputs and two 8-bit outputs. The whole project consists of eight sequential taps [13], with each proposed D-Latch, multiplier, and full-adder unit contributing to the cascading arrangement feeding into the following taps.

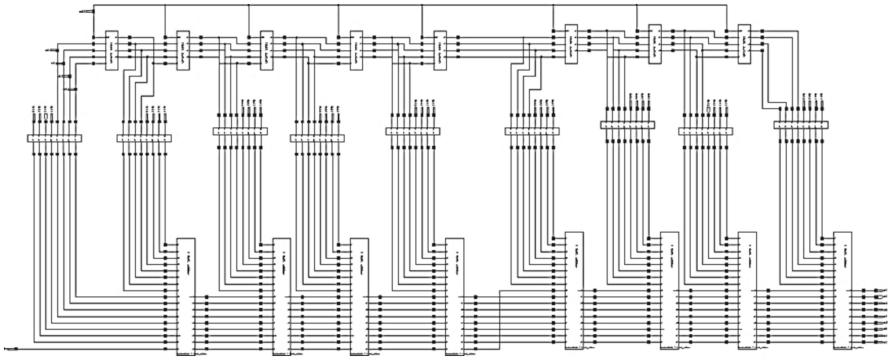

Fig. 5. 8-Tap FIR Filter implementation

4 Simulation Results

4.1 For Full Adder

The output waveforms for the proposed full adder describes in Fig. 6 which depicts a Direct Form FIR Filter highlighting each tap's integration of the proposed D-Latch unit, multiplier unit, and complete adder unit. The multiplier unit, in particular, is designed with two 4-bit inputs and two 8-bit outputs. The whole project consists of eight sequential taps, with each proposed D-Latch, multiplier, and full-adder unit contributing to the cascading arrangement feeding into the following taps.

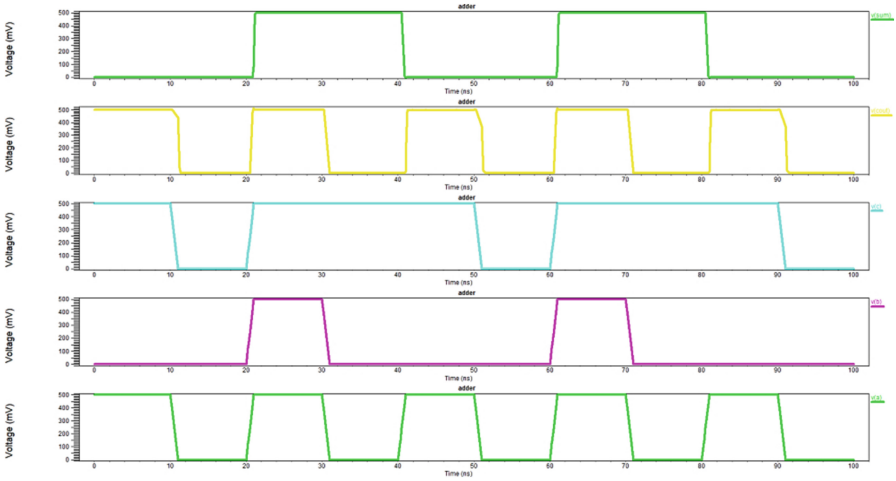

Fig. 6. Output Waveforms for the proposed full adder

4.2 For Proposed 4-bit D-Latch Unit

When a predetermined input is applied to a D latch, the output waveform reflects the applied input. "During the application of a clock signal, this waveform remains constant for a set period, represented as 't.' the repeated recurrence of this operation assures that the output waveform remains synchronized with the input waveform as long as the clock signal remains steady as combined all the four single delay units to produce four bit delay unit for single clock pulse.

Nonetheless, any change in the clock signal causes a detectable discontinuity in the output waveform, suggesting a substantial shift or change in the latch's behavior which is prescribed in the above Fig. 7 as shown below.

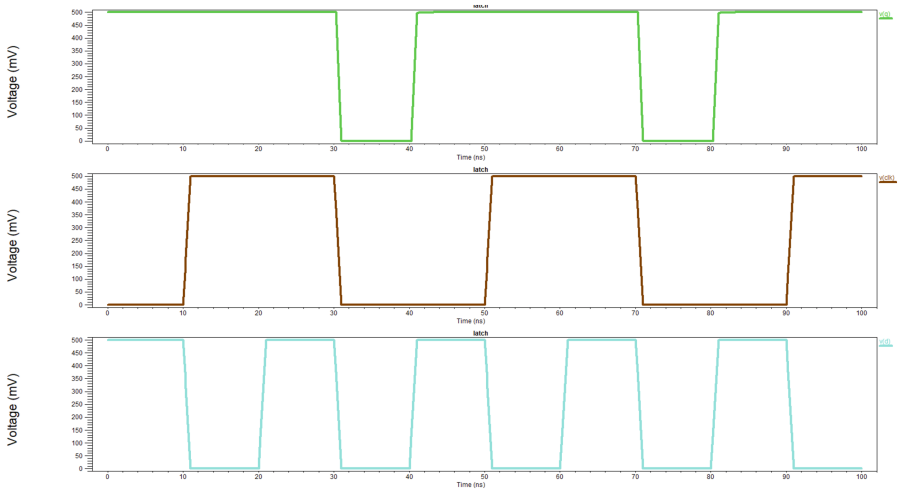

Fig. 7. Output Waveforms for proposed Delay Unit.

4.3 For 4-bit Array Multiplier

Figure 8 depicts the output waveforms that reflect the significant improvements obtained in the 4-bit Array Multiplier, with a particular emphasis on the astonishing reductions in both latency and power usage. The complexities of the waveforms not only show the efficiency improvements in the multiplier's response time, but also a significant reduction in overall energy consumption.

Figure 8 is a compelling demonstration of the purposeful efforts made to reduce delay, resulting in a more speedy and responsive 4-bit Array Multiplier. Simultaneously, the graph reveals a significant reduction in power consumption, emphasizing the careful design considerations targeted at improving energy efficiency.

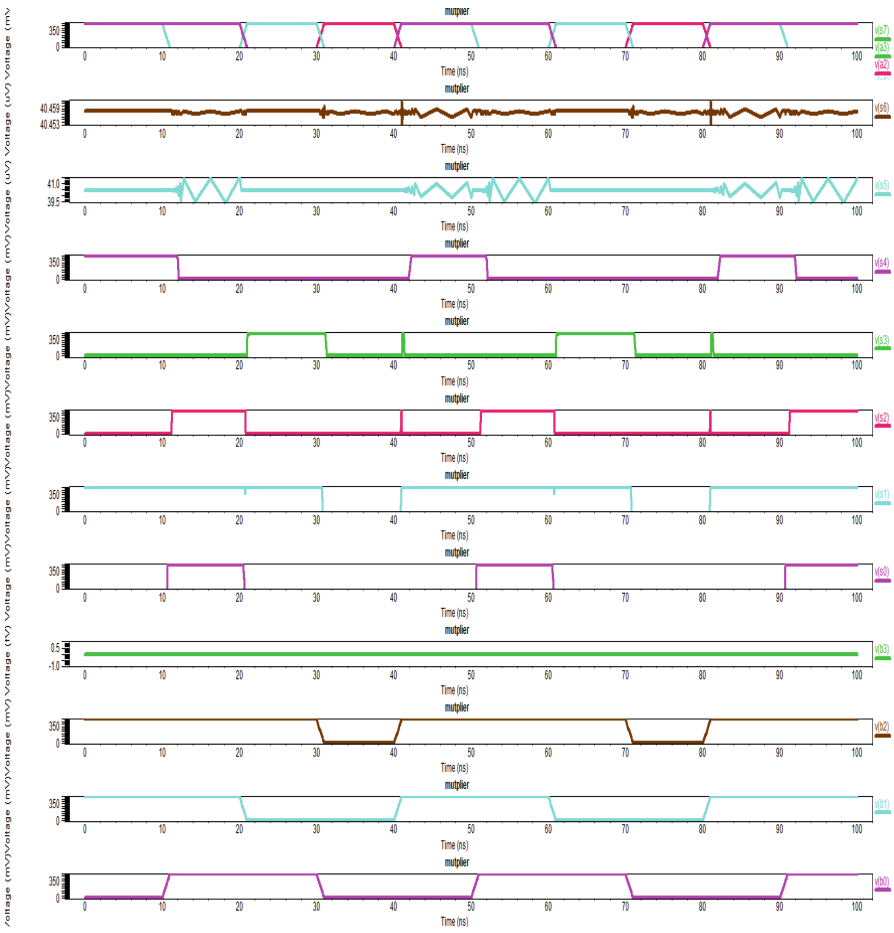

Fig. 8. Output Waveforms for 4-bit Array Multiplier

4.4 Proposed 8-Tap FIR Filter

The output waveforms shown in Fig. 9 match to the suggested 8-Tap Finite Impulse Response (FIR) Filter [13]. A major feature is the consistency found in the filter's region, which influences its effectiveness significantly [14]. The uniform characteristic within the filter's area, in particular, is intentionally engineered to achieve a dual goal: maximizing the filter's functionality while simultaneously decreasing power consumption. The constancy in the filter's area is a deliberate design choice intended to ensure signal processing stability and efficiency. By keeping this constant, the filter exhibits consistent and predictable behavior, which contributes to its overall efficiency in managing incoming signals [11]. Furthermore, the emphasis on this design component goes beyond conventional practicality; it is tightly tied to power consumption reduction.

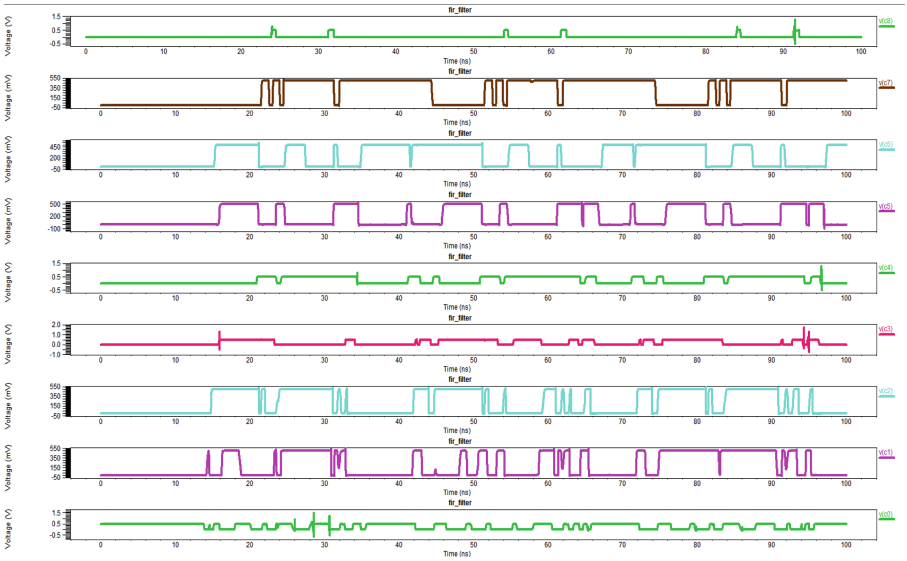

Fig. 9. Output Waveforms for proposed 8-Tap FIR Filter

5 Performance Comparisons

5.1 For Proposed Adder

From the Table 1, given below shows the performance comparison for the proposed full adder. The performance is greatly increased in the proposed adder using 22 nm DTMOS technology when compared with the 45 nm technology that uses the GDI Logic. Mainly, the area is not certainly increased and the average delay and the power consumption is greatly reduced.

Table 1. Comparison table for proposed adder

Full adder	Area (MOSFETS)	Delay	Average Power consumed	PDP
Existing adder (45nm)	18	10.541 ns	1.8225 μw	19.2109 fws
At (32nm)	18	10.545 ns	1.0070 μw	10.6182 fws
Proposed adder (22nm)	18	0.708 ns	0.8876 μw	0.6285 fws

5.2 For 4-bit Array Multiplier

The given below Table 2, a 2-bit array multiplier is extended to the 4-bit which gives the two 4-bit output. There is no change in the area usage when compared with the previous

research while the average power consumption is greatly reduced which results in the high performance of the multiplier.

Table 2. Comparison Table for 4-bit Array Multiplier

	Area (MOSFETS)	Average power consumed
Existing multiplier (45 nm)	296	427.05 μw
At (32 nm)	296	12.94 μw
Proposed Multiplier (22 nm)	296	7.45 μw

Table 3. Comparison table for proposed 8-Tap FIR Filter

	Area (MOSFETS)	Delay	Power	PDP
Existing (45 nm)	4520	9.18 ns	4119.5 μw	37.82 pws
At (32 nm)	4520	9.22 ns	318.15 μw	2.93 pws
Proposed FIR Filter (22 nm)	4520	2.51 ns	293.40 μw	0.73 pws

5.3 For Proposed 8-Tap FIR Filter

The total MOSFETS used in the proposed design are 4520. The average power consumption shows that a significant 72.6% reduction in power consumption when compared to previous research, while maintaining the same Area of 4520 MOSFETS. The delay is greatly reduced to 80% from the previous research. So, in this research we have proved that the energy is greatly reduced at 22nm DTMOS technique when compared with 45 nm GDI Technology which is prescribed in the below given Table 3.

Tables 1, 2, and 3 proves that the 8-Tap FIR Filter suggested here produces superior results in terms of MOSFET Area and power consumption.

6 Conclusion

This inquiry focuses on the implementation of an 8-Tap Finite Impulse Response (FIR) Filter using DTMOS logic-based circuits and DTMOS sensing techniques. The study reports a significant achievement: a 72.6% reduction in power consumption compared to earlier studies, while maintaining consistent hardware utilisation with 4520 MOSFETS. This work, which is based on a complete review of contemporary literature, emphasises DTMOS Technology's practical feasibility. Key variables such as MOSFET area, power consumption, latency, and Power-Delay Product (PDP) were thoroughly investigated. We successfully reduced power consumption and power delay product without spatial augmentation using simulation on CMOS 22nm technology. This project demonstrates not just the effectiveness of DTMOS technique in FIR Filter design, but also its critical role in advancing power efficiency and latency optimisation in semiconductor circuitry.

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