Performance Comparison of 4T SRAM Cell Using Different Techniques at 32nm and 22nm Nodes for Portable Electronic Devices

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Abstract. SRAM (Static Random Access Memory) has become an indispensable component in various Very Large-Scale Integration (VLSI) chips due to its high storage density and fast access times. This has significantly contributed to the global VLSI industry. The research community has also shown a growing interest in SRAM, particularly in low-power and low-voltage memory systems. The design of SRAM has evolved, with advancements in technology and manufacturing processes. One such design is the 4T SRAM, which utilizes CMOS, Schmitt Trigger, and Adiabatic technology. This design has been implemented at 22nm and 32nm nodes, showcasing the continuous improvement in semiconductor technology. The simulation of the 4T SRAM design was conducted using the Tanner EDA Software, a widely used tool in the industry. The simulation results have shown improvements in both power consumption and delay, which are critical factors in the performance of memory systems. Overall, SRAM has played a vital role in advancing VLSI technology, enabling the development of more efficient and powerful electronic devices. The continuous research and development in SRAM design and technology will further enhance its capabilities and contribute to the future growth of the semiconductor industry.

Keywords: Schmitt trigger · Adiabatic SRAM · Standard CMOS 22nm and 32nm nodes · PDP

1 Introduction

SRAM memory cell. SRAM cells frequently use minimum-size transistors to optimize packing density. Scaling has been used to lower the size of SRAM cells during the previous few decades, posing issues in power dissipation and propagation latency during read and write operations [1]. Dynamic power dissipation, which occurs during typical read-and-write activities, is critical in determining portable device battery life. Furthermore, stability is a primary problem for SRAM cell design, as it influences memory operation. This paper's examination focuses on the design and stability of a 4T SRAM cell across several CMOS technologies. The study employs PTM model cards for accurate performance characterization, taking into account the cell's many modes. SRAM's total power

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dissipation includes both dynamic and static power dissipation, with dynamic power consumed during normal operation and standby power consumed when idle [2]. Because it does not require periodic refreshing, the 4T SRAM cell, with its cross-coupled inverters and access transistors, outperforms DRAM in terms of speed and resilience. SRAM is preferred over Dynamic RAM (DRAM) because of its higher speed and durability.

The 4T SRAM cell, which uses CMOS technology and a Schmitt trigger, addresses memory issues in CPS at the 22nm and 32nm nodes. Its sophistication improves the stability and reliability required for real-world applications. Adiabatic technology reduces energy loss during charging and discharging cycles, meeting CPS's energy efficiency requirements [3]. This evolution ensures effective memory solutions for CPS, where computational and physical elements converge, requiring consistent operation under changing situations. 4T SRAM cells use modern semiconductor processes to maximize performance, reliability, and energy efficiency, allowing for the seamless integration of computational and physical components in the dynamic landscape of cyber-physical systems.

The Tanner EDA tool is used for the design and analysis of this advanced 4T SRAM cell, providing a robust environment for exploring and simulating the device's performance characteristics. This combination of CMOS, Schmitt trigger, adiabatic technology, and Tanner EDA demonstrates a comprehensive and novel approach to memory cell design that caters to the complexities of current semiconductor applications in the nanoscale era.

2 Literature Review

In the year 2021, Asheesh Sachdeva and V. K. Tomar investigate. "Design of Low Power Half Select Free 10-T Static Random-Access Memory cell" [4]. The part will most likely analyze existing SRAM cell designs, emphasizing the constraints of traditional architectures. Prior attempts to overcome these issues, such as assist circuits and dual-port SRAMs, are likely to be discussed by the authors, as are significant research gaps. The adoption of a 10-T SRAM cell indicates a deviation from the typically utilized 6T designs, which could be motivated by specific advantages in minimizing read and write problems, which summarizes significant insights, emerging trends, and research objectives gathered from the existing body of work in SRAM cell design, most likely sets the stage for the suggested design.

In 2020, D. Mittal and V. K. Tomar surveyed the literature on SRAM cell topologies at the 90nm technology node [5]. The project is likely to investigate existing studies on 6T, 7T, 8T, and 9T SRAM cell designs, with a focus on performance evaluations. The writers may have investigated the trade-offs and benefits of each topology, taking into account characteristics like as speed, stability, and power usage. This survey might have explored the unique issues provided by the 90nm technology node, as well as how various SRAM architectures manage these challenges. The paper's conclusions are likely based on a thorough grasp of the state-of-the-art SRAM cell design, providing vital insights for future developments in semiconductor memory technology.

In 2019, "Single Bit 7T Sub-threshold SRAM Cell for Ultra Low Power Applications". Hare Krishna Kumar and V. K. Tomar most likely did a thorough review of the

literature on sub-threshold SRAM cells [6]. The survey most likely looked into existing research on sub-threshold SRAM architectures, with a focus on their use in ultra-low-power circumstances. The authors may have looked into several SRAM cell layouts and their trade-offs in terms of power efficiency and stability It aids in the advancement of ultra-low-power applications. This research should provide useful insights into sub-threshold SRAM design and its possible uses in energy-efficient computing.

In 2012 "Robust SRAM Designs and Analysis" by Singh, Jawar, Saraju P. Mohanty, and Dhiraj K. Pradhan [7]. The authors will most likely investigate various procedures and techniques used in SRAM design to improve resilience, taking into account issues such as reliability and stability. The book will most likely dig into the difficulties involved with classic SRAM designs as well as the changing landscape of semiconductor technologies. It may highlight improvements in circuit-level innovations and architectural approaches to addressing SRAM cell reliability challenges. The literature review most likely sets the setting for the book's focus on robust SRAM design, providing insights into cutting-edge research and probable future directions in the field of semiconductor memory.

3 Methodology

3.1 Existing System

4T SRAM using CMOS:

Figure 1 displays the fundamental circuit diagram of the 4T SRAM (Static Random Access Memory) cell, which has a four-transistor structure and serves as a key building element in memory circuits [8]. The cell, which consists of two cross-coupled inverters and access transistors, stores binary information in a stable state.

Access transistors govern the flow of information into the cell during a write operation, making it easier to modify stored data. Notably, unlike dynamic memory systems, the 4T SRAM cell does not require periodic refreshing. Its operational speed and robustness make it a popular choice in a variety of electronic systems where quick and dependable access to stored information is critical. The read data is interpreted as '1' if the bit line differential voltage is high, signifying a logic high state; if not, it is interpreted as '0'. The word and bit lines are activated to access the cell during a write operation. The word line determines whether to write a '0' or a '1' into the cell once the new data is driven onto the bit lines. The. The read and write operations are controlled by the access transistors, which enable or disable access to the cross-coupled inverters.

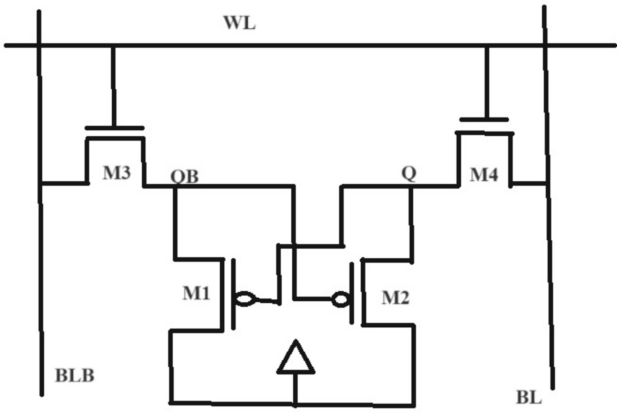

Fig. 1. 4T CMOS SRAM Cell.

3.2 Proposed System

4T SRAM using SCHMITT TRIGGER: The Schmitt trigger technology enables a more robust reaction to input signal changes during read and write operations [9]. It generates positive feedback using both PMOS and NMOS transistors, ensuring consistent high and low states. This design incorporates hysteresis, which means that it has higher and lower voltage thresholds for switching between states, which reduces susceptibility to small input fluctuations. In digital circuits, CMOS Schmitt triggers are extensively employed for noise immunity and signal conditioning (Figs. 2 and 3).

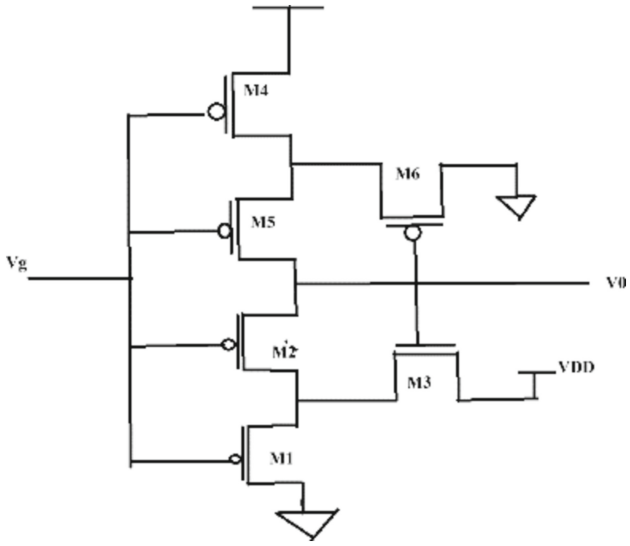

Fig. 2. Schmitt Trigger SRAM cell

4T SRAM using ADIABATIC Technique: Adiabatic approaches are focused on reducing energy loss during the charging and discharging stages, to increase power efficiency. The incorporation of adiabatic technology transforms the typical 4T SRAM cell structure, which consists of two cross-coupled inverters and access transistors [10].

$$E_{Dias} = \xi\, P\Delta T \tag{1}$$

$$= \xi\, I^2 RP\Delta T \tag{2}$$

$$= \xi (C_{Vdd/}\Delta T)^2 R_p \Delta T \tag{3}$$

The fundamental operation employs PMOS transistors for logic high ('1') and NMOS transistors for logic low ('0'). The transistors are placed in complementary pairs, and the voltage levels on the input signals regulate their behavior.

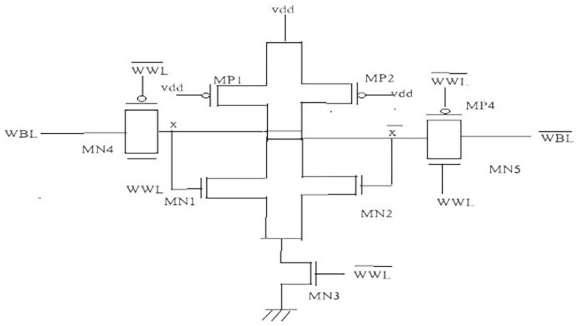

Fig. 3. Adiabatic SRAM cell

4 Simulation Results

Using the 32nm and 22nm CMOS technology and the Schmitt trigger adiabatic technique in the Tanner EDA tool, all of the results are simulated.

4.1 4T SRAM Using CMOS Technology at 32nm and 22nm

Figure 4 displays the schematic diagrams that have been drawn using basic SRAM Cell using CMOS.

The 4T SRAM cell in 32nm technology exhibits unique waveforms during read and write operations [11]. The read operation waveform responds quickly as the read signal triggers access transistors, allowing for quick and efficient data retrieval. Meanwhile, the write operation demonstrates a controlled and somewhat fast process, reflecting the characteristics of the larger technology node.

The 4T SRAM cell introduces improved waveforms that signify considerable advances in both read and write operations as it transitions to the advanced 22nm technology node [12]. Because of the smaller transistor size in the smaller technology node, the read waveform achieves even faster access times and higher power efficiency. The write operation is also improved, with higher speeds and lower power consumption, underlining the efficiency benefits realized in the smaller 22nm technology (Figs. 5 and 6).

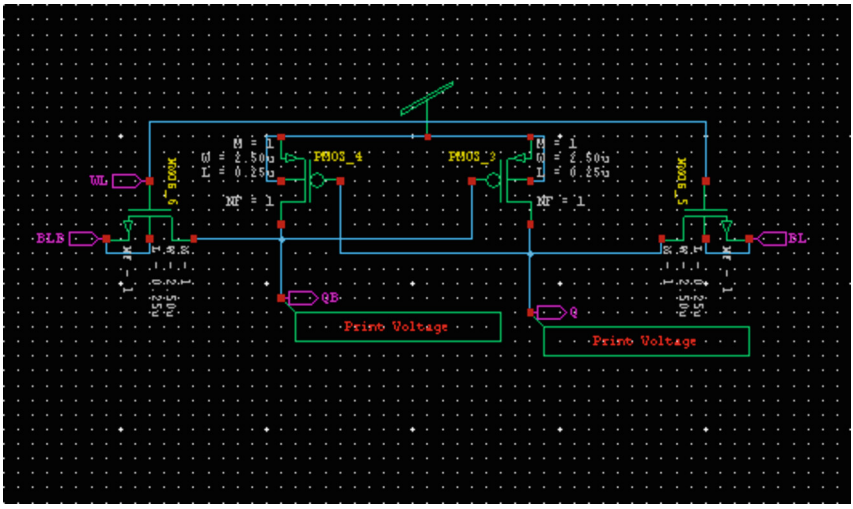

Fig. 4. Schematic Diagram of 4T SRAM Cell Using CMOS Technology

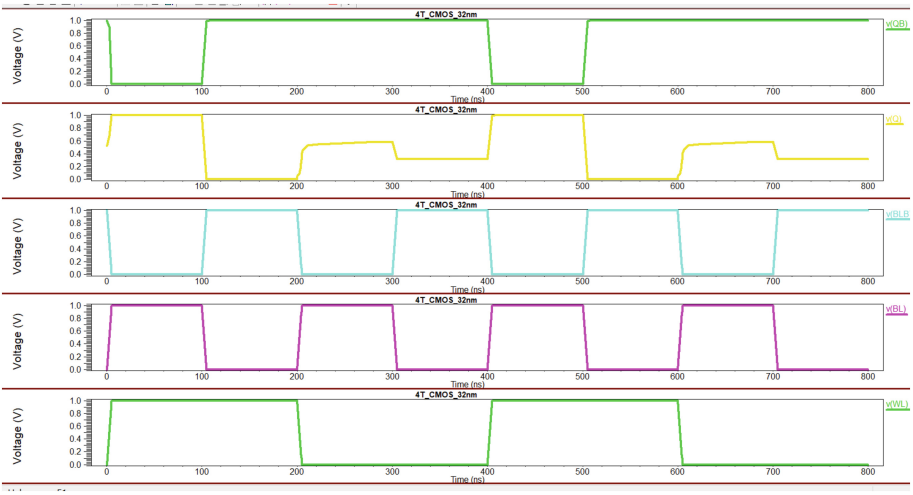

Fig. 5. 4T SRAM using CMOS output waveform at 32nm

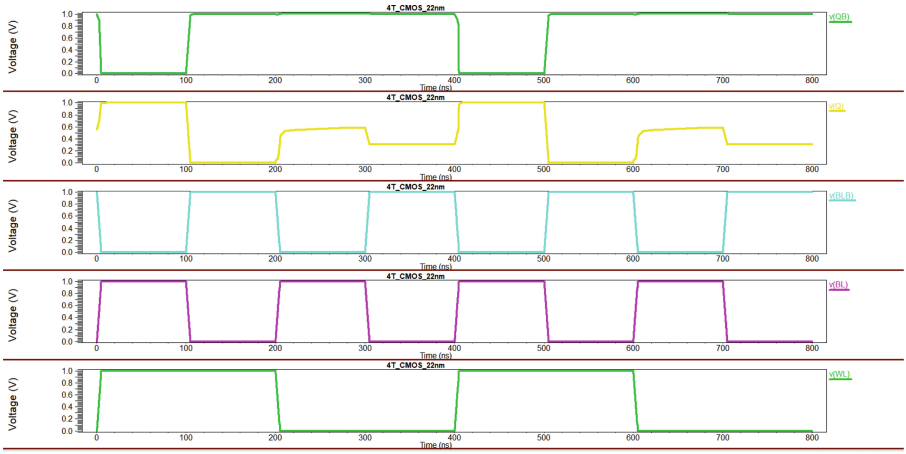

Fig. 6. 4T SRAM cell using CMOS output waveform at 22nm

4.2 4T SRAM Using Schmitt Trigger Technique at 32nm and 22nm

The 4T SRAM cell, upgraded with Schmitt trigger technology, exhibits characteristic waveforms during read and write operations in the 32nm technology environment [13]. As the Schmitt trigger amplifies the signal, the read operation waveform exhibits a quick and definitive reaction, contributing to a robust and noise-tolerant read process. Meanwhile, the Schmitt trigger's hysteresis improves the write operation, ensuring a controlled and dependable write process with less susceptibility to external disturbances. The waveforms continue demonstrating the usefulness of Schmitt trigger integration as the 4T SRAM cell grows toward the 22nm technology node. The waveform exhibits significantly faster access times and increased noise immunity during the read operation,

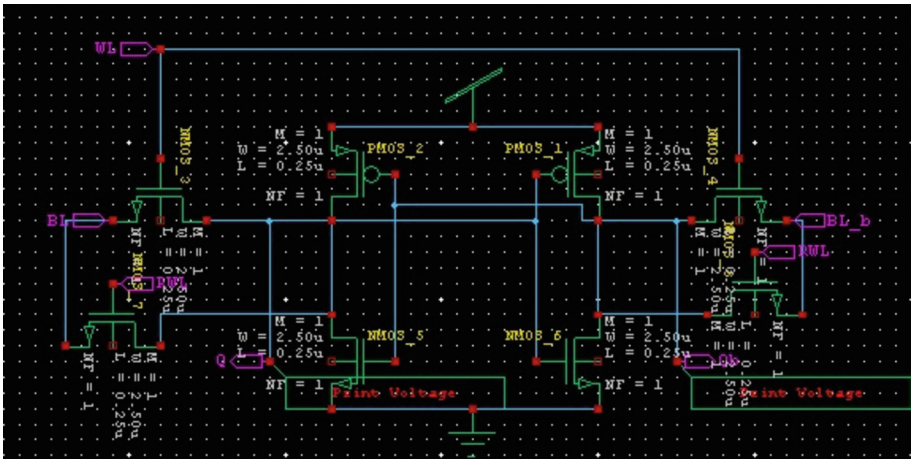

Fig. 7. Schematic Diagram of 4T SRAM Cell Using Schmitt Trigger Technology

increasing the cell's reliability. The write operation exhibits optimized waveforms as well, with the Schmitt trigger contributing to enhanced hysteresis and stability (Figs. 7, 8 and 9).

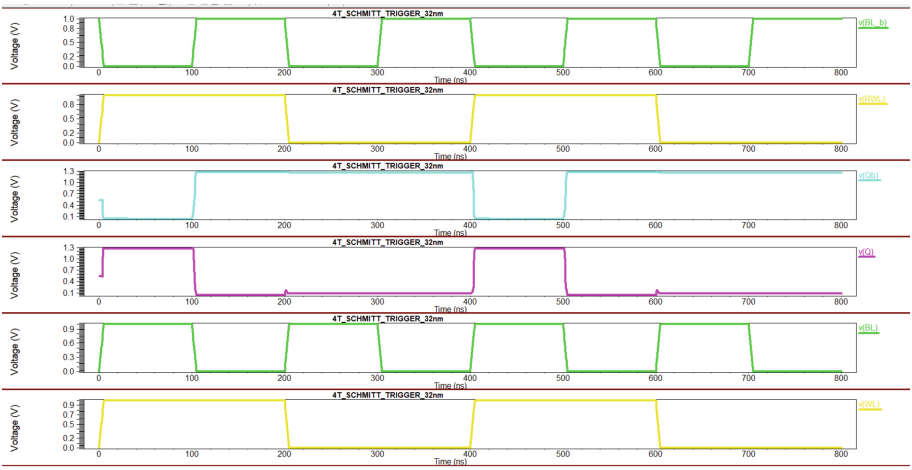

Fig. 8. 4T SRAM cell using Schmitt Trigger technique output waveform at 32nm

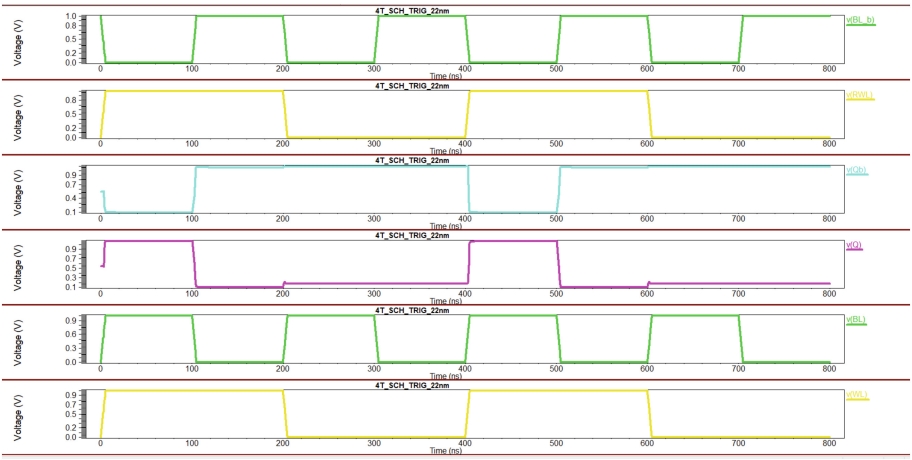

Fig. 9. 4T SRAM using Schmitt Trigger output waveform at 22nm

4.3 4T SRAM Using Adiabatic Technique at 32nm and 22nm

During read and write operations, the 4T SRAM cell adopting adiabatic techniques exhibits unique waveforms. The read operation waveform demonstrates a planned energy transfer technique that emphasizes power dissipation minimization during data retrieval. The adiabatic method enables a well-controlled and efficient read operation, improving power efficiency. The adiabatic approach optimizes energy flow during the write operation, resulting in a regulated and precise write process that meets the criteria of the 32nm technology node [14].

As the technology node moves to 22nm, the 4T SRAM cell with adiabatic techniques continues to redefine waveforms in both read and write operations [15]. The read waveform uses energy more efficiently, resulting in faster access times and lower power usage. Similarly, the adiabatic technique helps the write operation, demonstrating greater energy control and stability during data storage. In the advanced landscape of 22nm technology, these tailored waveforms highlight the versatility and increased efficiency of the 4T SRAM cell utilizing adiabatic approaches (Figs. 10, 11 and 12).

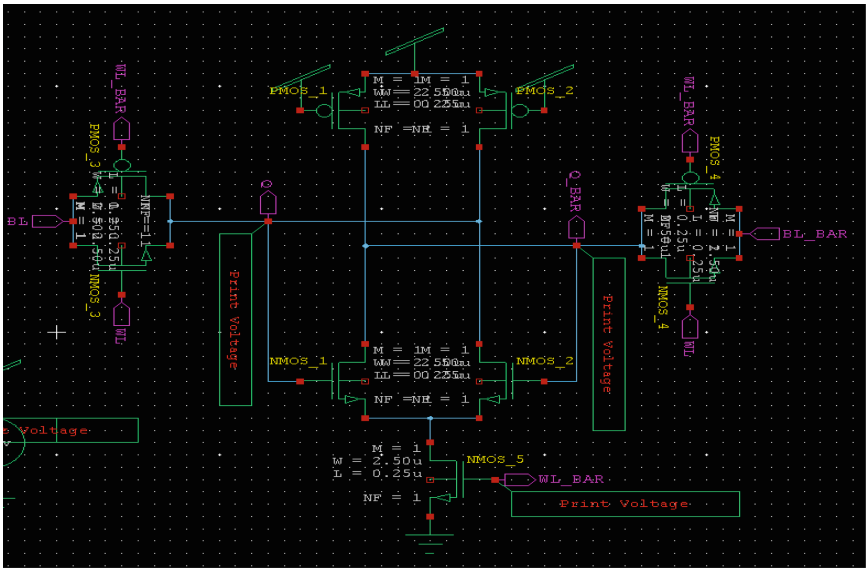

Fig. 10. Schematic Diagram of 4T SRAM Cell Using Adiabatic Technique

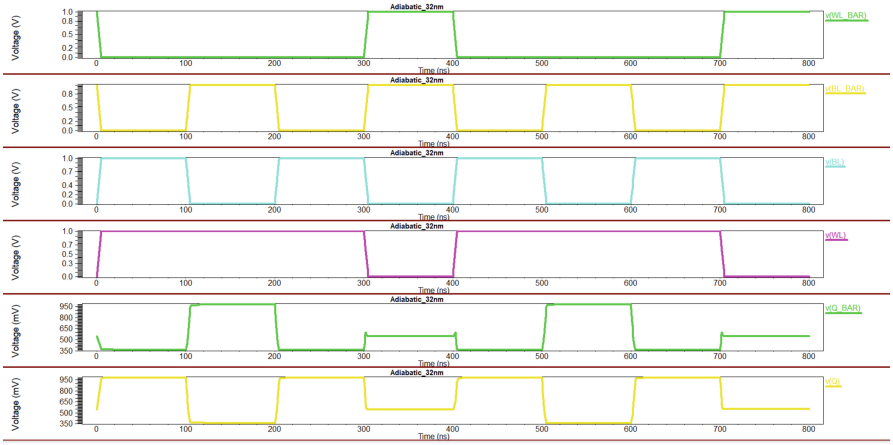

Fig. 11. Adiabatic technique output waveforms at 32nm

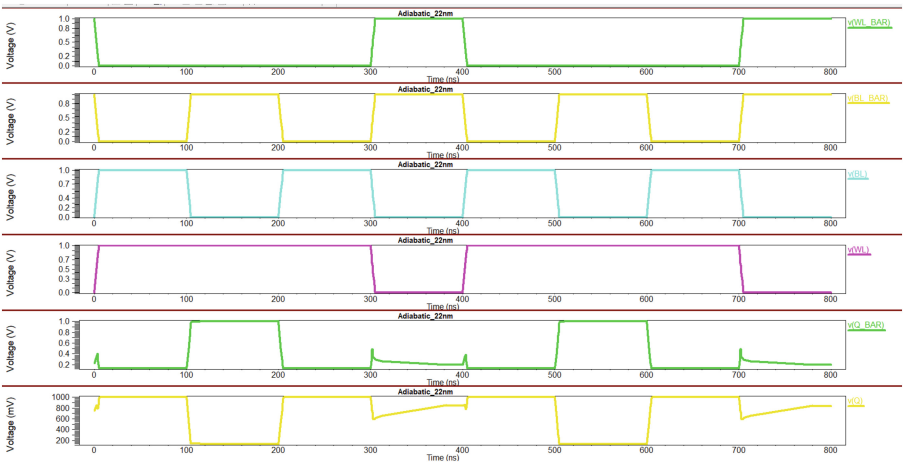

Fig. 12. Adiabatic technique output waveform at 22nm

5 Performance Comparisons

From Table 1 the power-delay product (PDP) is a metric used to evaluate the efficiency of digital circuits, considering both power consumption and performance (delay). It's calculated by multiplying the power dissipation (P) by the delay (D) of the circuit operation. Lower PDP values indicate better efficiency. For CMOS adiabatic logic, the PDP is generally lower compared to conventional CMOS logic due to the energy recovery mechanisms utilized in adiabatic circuits. Adiabatic logic aims to minimize energy dissipation by recycling energy stored in capacitors (Fig. 13).

Table 1. Comparison table at different nodes.

Methodologies	Power (μW)	Delay (ns)	PDP (pws)
CMOS_32nm	3.94	1.0149	3.99
CMOS_22nm	6.27	1.0150	6.36
Schmitt trigger_32nm	2.70	2.0112	5.43
Schmitt trigger_22nm	3.93	2.0103	7.90
Adiabatic_32nm	3.24	1.0015	3.24
Adiabatic_22nm	3.30	1.0001	3.30

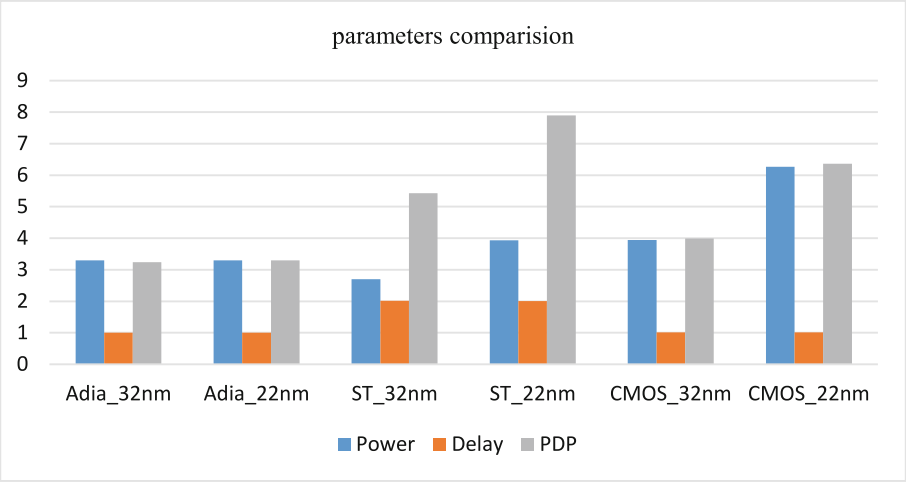

Fig. 13. paramters Comparison

6 Conclusion

In conclusion, the investigation of 4T SRAM at the 22nm and 32nm technology nodes using CMOS technology, Schmitt trigger, and adiabatic methodologies represents a strategic integration to address critical issues in memory cell design. The use of CMOS technology improves scalability and efficiency, the use of a Schmitt trigger improves stability, and the use of adiabatic technology coincides with the industry's aim of energy efficiency. This combination provides a balanced solution for advanced semiconductor applications by optimizing power consumption, speed, and stability. The 4T SRAM cell appears as a promising choice, demonstrating the ability of this integrated method to handle the severe demands of modern electronic systems while also paving the way for future semiconductor memory design breakthroughs.

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