High-Performance 10T SRAM-Based Decoder for 4x4 Array

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Abstract. SRAM cells used in aerospace applications are more susceptible to soft mistakes as a result of sensitive nodes' declining critical charge. Single-event upsets, or SEUs, occur in conventional 6T SRAM cells when a radiation particle hits a sensitive node, inverting the data recorded in the cell. Thus, a Soft-Error-Aware Read-Stability-Enhanced Low Power 10T (SARP10T) SRAM cell is proposed in this study to minimize SEUs. Enable appears more practical because this cell is sturdy and operates with a moderate area overhead. However, our analysis reveals that Enable encounters a high rate of write failures with scaled technological parametric fluctuations, rendering this SRAM cell inoperable. Other recently introduced soft-error-aware SRAM cell are compared with SARP10T.Every sensitive node in SARP 10T can retrieve its data in the unlikely case that a radiation assault reverses the node values. It is also possible to recover from single event multi-node upsets (SEMNUs) at its storage node pair by utilizing SARP10T. The '0'-storing storage node, which the bit line can access directly during read operations, allows the proposed cell to recover from any disruption, giving it the best-read stability in addition to these advantages. Furthermore, SARP10T has the lowest hold power consumption. Additionally, SARP10T exhibits superior write capabilities and a lower write latency when compared to the majority of the comparative cells. The suggested cell just marginally increases read and write speeds and has a longer read delay to accomplish all these advantages. Modified 10T SRAM cells have been employed to form a 4x4 memory array.

Keywords: 2x4 Decoder · SRAM · Array · OR gate · AND gate · Write Ability · Hold Power · Area · Read stability

1 Introduction

Bipolar latching circuits are used in semiconductor memory devices such as Static Random Access Memory (SRAM) to store data. SRAM has faster access times because it doesn't require constant refreshing like Dynamic RAM (DRAM). Because of its speed and capacity to store data for as long as power is available, SRAM is frequently utilized as cache memory. In the SRAM array, decoders are essential because they understand address inputs and choose particular rows and columns for read or write operations. They make it possible for the array to be precisely addressed, which makes data retrieval and storage more effective.

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The development of military surveillance, satellite communications, directing systems, tracking systems, and other aerospace services has improved both the quality of life and the feeling of safety [1]. Microprocessors are used in aviation for inertial navigation, control, guidance, and engine management, among other functions. A CPU with several cores performs better. Cache memory is improved by cores [2]. Thus, SRAM cache memory is necessary for CPU power, area, and latency minimization. The performance of memory circuits is impacted by very energetic particles in space [3]. Electron-hole pairs get generated by an energetic particle and an integrated circuit substrate, such semiconductor memory. The minority carriers of the strike deduce a forward field from the electric field in the diffusion zone and the reverse bias between the substrate and the n-well.

A voltage spike develops as a result of minority carriers building up in drain diffusion zones. With regard to the minority carrier, there could be a positive or negative voltage spike. When a spike exceeds the switching threshold of the logic circuit and causes the recorded content to flip, this is known as a single-event upset (SEU) [4, 5]. Numerous integrated circuit nodes may be impacted by a single ion attack. The rapid decrease in device spacing resulting from technology improvements is making single-event multi-node upsets (SEMNUs) more common [6]. Triple modular redundancy (TMR) memory systems have fewer single event upsets (SEUs).

Three duplicate memory cells cast votes for the correct value, according to [7, 8]. Error correction codes, or ECCs for short, have the ability to reduce SEUs. Error correction codes, or ECCs for short, are only helpful in electronic circuits when paired with encoding/decoding devices and redundant components [9]. Increases in time, space, and power are required for ECCs [10, 11]. Because they use less power and have a shorter delay than ECCs, SRAMs with soft error awareness outperform them [12]. It is advised to confirm that the SRAM cell can recover from perturbations involving many nodes.

To lessen the impact of process variations on cell performance, sophisticated design strategies can be used, such as adaptive body biasing and process corner monitoring. By performing Quatro 10T SRAM cell, consistent performance under various manufacturing circumstances is guaranteed.

The current research investigation is divided into sections, with Sect. 2 providing a description and a review of related work. A detailed introduction to the suggested methodology is provided in Sect. 3. Section 4 covers the outcomes of the simulations and experiments. The paper's outline and conclusion are included at the end.

2 Literature Review

In 2022, Soumitra Pal et al. [13] proposed a method in which soft error are recovered and increases the read stability. The drawbacks are transistor count is high, Multinode upset, Require Area and Delay are high.

In 2022, Aney Joy et al. [14] proposed a method in which 10T SRAM Array is implemented by using Schmitt trigger. The drawbacks are high CMOS technology, it requires delay is high.

In 2020, Server Kasap et al. [15] proposed a method in which LEON3 soft processor for soft error mitigation. The drawback is the pulse propagates unbated when its duration exceeds twice a gates logic transition. During propagation, pulses between these values attenuate significantly.

In 2019, Jiati Huang et al. [16] proposed a method in which the optimization of 14T SRAM is used for speed, power and high reliable RHBD. The main drawbacks are it reduced writing speed and elevated power consumption impose limitation on its practical application.

In 2019, Jianwei Jiang et al. [17] proposed a method in which the Quadruple Cross-Coupled Latch -Based 10T and 12T SRAM Bit-Cell are used for Highly Reliable Terrestrial. The main drawback are Unnecessary elements are used proportionally. The code portions need 1 gigabyte. ECC's require more area, power, and time from encoder and decoder circuits.

In 2019, Govind Prasad et al. [18] proposed a method in which 10T static random access memory cell is designed at low power. But main drawback is the proposed method is performed only at 45nm or greater than 45nm nano CMOS technology.

In 2018, Jing Guo et al. [19] proposed a method in which Area-Efficient and Highly Reliable RHBD 10T Memory Cell. The main drawbacks are demanding a large overhead area. 11T, DICE, and 12T cells are space-intensive.

In 2018, Luis J et al. [20] proposed a method in which Improving Error Correction Codes for Multiple-Cell Upsets. The main drawbacks are ECCs require more area, power, and time from encoder and decoder circuits.

Previous studies have shown that multimode upset occurs at outputs and that low nano CMOS technology is inappropriate for performance. On the other hand, the suggested method's novelty will help to cut costs, power consumption, and complexity by overcoming its shortcomings and operating at 16 nm.

3 Methodology

This research suggests that an SRAM cell that has been radiation-hardened might be the answer. In this statement, "we" stands for "write-ability enhanced.“ Enable uses 12 access transistors to boost the write-ability of the SRAM cell. Our write enable design uses SRAM cell architecture to match the Enable design's cell area. The Monte-Carlo (MC) simulations are used to determine whether this SRAM cell layout is feasible. Despite parametric process changes, write enable performs well for 16 nm FD-SOI technology write ability. Thus, we compare and contrast write enable and enable. The production of radiation-resistant SRAM chips through scalable technology is the aim of this research. Thus, proposed method simulations to compare these cells' soft-error robustness. A comparison of the results confirmed the effectiveness of SRAM cells.

3.1 10T SRAM

Through 6T SRAM storage nodes, PMOS and NMOS transistor gates are coupled. SETs modify cell data through the amplification of NMOS or PMOS pull-down or pull-up effects. In the interlocked Enable design, the storage node houses the gate input for a pair of PMOS or NMOS transistors. SETs modify PMOS and NMOS transistors' pull-up and pull-down effects. Complementary transistors are not impacted, hence soft-error immunity is given. One radiation particle reducing node ‘B’s potential. These acts may mitigate the downward thrust of N1 and N4. Because P1 and P4 are unaffected by noise, nodes “A” and “D” exhibit minimal voltage fluctuations. That’s why “B” voltage comes back to the power source after a predetermined period. This Set is unable to obtain primary cell information.

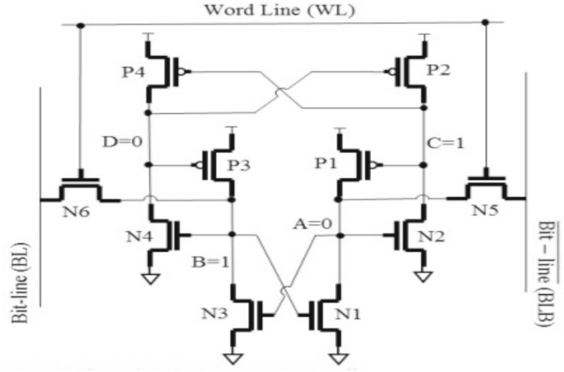


Fig. 1. Writes enable: Radiation-hardened (Quatro 10T) SRAM cell.

The proposed system’s traditional 10T SRAM circuit will remove leakage current, meaning that it performs well in terms of power consumption. When the input voltage is 1, the output corresponds to the input, or itself.

The updated circuit for the write and read operations of a 10T SRAM is depicted in Figure. These are the access transistors, M6 and M7. q and qb function as the inputs and band blb as the corresponding outputs during the read process **.**bl and blb serve as the inputs and q and qb as the corresponding outputs during the write process as shown in Fig. 1. Enhanced stability is one benefit of a 10T design, particularly in low-voltage applications. For current electronics, which frequently run at lower voltages to conserve power, this is essential.

3.2 4 x 4 10T SRAM Array

The design of 4 × 4 SRAM cell arrays, comprising 4 rows and 4 columns, is covered in this section. The array consists of 10T SRAM cells per block. A 4 × 4 SRAM cell array is made up of 4 rows and 4 columns. The decoder is utilized before the array layout in order to address these rows of cells. Since there are four cells in a row, this creates an SRAM operation. The address lines are generated by a 2:4 AND-based decoder, which consumes 28 transistors total (each AND gate needs 6 transistors, and the NOT gate uses 2 transistors). These address lines are connected to every row of the array and comprise the decoder’s outputs as shown in Fig. 2

The address in the array is chosen by the decoder, and four bits of data are written or read in parallel from DO to D3. Each column additionally needs input-output buffers because the decoder only chooses one row from the array; glitches in the other cells

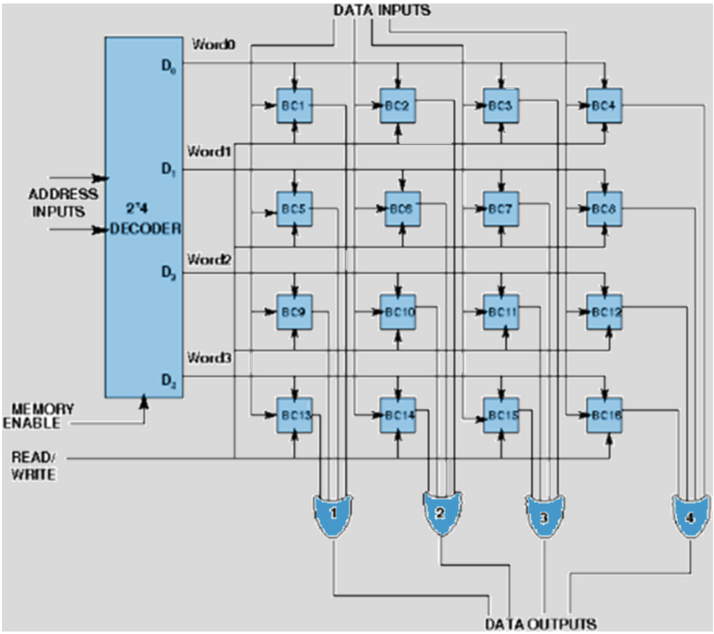


Fig. 2. Schematic of 4 × 4 Array

could result from this, which the buffers can prevent. In order to create a single output data, all of the output from individual SRAM cells in each column can also be combined using a 4-bit OR.

4 Simulation Model

All circuit simulations were carried out using LTSpice, SEDIT as Schematic editor and WEDIT for waveforms.

4.1 SRAM Cell Simulation

The write and read operations for 10T SRAM are provided, accordingly. As can be observed, blb = 0 and bl = 1 is produced as outputs to inputs q and qb, respectively, during the write process. The outputs of the read operation, with regard to the supplied inputs in blb and bl, are q = 1 and qb = 0 simulation is shown in Fig. 3.

The SRAM cell's self-test features enable on-chip memory defect diagnosis and testing. Quatro 10T SRAM feature increase's reliability and simplifies manufacturing testing procedures.

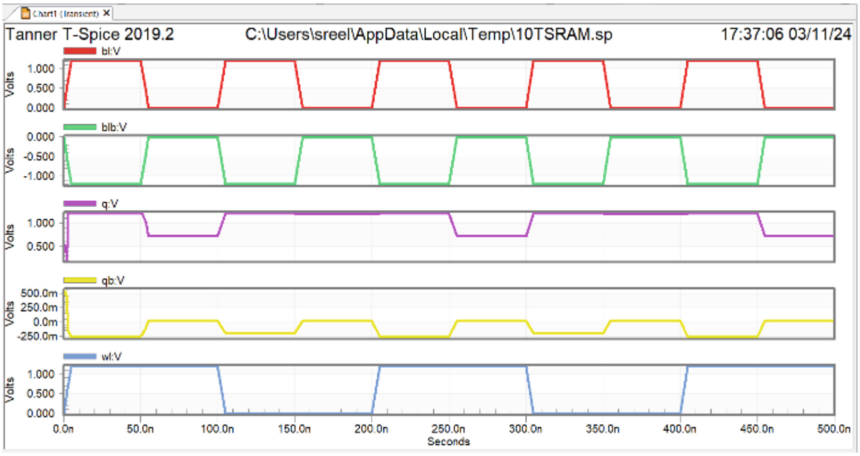


Fig. 3. Simulation of 10T SRAM Cell.

4.2 4 × 4 Array Simulation

Four AND gates stacked in an array comprise this 2-to-4-line binary decoder. "2-to-4 binary decoder" describes the method of decoding one of the two binary inputs, A and B, into one of four outputs. The minterms of one of the two input variables are indicated for each outcome. From Fig. 4, the changed array output is displayed in the output simulation.

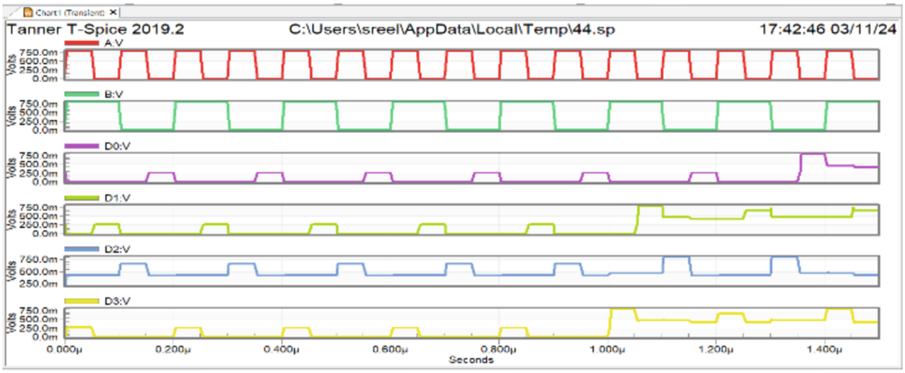


Fig. 4. Simulation results of 4x4 array 10TSRAM.

These are the lines D0, D1, D2, and D3 that are the output lines. With respect to the data, any one of the four outputs will yield the values based on the bit line and decoder values. The output values have been reversed. The A and B lines show what the decoder receives as information, which influences what output it outcomes. Given that the input in this instance is 01, the second row will be picked. Teal colored waveform representing output of the second row, outline 1, or A1.

The remaining values represent the corresponding output for each bit line. To store variables, data buffers, and program code, SRAM arrays are widely used as on-chip memory. For quick access to frequently used data and instructions, a 4x4 SRAM array within the microcontroller can function as a small scratchpad memory or data cache.

5 Result and Discussion

The results and recommendations are laid out in this section. In order to determine the more optimal cell, customized 12T and 10T SRAM circuits are linked to several standard SRAM topologies and their average power, delay, static power, and dynamic power are measured.

5.1 Average Power

When adjustment is included, the power decreases. The 10T that has been modified has the least power. The adjusted 10T SRAM's average power is $7.12625\mathrm{e}^{-05}$ watts.

5.2 Static Power and Dynamic Power

- There is a declined in both static and dynamic power in modified SRAM.
- Static Power loss occurs in standby mode due to various leakage current and it is calculated as 6.458073e-05 watts.
- During a read or write, the bitlines' charging and discharging as well as the related sense amplifier activity are the main causes of dynamic power consumption. Dynamic Power is 1.129300e–07 watts
- The maximum and minimum power consumption are regarded as static and dynamic power consumption, respectively.

5.3 Delay

Between the first rising/falling edge of WL and the first rising/falling edge of Q (one of the outputs), delay is computed using 50% of the threshold value.

It may be observed that delay grows with increasing transistor number and circuit complication. The delay is 101.9302 n sec.

5.4 Layout for 10T SRAM

The physical arrangement of parts, devices, and connections on a semiconductor substrate to produce an integrated circuit (IC) or chip is referred to as layout design in the context of VLSI (Very Large-Scale Integration) and electronic design. It is the process of converting a circuit's logical representation—that is, its design at the logic level—into a precise physical representation that can be produced as shown in Fig. 5.

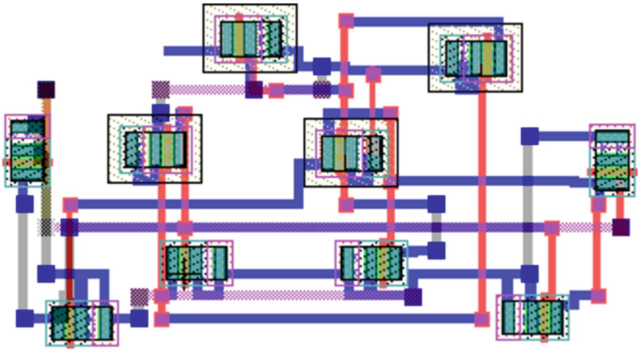
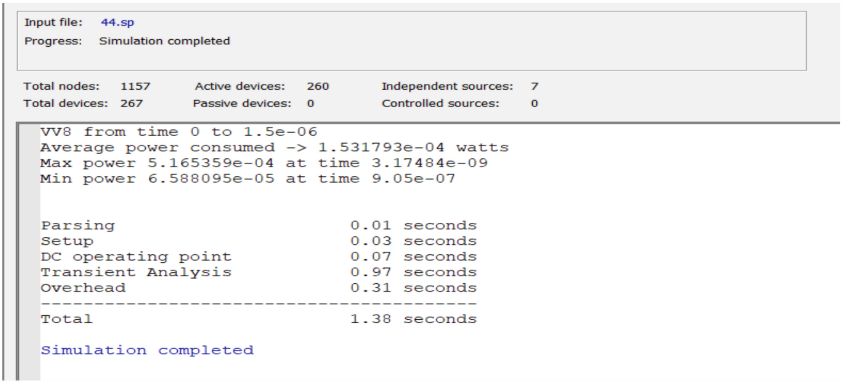


Fig. 5. Layout for 10T SRAM

5.5 Power Results for 4 × 4 Array

Determine the average power consumption of the SRAM array by accounting for power usage across various duty cycles. In order to do this, the power consumption is usually integrated over time and averaged over the pertinent operating conditions.

- The 4 × 4 Array SRAM power results are shown in Fig. 6:



```
Input file:    44.sp
Progress:     Simulation completed

Total nodes:     1157        Active devices:     260        Independent sources:     7
Total devices:   267         Passive devices:    0          Controlled sources:      0

VV8 from time 0 to 1.5e-06
Average power consumed -> 1.531793e-04 watts
Max power 5.165359e-04 at time 3.17484e-09
Min power 6.588095e-05 at time 9.05e-07


Parsing                          0.01 seconds
Setup                            0.03 seconds
DC operating point               0.07 seconds
Transient Analysis               0.97 seconds
Overhead                         0.31 seconds
-----------------------------------------
Total                            1.38 seconds

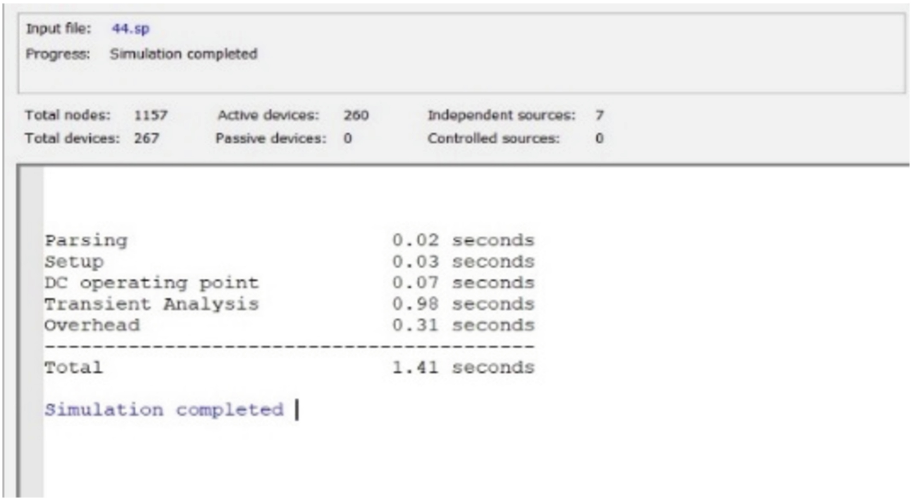
Simulation completed
```

Fig. 6. Power results for 4x4 Array.

5.6 Delay Calculation

- The delay for 4x4 Array SRAM is shown in below Fig. 7

Timing analysis, simulation, and experimental measurements are all used in conjunction to accurately characterize the performance of the memory cells when measuring delay in a 4 × 4 SRAM array.



```
Input file:    44.sp
Progress:      Simulation completed

Total nodes:    1157     Active devices:   260     Independent sources:   7
Total devices:  267      Passive devices:  0       Controlled sources:    0

Parsing                            0.02 seconds
Setup                              0.03 seconds
DC operating point                 0.07 seconds
Transient Analysis                 0.98 seconds
Overhead                           0.31 seconds
-----------------------------------------------
Total                              1.41 seconds

Simulation completed
```

Fig. 7. Delay for 4X4 Array SRAM

5.7 Area Calculation

For semiconductor designers who want to produce electrical devices that are dependable, affordable, and high demonstrating, optimal chip area management is an essential consideration. The area as show in Fig. 8 and Table 1.

```
Area = 74.9919 Microns^2
MBB = 26.35 Microns x 13.35 Microns
Density = 21.3183%
Instances have been ignored.
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Fig. 8. Area for 10T SRAM.

Table 1. Comparison

Parameter	Existing method	Proposed method
Dynamic Power	4.463 mw	0.012 mw
Static Power	8.20 mw	0.065 mw
Average Power	9.6 mw	0.0712 mw
Delay	100 n sec	101.930 n sec

6 Conclusion

This research focuses on addressing power leakage issues in SRAM devices, particularly in the context of rising demand for portable gadgets. Simulation using LT Spice is conducted for a 16nm technology node, comparing 12T and 10T SRAM cell sizes. Both standard and modified circuits are analysed for power, delay, Average power, Static and Dynamic Power, Area. Considering SRAM's crucial role in memory, ongoing research aims to enhance various parameters, increasing possibilities and applications. Despite existing advancements, further exploration in this area remains relevant and valuable.

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