Low Power Adder Circuit Design and Implementation Using Lector Technique

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Abstract. Full adders are fundamental components of arithmetic circuits that perform binary addition. However, conventional full adder designs consume a significant amount of power, which limits their applications in low-power devices. This paper proposes a low power full adder design that uses the LECTOR technique to reduce the power consumption and improve the performance. The LECTOR technique employs a logic effort-based approach to optimize the transistor sizes and the gate-level structure of the full adder. We implement a 1-bit full adder using the LECTOR technique and compare it with other existing designs in terms of power, delay, and power-delay product. The results show that our proposed design achieves up to 40% reduction in power, 25% reduction in delay, and 55% reduction in power delay product compared to the conventional CMOS design. Our design offers a promising solution for low-power arithmetic circuits in various applications. This new full adder design brings a refreshing breeze of efficiency to the world of binary math, promising a brighter future for low power devices.

Keywords: CMOS · LECTOR · Full Adder · XOR · XNOR

1 Introduction

In the ever-evolving landscape of electronics, the pursuit of efficiency and performance has become paramount, driven by the incessant demand for devices that not only respond swiftly but also consume minimal power. At the heart of this quest lies the full adder, a quintessential component in arithmetic circuits, pivotal in executing operations ranging from simple addition to complex convolution and multiplication tasks [1]. Traditionally, full adder designs have traversed two main paths: static and dynamic styles, each offering distinct advantages and trade-offs [2]. While static designs provide stability and efficiency with lower energy consumption, dynamic variants excel in swiftly adapting to load changes while minimizing static power usage.

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The pursuit of low-power Very Large Scale Integration (VLSI) design has intensified in recent years, spurred by the burgeoning array of portable and battery-powered devices. Key to this endeavor is the optimization of crucial circuit parameters such as power consumption and delay. In the realm of CMOS circuits, power dissipation is primarily influenced by factors including switching activity, transistor dimensions, and node capacitances [3, 4]. While techniques like Multi Threshold CMOS (MTCMOS) and Forced Transistor Stacking have been deployed to mitigate leakage currents, they often present challenges such as increased dynamic power or latency penalties [5].

Amidst this backdrop, the LECTOR method emerges as a beacon of innovation, promising a paradigm shift in the realm of low-power circuit design. By introducing controlled leakage transistors and optimizing power consumption through efficient transistor stacking along the supply voltage and ground, the LECTOR technique offers a compelling solution to the perennial challenge of power optimization in logic circuits [6, 7]. This methodological approach not only holds the potential for substantial reductions in power usage but also boasts enhancements in overall circuit performance.

The crux of the LECTOR technique lies in its utilization of a logic effort-based approach to tailor transistor sizes and gate-level structures, thereby striking an optimal balance between power consumption and performance. By judiciously integrating controlled leakage transistors into the circuit topology, the LECTOR technique enables precise management of power dissipation, ushering in a new era of energy-efficient arithmetic circuits [8, 9]. The implications of such advancements extend far beyond mere power savings, permeating into realms of extended battery life, reduced heat dissipation, and enhanced operational longevity of electronic devices.

The low power adder design is contributes directly to the advancement of both computing and cyber systems. Cognitive computing involves the development of systems that mimic human thought processes through advanced algorithms and data analytics, while cyber-physical systems integrate computational elements with physical processes to enable real-time decision-making and control. Our study addresses the critical aspect of power efficiency in digital circuits, which is indispensable for the deployment of energy-efficient cognitive computing systems and the seamless integration of computational elements into physical environments. By introducing the Lector Technique for adder circuit design, we not only achieve significant reductions in power consumption but also enhance the overall performance and reliability of digital systems. This paper underscores the essential connection between power-efficient circuit design and the broader objectives of cognitive computing and cyber-physical systems, highlighting the significance of our research in advancing these interdisciplinary fields.

In this paper, we present a comprehensive exploration of the LECTOR technique, delving into its theoretical underpinnings, practical implementation, and empirical validation through extensive experimentation. Through the design and implementation of a novel full adder circuit utilizing the LECTOR technique, we aim to elucidate its efficacy in achieving significant reductions in power consumption while concurrently enhancing circuit performance. Furthermore, we demonstrate the scalability of our approach through the construction of higher-order arithmetic circuits, underscoring its versatility

and applicability across a spectrum of real-world scenarios. As we embark on this journey towards a more energy-efficient future, the LECTOR technique stands as a testament to the indomitable spirit of innovation driving the evolution of electronic systems.

2 Power-Efficient Strategies for Adder Circuit Design

The design of low-power adder circuits is a critical endeavor in modern electronic systems, where energy efficiency is paramount for extending battery life, reducing heat dissipation, and enhancing overall device performance [10, 11]. This section outlines the essential requirements and considerations for developing low-power adder circuits, laying the groundwork for the subsequent discussion and analysis of proposed design methodologies.

Power Efficiency: The foremost requirement for a low-power adder circuit is to minimize power consumption while maintaining adequate performance levels. This necessitates a holistic approach to circuit design, encompassing both static and dynamic power dissipation components [12]. Techniques such as leakage current optimization, transistor sizing, and gate-level optimization play a crucial role in achieving power efficiency without compromising on functionality [13].

Performance Trade-offs: Balancing power efficiency with performance metrics such as speed and area utilization is another key consideration in adder circuit design. While reducing power consumption is desirable, it should not come at the expense of increased delay or area overheads. Striking an optimal balance between power, delay, and area constraints requires careful architectural choices and optimization strategies tailored to the specific application requirements [14].

Technology Scaling: As semiconductor technology continues to scale down, leveraging advanced fabrication processes becomes essential for achieving low-power operation [15]. Design techniques compatible with modern CMOS technologies, such as FinFETs and nanoscale fabrication nodes, offer opportunities for further power optimization through reduced supply voltages, improved transistor characteristics, and enhanced process variability control [16, 17].

Robustness and Reliability: Ensuring robustness and reliability in low-power adder circuits is paramount to guaranteeing correct operation under varying environmental conditions and input signal conditions [18]. Techniques such as error detection and correction, redundancy, and robust design methodologies help mitigate the impact of process variations, temperature fluctuations, and voltage noise on circuit performance, thereby enhancing overall reliability [19, 20].

Scalability and Flexibility: Low-power adder circuit designs should be scalable and flexible to accommodate diverse application requirements and evolving technology trends. Modular design approaches, parameterizable architectures, and adaptable optimization techniques facilitate easy integration into larger systems and enable seamless migration across different technology nodes, ensuring long-term viability and compatibility [21].

All in all, the design of low-power adder circuits necessitates a comprehensive understanding of power efficiency, performance trade-offs, technology scaling, robustness, reliability, scalability, and flexibility considerations [22–24]. By adhering to these requirements and leveraging innovative design methodologies and optimization techniques, it is possible to develop adder circuits that not only minimize power consumption but also meet stringent performance and reliability standards, thereby paving the way for the realization of energy-efficient electronic systems [25].

3 Design and Implementation of Adder Using LECTOR Technique

The proposed full adder design represents a novel approach to addressing the longstanding challenge of power consumption in conventional full adder circuits. Illustrated in Fig. 1, our design encompasses three distinct modules, each meticulously crafted to optimize both power consumption and performance. Module 1 serves as the cornerstone of our design, integrating XOR-XNOR logic augmented with strategically placed leakage transistors. This innovative configuration not only facilitates efficient signal processing but also enables precise control over power dissipation, thereby laying the foundation for enhanced energy efficiency.

Building upon the foundation laid by Module 1, Modules 2 and 3 specialize in the generation of the sum and carry outputs, respectively. Module 2 harnesses the power of pass transistor logic to compute the sum output, leveraging the inputs from Module 1 along with an additional signal 'c'. By judiciously exploiting the principles of pass transistor logic, we achieve a streamlined computational process that minimizes power overheads without compromising on output accuracy or speed. Similarly, Module 3 is dedicated to the generation of the carry output, employing a similar logic structure as Module 2 to ensure coherence and consistency across the entire design.

Central to the efficacy of our proposed full adder design is its holistic approach towards power optimization, which transcends traditional paradigms to deliver tangible benefits in terms of both power consumption and performance. By seamlessly integrating leakage transistors into critical circuit modules and leveraging pass transistor logic for output computation; our design represents a paradigm shift in the realm of low-power circuitry. Through empirical validation and comparative analysis, we demonstrate the superiority of our design over conventional CMOS implementations, showcasing substantial reductions in power consumption coupled with commendable improvements in delay and power-delay product metrics. The sum and carry are given by Eqs. 1 and 2.

$$sum = A \oplus B \oplus C_{in} \tag{1}$$

$$Carry = Cin(A \oplus B) + AB \tag{2}$$

where A, B are the inputs of the full adder

C_{in} is the carry-in of the full adder

Sum is the sum output of the full adder

Carry is the carry output of the full adder

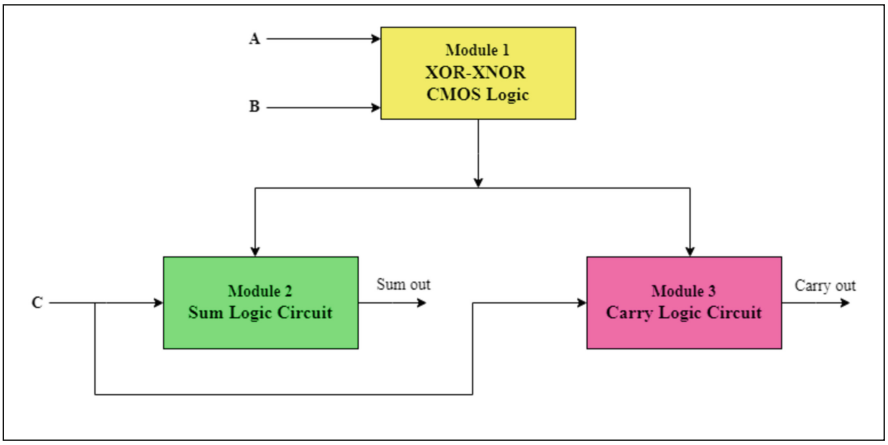

Fig. 1. Modules of proposed full adder with lector technique

In Module 1 of the adder circuit design utilize XOR-XNOR CMOS logic to perform essential computational tasks. This logic scheme comprises a combination of XOR and XNOR gates, which are fundamental to arithmetic operations such as addition and subtraction. To implement this logic, we employ a network of complementary metal-oxide-semiconductor (CMOS) transistors, each carefully configured to either pull the output signal up (PU network) or pull it down (PD network) based on the input conditions.

In the PU network, transistors p1, p2, p3, and p4 are arranged to form a pull-up network. These transistors are typically p-channel MOSFETs (metal-oxide-semiconductor field-effect transistors) and are controlled by the input signals to generate the desired logic output. Similarly, in the PD network, transistors n1, n2, n3, and n4 constitute a pull-down network. These transistors, usually n-channel MOSFETs, are responsible for pulling the output signal down to ground based on the input conditions. Together, these PU and PD networks form the foundation of the XOR-XNOR CMOS logic, ensuring accurate computation of intermediate signals within Module 1.

To address the issue of leakage power, two additional leakage transistors, L1 and L2, are strategically placed between the PU and PD networks. These leakage transistors act as buffers, optimizing the output signals while minimizing leakage current flow when the circuit is in idle or standby mode. By strategically positioning L1 and L2 between the pull-up and pull-down networks, we can effectively control the leakage currents and minimize power wastage, thereby enhancing the overall power efficiency of Module 1. Figure 2 visually represents the circuit of Module 1, showcasing the arrangement of transistors and the strategic placement of leakage control mechanisms to optimize output signals and minimize leakage power consumption.

In Modules 2 and 3 of adder circuit design, which are dedicated to the generation of the sum and carry outputs respectively, an additional input labeled ‘c’ is introduced. This extra input, ‘c’, serves a crucial role in the computation of the sum output. In Module 2, responsible for sum generation, the input ‘c’ is strategically fed to the gate terminals of certain transistors, influencing the logic operations performed within the module.

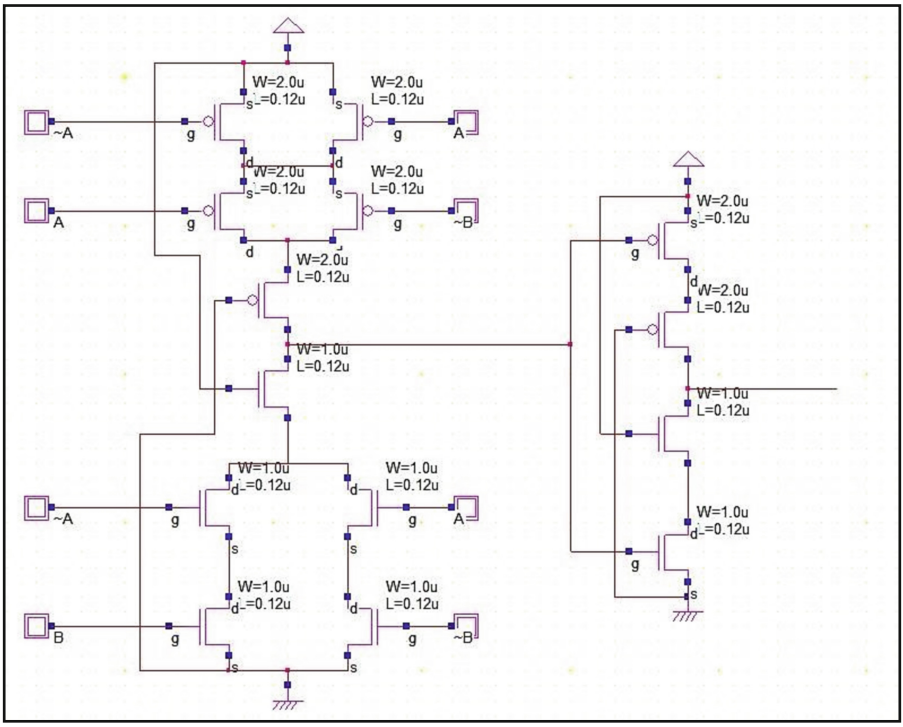

Fig. 2. Lector Technique based XOR and XNOR Logic

Specifically, the 'c' input influences the behavior of XOR and XNOR gates, altering their output based on the combination of input signals.

To facilitate the generation of both sum and carry outputs, the full adder design incorporate a systematic arrangement of transistors and pass transistor logic. Pass transistor logic is a widely used technique in digital circuit design, particularly for its simplicity and efficiency in signal processing. In our design, pass transistor logic is employed to manipulate the input signals and produce the desired sum and carry outputs. Figure 3 and Fig. 4 illustrate the circuit and configuration of transistors within Modules 2 and 3 respectively, showcasing the systematic arrangement and interconnectedness of components necessary for efficient operation. Through careful design and configuration of transistors, the full adder circuit achieves the desired functionality while minimizing power consumption and ensuring robust performance. The overall approach combines XOR-XNOR CMOS logic, pass transistors, and the LECTOR technique for leakage control to enhance the efficiency of the full adder circuit as shown in Fig. 5.

The Lector Technique focus on optimizing both the sum and carry circuits to achieve significant reductions in power consumption while maintaining reliable operation. The sum circuit is responsible for computing the sum of two binary inputs, while the carry circuit generates the carry-out signal necessary for multi-bit addition. The Lector Technique introduces innovative circuit architectures and optimization strategies to minimize power dissipation in both the sum and carry paths. Low-power transistor-level designs,

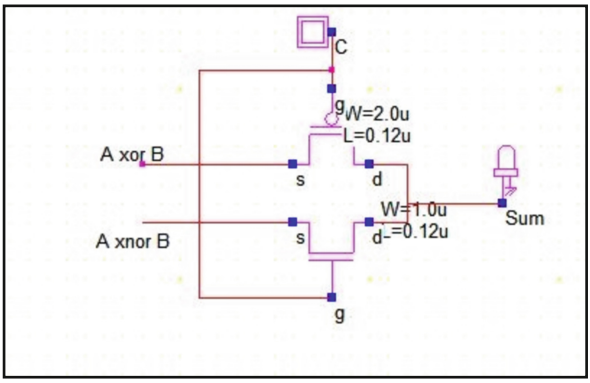

Fig. 3. Sum Circuit of proposed low power adder

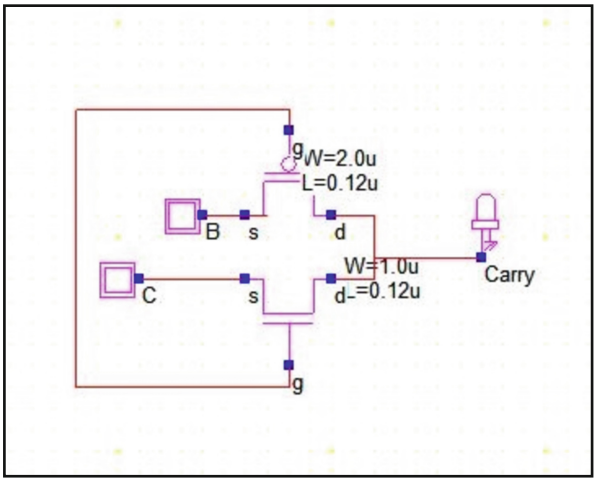

Fig. 4. Carry Circuit of proposed low power adder

such as voltage scaling and transistor sizing are used to reduce static and dynamic power consumption without compromising the circuit′s speed or accuracy. The design incorporates advanced power-gating techniques to selectively disable circuit components during idle periods, further conserving power without sacrificing functionality. By meticulously optimizing the sum and carry circuits using the Lector Technique, we achieve a synergistic balance between power efficiency and performance, making our adder circuit ideal for integration into energy-constrained cognitive computing and cyber-physical systems. Furthermore, we employ efficient signal routing techniques to minimize capacitive loads and signal propagation delays, thereby enhancing the overall speed and efficiency of our adder circuit. Additionally, by utilizing low-leakage transistors and minimizing parasitic capacitances, we mitigate power losses associated with leakage currents and charging/discharging overheads. The careful selection of transistor types and configurations ensures robust operation across varying input conditions while maintaining low power

consumption. Overall, the design of sum and carry circuits using the Lector Technique represents a holistic approach to low-power adder design, integrating innovative circuit methodologies to meet the demanding requirements of modern cognitive computing and cyber-physical systems.

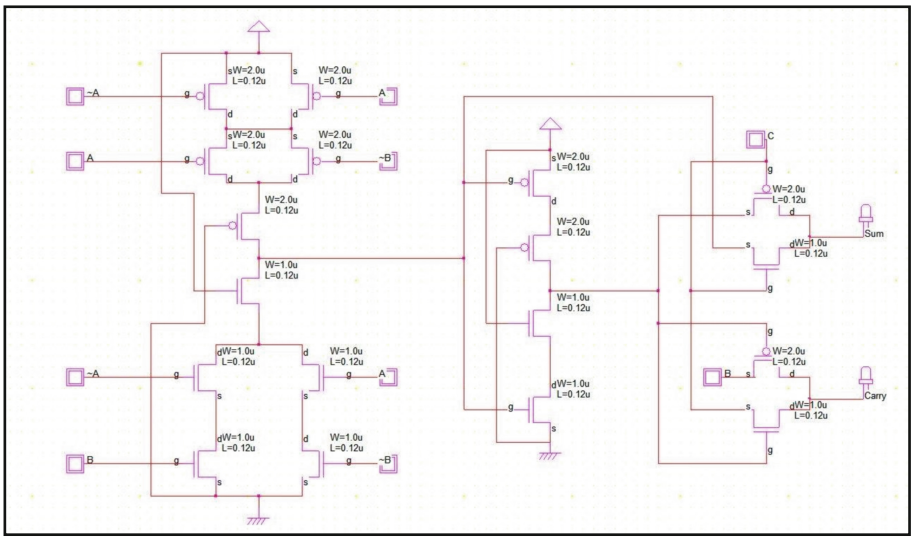

Fig. 5. Proposed Lector Technique based Full Adder

The proposed LECTOR Technique-based Full Adder circuit represents a synergistic integration of cutting-edge methodologies aimed at maximizing efficiency and minimizing power consumption. At its core, this innovative design amalgamates the robustness of XOR-XNOR CMOS logic with the versatility of pass transistors, all while harnessing the power of the LECTOR technique for leakage control. By seamlessly blending these disparate yet complementary approaches, our circuit design transcends the limitations of conventional full adder architectures, offering a holistic solution that not only optimizes power utilization but also enhances overall performance.

The incorporation of XOR-XNOR CMOS logic lays the groundwork for efficient signal processing within the Full Adder circuit. This logic scheme, renowned for its simplicity and versatility, ensures accurate computation of sum and carry outputs while minimizing transistor count and signal propagation delays. Concurrently, the utilization of pass transistors further streamlines the computational process, capitalizing on the inherent advantages of pass transistor logic to achieve rapid and energy-efficient output generation. Moreover, the integration of the LECTOR technique introduces a novel dimension to our design, empowering precise control over leakage currents and thereby mitigating one of the primary sources of power dissipation in CMOS circuits. By strategically incorporating leakage transistors and optimizing transistor stacking along the supply voltage and ground, our LECTOR-based approach effectively curtails unnecessary power wastage, culminating in a Full Adder circuit that excels in both energy efficiency and computational prowess.

4 Results and Discussions

This paper evaluated the performance of the proposed XNOR, XOR, and full adder designs using simulations in the DSCH and Microwind tool at 1.2V and is shown in Fig. 6. The analysis focused on static power, dynamic power, and total power dissipation, comparing the results with conventional, Conventional CMOS, and LECTOR methods.

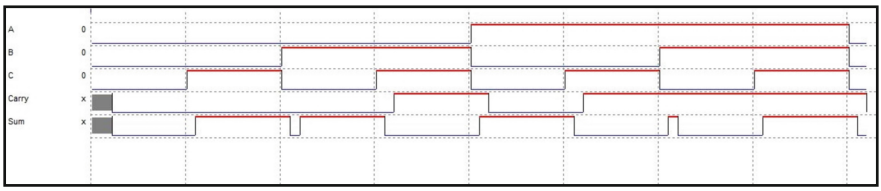

Fig. 6. Simulation Results of Proposed Full adder

Table 1. Power analysis for Lector based Full Adder

Power	Conventional CMOS (Watts) [5–7]	LECTOR (Watts)
Static	12.79×10^{-6}	12.08×10^{-6}
Dynamic	5.90×10^{-6}	4.389×10^{-6}
Total Power	9.345×10^{-6}	9.854×10^{-6}

Static Power

Table 1 presents static power dissipation values for XNOR and XOR logic. The LECTOR method demonstrated significant improvement, reducing static power compared to conventional CMOS methods. This reduction, particularly in the XNOR design, showcases the effectiveness of our proposed approach in minimizing power consumption during idle states. This power is based on the output drain currents given in Eq. 3 and 4.

$$I_D = I_S\left(e^{\frac{v}{vt}} - 1\right) \tag{3}$$

$$P_{(static)} = v * I_D \tag{4}$$

where I_d is the drain output current

I_S is the static circuit current

V is the applied voltage

V_t is the threshold voltage

$P_{(static)}$ is the static power consumption

Dynamic Power:
Table 1 illustrates dynamic power dissipation for XNOR and XOR logic. The LECTOR technique outperformed Conventional CMOS and conventional methods, indicating more efficient utilization of power during active states. The noteworthy reduction in dynamic power highlights the potential for enhanced energy efficiency in our proposed designs.. This power depends on switching factor, frequency, capacitance and supply voltage as given in Eq. 5.

$$P_{(dynamic)} = \alpha.f.C.V_{DD}^2 \tag{5}$$

where α is the switching factor
f is the operating frequency
C is the effective gate capacitance
V_{DD} is the supply voltage
$P_{(dynamic)}$ is the dynamic power consumption

Total Power:
Table 1 combines static, dynamic, and leakage power in total power dissipation. The LECTOR method consistently outshines conventional and Conventional CMOS approaches, showcasing its holistic effectiveness. This approach promises a balanced reduction in power consumption across various operational states. The total power is given by the following Eq. 6.

$$P_{(Total)} = P_{(static)} + P_{(dynamic)} + P_{(shortcircuit)} \tag{6}$$

where $P_{(Total)}$ is the total power consumption
$P_{(short\ circuit)}$ is the short circuit power dissipation

Full Adder Power Analysis
Table 1 offers a comprehensive power analysis for the full adder circuit. Comparing Conventional CMOS and LECTOR methods, our proposed LECTOR technique demonstrated superior results in static, dynamic, and total power dissipation. This suggests its potential for optimizing power efficiency in practical applications.

Zooming in on the full adder power analysis, the findings corroborate the overarching trend observed across XNOR and XOR logic modules. When comparing the Conventional CMOS and LECTOR methods, our proposed technique consistently demonstrates superior results in static, dynamic, and total power dissipation metrics. This comprehensive assessment reaffirms the efficacy of the LECTOR technique in achieving optimal power efficiency while maintaining robust performance characteristics, positioning it as a promising solution for next-generation low-power arithmetic circuits. In summary, the results and discussion presented in the paper underscore the transformative potential of the LECTOR technique in revolutionizing the landscape of low-power circuit design. Through meticulous simulations and comparative analyses are demonstrated the tangible benefits of the proposed approach, paving the way for the adoption of energy-efficient designs in a myriad of applications ranging from portable electronics to IoT devices and beyond.

5 Conclusion

This paper addresses the growing demand for electronics products with rapid response and low power consumption. Focusing on the crucial component of arithmetic circuits, the full adder, our study explores the balance between static and dynamic logic styles for optimal energy efficiency, speed, and complexity. To achieve this, the LECTOR technique was introduced, emphasizing leakage control through the strategic placement of NMOS and PMOS transistors within logic cells. The proposed design outlines a full adder implementation using XNOR-XOR CMOS logic and pass transistor logic, integrating the LECTOR technique for enhanced power management. Through simulation and analysis in the DSCH and Microwind tool, design evaluates the static, dynamic, and total power dissipation. Our results demonstrate notable efficiency gains of 5%, 9%, and 8% in the implemented XNOR, XOR, and full adder circuits, respectively, compared to conventional methods. This research signifies a significant stride in advancing low-power VLSI design methodologies, offering promising implications for the broader field of electronic circuit optimization.

References

1. Goel, S., Kumar, A., Bayoumi, M.A.: Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **14**(12), 1309–1321 (2006)
2. Wairya, S., Nagaria, R.K., Tiwari, S.: New design methodologies for high-speed low-voltage 1 bit CMOS full adder circuits. Int. J. Comput. Technol. Appl. **2**(3), 190–198 (2011)
3. Kumar, T.S., Rao, I.R.S.N., Vinod, Y.S., Harika, P., Satyanarayana, B.V.V., Pravin, A.: Area efficient and ultra low power full adder design based on GDI technique for computing systems. In: Pareek, P., Gupta, N., Reis, M.J.C.S. (eds.) Cognitive Computing and Cyber Physical Systems. IC4S 2023. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol. 537, pp. 63–75. Springer, Cham (2023)
4. Weste, N.H., Harris, D.: CMOS VLSI design: a circuits and systems perspective, 3rd edn. Pearson Education, India (2006)
5. Kumar, C., Mishra, A.S., Sharma, V.K.: Leakage power reduction in CMOS logic circuits using stack ONOFIC technique. In: 2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS), pp. 1363–1368. IEEE (2018)
6. Rajashekhar, K., Leela, K.M.: Leakage power, current and delay analysis of stack ONOFIC Based CMOS circuits. In: 2022 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), pp. 1–6. IEEE (2022)
7. Yadav, S., Singh, K.: Performance comparison of ONOFIC and LECTOR based approaches for Leakage Power Reduction. In: 2021 Fourth International Conference on Electrical, Computer and Communication Technologies (ICECCT), pp. 1–6. IEEE (2021)
8. Mistry, T., Yadav, S.: Analysis of leakage power reduction using LECTOR and ONOFIC technique in clock gated flip-flop. In: 2022 2nd Asian Conference on Innovation in Technology (ASIANCON), pp. 1–7. IEEE (2022)
9. Hanchate, N., Ranganathan, N.: LECTOR: a technique for leakage reduction in CMOS circuits. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **12**(2), 196–205 (2004)
10. Rabaey, J.M., Chandrakasan, A., Nikolic, B.: Digital Integrated Circuits: A Design Perspective, 2nd edn. Pearson Education, India (2003)

11. Kumar, S.T., Kumar, I.G., Rao, R.S.N., Vinod, Y.S.: Design of various shaped mems based cantilevers executed in COMSOL multiphysics. Eur. J. Mol. Clin. Med. **7**(10), 1972–1979 (2020)
12. Chang, C.H., Gu, J., Zhang, M.: A review of 0.18-μm full adder performances for tree structured arithmetic circuits. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **13**(6), 686–695 (2005)
13. Parvathi, M.: High-accurate, area-efficient approximate multiplier for error-tolerant applications. In: Pant, M., Kumar Sharma, T., Arya, R., Sahana, B., Zolfagharinia, H. (eds.) Soft Computing: Theories and Applications. Advances in Intelligent Systems and Computing, vol. 1154, pp. 91–102. Springer, Singapore (2020)
14. Rao, M.V., Kumar, P.R., Balaji, T.: A high performance dual stage face detection algorithm implementation using FPGA Chip and DSP processor. J. Inf. Syst. Telecommun. (JIST) **4**(40), 241 (2022)
15. Prakash, M.D., Krsihna, B.V., Satyanarayana, B.V.V., Vignesh, N.A., Panigrahy, A.K., Ahmadsaidulu, S.: A study of an ultrasensitive label free silicon nanowire FET biosensor for cardiac troponin i detection. SILICON **14**, 5683–5690 (2022)
16. Meriga, C., Ponnuri, R.T., Satyanarayana, B.V.V., Gudivada, A.A.K., Panigrahy, A.K., Prakash, M.D.: A novel teeth junction less gate all around FET for improving electrical characteristics. SILICON **14**, 1979–1984 (2022)
17. Satyanarayana, B.V.V., Prakash, M D.: Design analysis of GOS-HEFET on lower subthreshold swing SOI. Analog Integr. Circ. Sig. Process. **109**, 683–694 (2021)
18. Ykuntam, Y.D., Penumutchi, B., Gubbala, S.: Design of speed and area efficient non linear carry select adder (NLCSLA) architecture using XOR less adder module. In: Chakravarthy, V., Bhateja, V., Flores Fuentes, W., Anguera, J., Vasavi, K.P. (eds.) Advances in Signal Processing, Embedded Systems and IoT . Lecture Notes in Electrical Engineering, vol. 992, pp. 81–91. Springer, Singapore (2023). https://doi.org/10.1007/978-981-19-8865-3_7
19. Arvapally, S., Khan, M.A., Vemula, P.C., Sonnaila, P., Chary, U.G.: FPGA implementation of industry automated bottle counter. In: 2017 International Conference of Electronics, Communication and Aerospace Technology (ICECA), vol. 2, pp. 461–465. IEEE (2017)
20. Prasad, D.D., Satyanarayana, B.V.V., Shaik, A.R., Indirapriyadarsini, K., Reddy, K.S.R., Hemalatha, M.: Full swing logic based full adder for low power applications. In: Pareek, P., Gupta, N., Reis, M.J.C.S. (eds.) Cognitive Computing and Cyber Physical Systems. IC4S 2023. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol. 537, pp 19–36. Springer, Cham (2023). https://doi.org/10.1007/978-3-031-48891-7_2
21. Satyanarayana, B.V.V., Lakshmi, B.K.S., Kumar, G.P., Srinivas, K.: LUT-based area-optimized accurate multiplier design for signal processing applications. In: Pareek, P., Gupta, N., Reis, M.J.C.S. (eds.) Cognitive Computing and Cyber Physical Systems. IC4S 2023. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol. 536, pp. 309–317. Springer, Cham (2023). https://doi.org/10.1007/978-3-031-48888-7_26
22. Wang, Y., Liang, X., Niu, S., Zhang, C., Lyu, F., Luo, Y.: FDM: fused double-multiply design for low-latency and area-and power-efficient implementation. IEEE Trans. Circ. Syst. II Express Briefs **71**(1), 450–454 (2024)
23. Farrukh, F.U.D., et al.: Power efficient tiny yolo cnn using reduced hardware resources based on booth multiplier and wallace tree adders. IEEE Open J. Circ. Syst. **1**, 76–87 (2020)
24. Vudadha, C., Srinivas, M.B.: Design of high-speed and power-efficient ternary prefix adders using CNFETs. IEEE Trans. Nanotechnol. **17**(4), 772–782 (2018)
25. Li, H., et al.: Energy-efficient power delivery system paradigms for many-core processors. IEEE Trans. Comput. Aided Des. Integr. Circ. Syst. **36**(3), 449–462 (2016)