FPGA Based Peak Cancellation for Efficient Communication Transmitters

G. Prasanna Kumar(✉), M. Pavan, M. Sobha Rani, K. V. Ganesh, M. Narasimha Rao, and N. Yoshith

Vishnu Institute of Technology, Bhimavaram, India
prasannakumar.g@vishnu.edu.in

Abstract. In communication transmitters peak cancellation (PC) is one of the essential modules. The main objective of PC is to reduce the peak-to-average power ratio (PAPR) of the message signal. FPGA implementation of PC is widely used technique because of low power and delay nature of FPGA. FIR filters are in general used as PC in communication receiver which requires higher order filter increases the usage of resources in FPGA. IIR filter with lower order one choice of using PC in communication receiver.

In this paper we proposed a new method of PC technique using lower order IIR filter. We outline the design principles for the IIR filter in the context of PC and delve into the FPGA implementation strategy, emphasizing resource optimization. The effectiveness of our proposed method is validated using the VIVADO tool. The implemented design of PC performance is compared with the standard methods. The proposed design of PC significantly reduces the delay with limited power consumption.

Keywords: Power Amplifiers (PAs) · Infinite Impulse Response (IIR) Filter · Resource Optimization · Field-Programmable Gate Array (FPGA) · Low Delay · VIVADO Simulation · Fifth Generation NR Signal · Efficiency Enhancement · Peak-to Average Power Ratio (PAPR)

1 Introduction

In the field of communication and signal processing Orthogonal Frequency Division Multiplexing (OFDM) is very important multiplexing technique and which is widely used in modern communication [1]. In OFDM signal fluctuated this is called distortion causes the efficiency reduction in power amplifiers. PAPR is the measure of efficiency of system, it is the ratio between peak power to the average power. Higher the PAPER indicates that signal having large peaks so that there is more complex to design the power amplifier and lower the PAPR reducing the distortion and flexible to design power amplifier.

FPGA implementation of communication and signal processing [2] devices are presently very important and widely used so that PAPR using FPGA implementation is effective for communication transmitters. In [3] Authors proposed Active constellation

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extension for PAPR reduction which is the begging of many PAPR reduction techniques which is mainly based on the FIR filter based PAPR reduction technique. The main advantage of this architecture is its hardware cost is low.

In [4] authors proposed peak cancellation techniques based on FPGA using IIR filter, which is the very efficient with respect to hardware utilization. In this paper mainly address the improvement of power amplifier using IIR filter instead of FIR filter. The usage of IIR filter greatly reduce the order of the filter compared to FIR filter so that overall adders and multipliers are reduced. In FPGA implementation of IIR filter we can optimize the number of adders and multipliers. In [5] authors proposed the LUT based multiplier design which is are optimized because it uses only LUT's without using DSP 48 hardware units. Generally, in FPGA DSP 48 blocks consumes more power and uses ore area. This technique has optimized technique likewise many optimization techniques are introduced in modern front end VLSI design.

In [6] authors proposed FPGA implementation of DSP application such as Fast Fourier transform. This is optimized design mainly optimizes the multiplier in FFT. In this proposed a Uniform Montgomery multiplier for twiddle factor multiplication, main advantage of this design is it has low power compared to previous designs because of its multiplier optimization. In [7] authors proposed efficient PAPR reduction scheme implemented using FPGA, which is based on the FIR filter. The main advantage of this design is low latency and finding is high power. In [8] authors proposed the VLSI back-end designs for DSP applications which are designed on back-end platform using mentor tools.

In [9, 10] authors proposed FPGA implementation of PAPR schemes with effective optimized filter designs. This technique mainly uses the optimization of resources in FPGA, hardware units in FPGA are LUT's, slice registers and DSP blocks. The applications of FPGA have involved in the field of signal and image processing. In [11, 12] authors proposed image processing techniques which can be implemented in FPGA also by using the optimization of resources of hardware. In [13–15] authors proposed digital image processing techniques of noise cancellation and segmentation, this can be also implemented in FPGA. This type of applications uses more resources in FPGA and requires high power.

In [16, 17] authors proposed OFDM implementation of clipped filtering and PAPR reduction using the clipped filtering which has many advantages compared to traditional PAPR reduction technique. Figure 1 shows the clipping and PAPR reduction using clipping. In [18] authors proposed IP core multiplier designed by Xilinx which is optimized in all aspects.

The literature of the previous existing works gives the future extension of implementation of FPGA based PAPR reduction scheme. This paper mainly focusses on the FPGA based PAPR reduction scheme for communication transmitters using IP core multiplier for efficient multiplication. The design of IIR filter is specified, highlighting optimized resource usage. Additionally, the introduced method is implemented in FPGA.

The rest of the paper organized as follows, Sect. 1 gives the introduction of the previous works and need of the work, Sect. 2 gives the IIR filter design techniques for efficient peak reduction, Sect. 3 gives the IIR filter FPGA implementation, Sect. 4 describes the simulation results of IIR filter and finally Sect. 5 gives the conclusion and future extensions of the work. The proposed work is extension of the previous existing works that is peak cancellation in the communication receiver using the IIR filter which is designed using the FPGA IP core multiplier and the ripple carry adder.

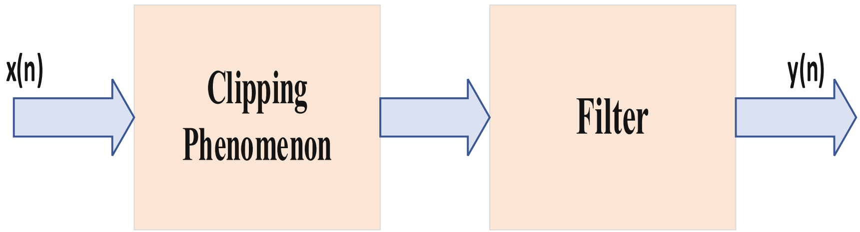

Fig. 1. The fundamental block layout of Clipping and filtering (CAF).

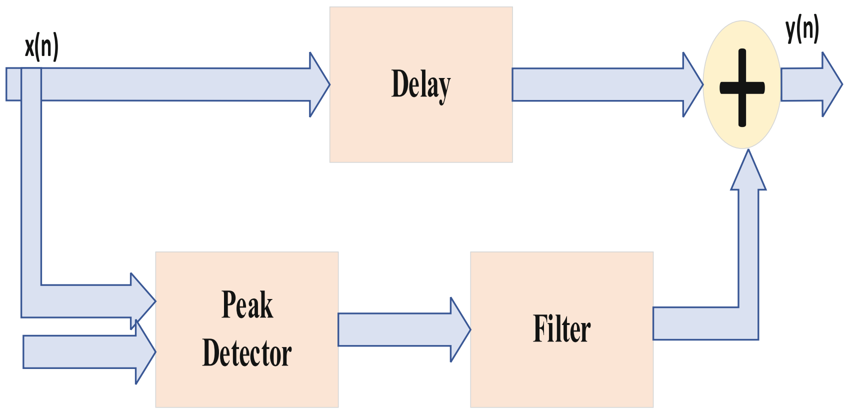

Fig. 2. The fundamental diagram peak detection and filtering.

Figure 1 shows the clipping pulse generator block diagram. In this document, we introduce the IIR-PC (Peak Cancellation with Infinite Impulse Response) method, employing a Peak Cancellation (PC) approach with an Infinite Impulse Response (IIR) filter. The design of IIR filter is specified, highlighting optimized resource usage. Additionally, the introduced method is implemented in FPGA. Figure 2 shows the fundamental block diagram of peak detection and filtering here delay is generated by d flip flop and filter is IIR filter used because of advantages of IIR filter over FIR filter.

A key advantage of IIR-PC, in comparison to previously discussed FIR-based PC techniques, is its notably reduced input-to-output delay. Beyond this, IIR-PC offers favourable PC performance and minimizes resource consumption.

2 Proposed Methodology

The propose method of PC cancellation is shown in Fig. 3, which consists of delay unit peak detector and IIR filter. The important modification in this proposed method for peak cancellation is using IIR filter and optimization of IIR filter design using FPGA core multiplier and ripple carry adder for addition.

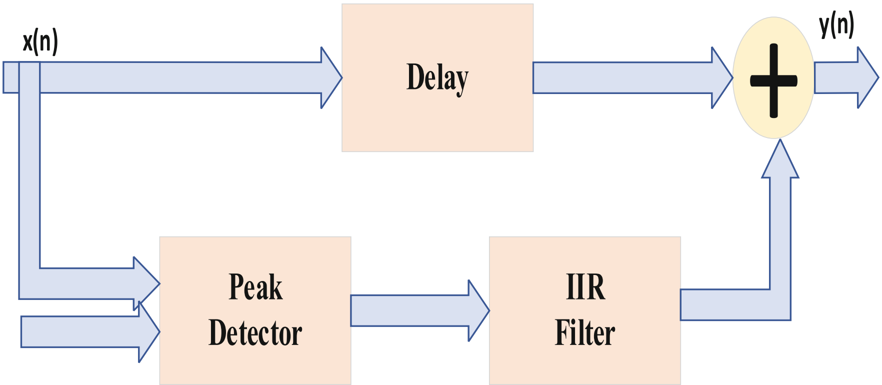

Fig. 3. Block diagram of Proposed method for PC

IIR filters are distinguished by feedback loops in their filter structure, which can lead to a more efficient implementation than FIR filters in certain applications. However, they are more prone to stability difficulties, particularly if not well constructed.

One popular application for IIR filters is audio processing, where they are utilized for tasks such as equalization, filtering and noise reduction. They are also utilized in control systems, communications systems, and a wide range of other digital signal processing applications.

The Direct Form II (DF-II) realization of an Infinite Impulse Response (IIR) filter is a common implementation structure in digital signal processing. In DF-II, the filter is represented as a cascade of second-order sections, which makes it computationally efficient and numerically stable. Here's how the DF-II structure is typically formulated: Fig. 4 shows the D-II realization of IIR filter in which z-1 represents the delay and adders are used for the design of IIR filter. The main advantages of D-II realization is it uses less hardware compared to D-I realization.

3 FPGA Implementation of IIR Filter

Implementing signal processing algorithms on an FPGA requires a good understanding of both digital signal processing and FPGA design principles. It can be a challenging but rewarding task. Additionally, utilizing high-level synthesis (HLS) tools like Vivado HLS or Intel HLS can help accelerate the development process.

Implementing an IIR (Infinite Impulse Response) filter on an FPGA involves translating the filter algorithm into hardware description language (HDL) like Verilog or

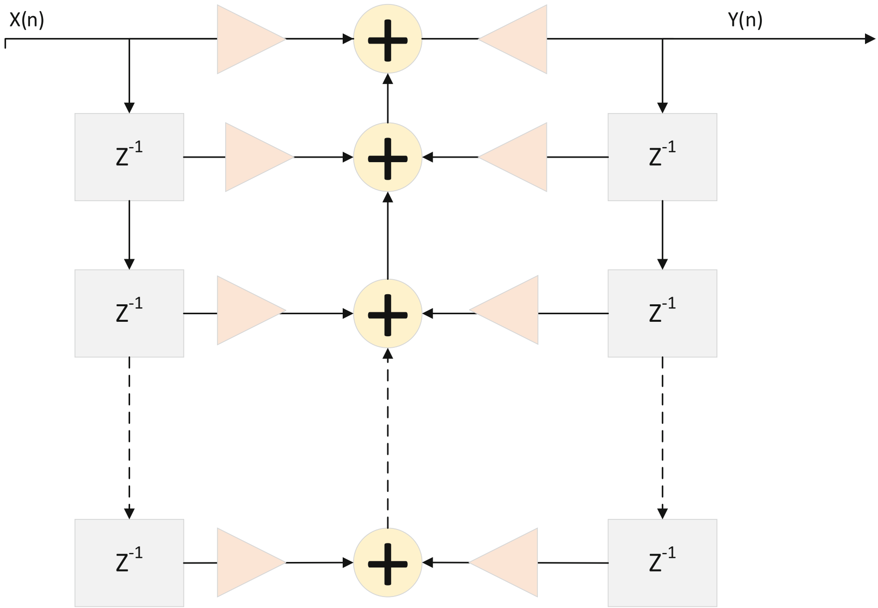

Fig. 4. D-II realization of IIR filter

VHDL, and then synthesizing it for the FPGA hardware. Here's a basic overview of how you might approach it. Decide on the type of IIR filter you want to implement.

Specify the filter parameters such as cutoff frequency, filter order, and pass-band/stopband ripple and MATLAB is used to design the filter coefficients. You'll obtain coefficients for the numerator and denominator polynomials of the IIR filter transfer function.

Write HDL code (Verilog or VHDL) to implement the IIR filter algorithm. Break down the algorithm into smaller modules such as multiplier, adder, delay line, and feedback loop.

Use fixed-point arithmetic if floating-point operations are too resource-intensive for your FPGA. Simulate the HDL code using simulation tools like Model Sim or Xilinx VIVADO Simulator. Verify that the filter behaves as expected and meets the design specifications. Debug any issues that arise during simulation. Use FPGA synthesis tools such as Xilinx VIVADO or Intel Quartus Prime to synthesize the HDL code. Map the synthesized design to the FPGA's resources and optimize for timing, area, and power consumption. Generate the programming file (bitstream) for the FPGA. Load the generated bitstream onto the FPGA development board.

Interface the FPGA with input and output devices that is Analog-to-digital converter (ADC) for input, digital-to-Analog converter (DAC) for output). Test the filter with real-world input signals and verify its performance. If necessary, optimize the design for performance, resource utilization, and power consumption. Consider techniques like pipelining, parallel processing, or hardware/software co-design to improve efficiency. Integrate the FPGA-based IIR filter into your larger system or application. Ensure proper interfacing and communication with other components. Deploy the system in its target environment and validate its functionality.

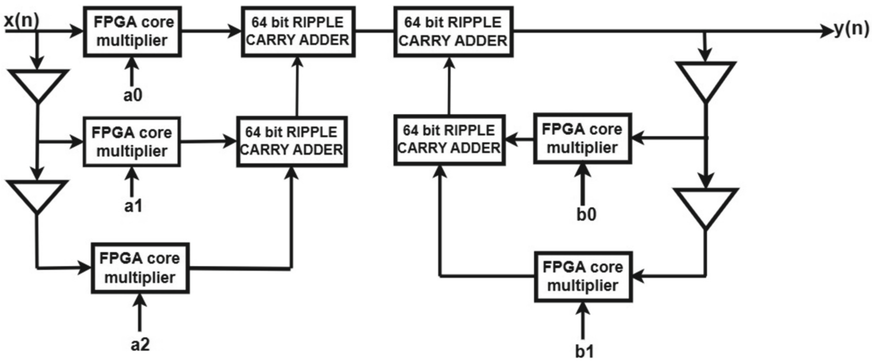

Fig. 5. FPGA design of D-II Diagram IIR Filter

Figure 5 shows the implementation of IIR filter. The multiplier in this design is FPGA core multiplier and adder used as 64-bit ripple carry adder. The implementation of proposed method consists of two stages one is MATLAB implementation for coefficients and FPGA design using the constant coefficients and multipliers and adders. The MATLAB based coefficient design using FDA Tool is shown in Fig. 6, which is Chebyshev type1 filter. The FPGA implementation of IIR filter schematic diagram is shown in Fig. 7.

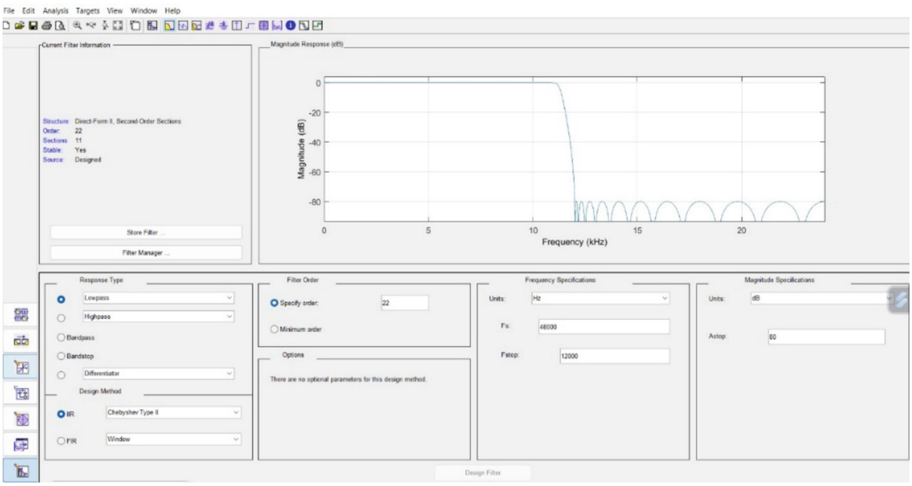

Fig. 6. IIR Filter Design using MATLAB FDA Tool.

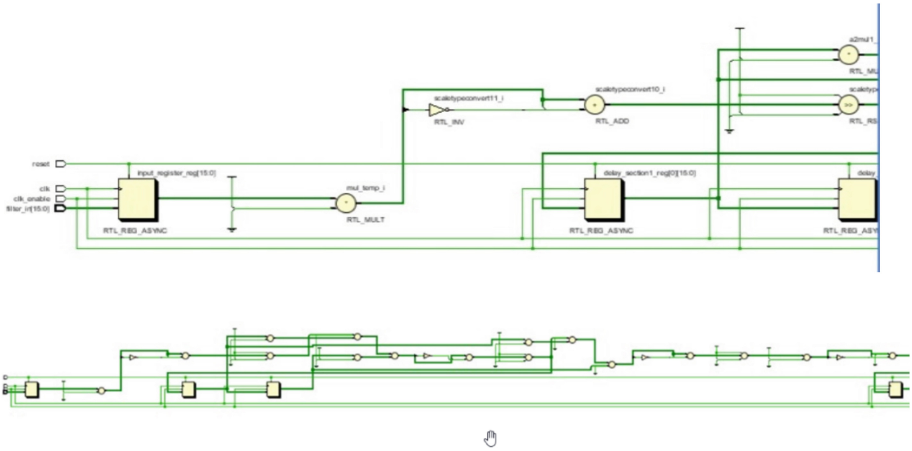

Fig. 7. Schematic diagram of implemented design.

4 Simulation Results

The simulation of the work has been done in Xilinx VIVADO tool which is a comprehensive development environment for FPGA design and verification. It's widely used for designing, synthesizing, implementing, and debugging FPGA-based systems. Here's an overview of the key features and steps involved in using VIVADO for FPGA development. Figure 8 shows the simulation result of IIR filter, in which, 'clk' is the clock signal "filter out" is the output of the filter.

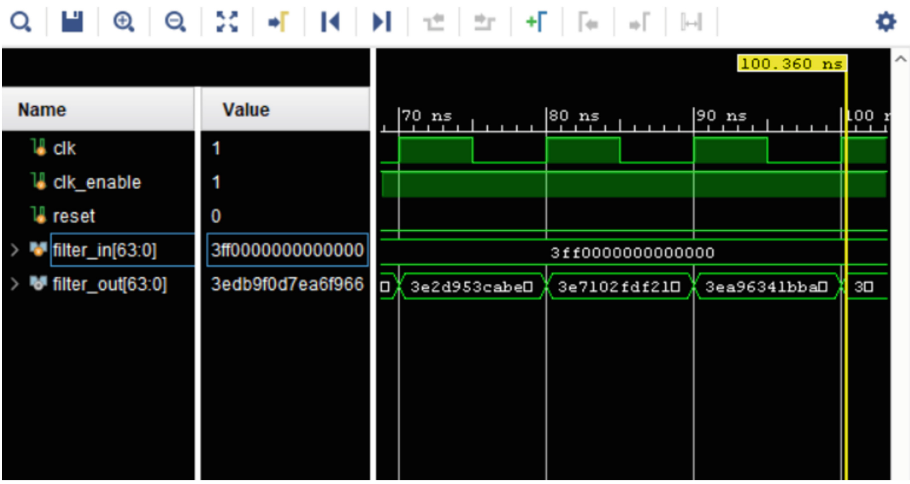

Fig. 8. Simulation result of IIR.

Table 1 provides the resource use and time delay for each strategy. The suggested methods' resource consumptions are similar to those of the clipping pulse generation but their delays in between the input and the output are significantly shorter. From the Table 1 the flipflops, LUTs and DSPs used by proposed method is slightly increased when compared to the previous methods. The proposed 64-bit IIR PC implementation appears to have the high resource utilization and power consumption but the delay is greatly decreased among the listed designs.

Table 1. Representation of resource consumption.

	LUT	FF	DSP48	Power(w)	Delay(ns)
[11]64-bit	986	245	42	0.95	385
[19]64-bit	1065	324	50	0.99	487
[20]32-bit	558	154	24	0.66	254
Proposed 64-bit IIR PC	1296	384	56	1.25	174

5 Conclusion

This brief describes a PC method for reducing PAPR using an IIR filter. The FPGA implementation technique and IIR filter design requirements are explained. The experiment's findings demonstrate that the suggested approach can significantly lower the PC's input-to-output latency. The proposed design of PC using FPGA core multiplier and Ripple carry adder greatly reduce the delay with additional consumption of small resources. The power of the proposed design is little high compared to existing results.

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