Suspended-Gate FET as a sleep transistor for ultra-low stand-by power applications

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Introduction: Increased interest in hybrid Micro-Electro-Mechanical-Solid-State devices like Suspended-Gate FETs (SGFETs, Fig.1) has been shown recently thanks to their potential for low-power applications, especially as memory cells [1,2]. In principle, the device takes advantage of the movable gate, suspended over the transistor's channel, to obtain very abrupt switching of the FET along with two different voltages for turning the device "on" and "off". Once the gate is at the "up" position the transistor is "off" presenting an extremely low current. Increasing the gate bias V_G the gate moves towards the channel and at the "on" voltage it snaps onto the gate oxide driving the SGFET above its threshold providing very high current. The design and the optimization of this kind of device is a considerable challenge due to the lack of dedicated tools for MEMS-Solid-State analysis and numerical simulation. The purpose of this work is to present an original method of coupling state-of-the-art finite element analysis (FEA) tools in a self-consistent way and generate data for SGFET operation. These data are then used for the validation of an analytical model, which is implemented in a circuit simulator to demonstrate the concept of the SGFET as an ultra-low-off-current sleep transistor in advanced CMOS architectures.

Hybrid FEA: Numerical simulation of a SGFET requires a solver capable of handling the electrostatics and semiconductor physics along with the structural domain. As a solution to that, we propose the coupling of two different FEA tools, ANSYS Multiphysics and ISE-DESSIS originally bound together in a self-consistent system. ANSYS is used for the electromechanical solution while DESSIS provides the correct boundary conditions for the electrostatic domain taking account of semiconductor physics. In Fig.2 the procedure of the analysis is presented in a flowchart for a V_G loop. The advantage of using a separate FEA tool for semiconductors is that one can easily add physics models of more complicated phenomena, e.g. tunneling. To our best knowledge there is no such tool available for electromechanically actuated semiconductor devices. The original "binding" of the two (initially incompatible) simulators is programmed using a Perl script. The first step in the loop is performed by ANSYS in order to generate the 2D geometry of the problem, which is then passed to DESSIS that resolves the problem with the proper Dirichlet boundary conditions (bulk, source, drain and gate biases) for the initial ("up") position of the suspended-gate. After the DESSIS solution has converged, all the resulting boundary conditions are sent back to ANSYS for the electromechanical analysis to provide the new geometry. The latter is reintroduced to DESSIS for a new iteration and eventually the loop is terminated once the convergence criterion is satisfied. A sequence of loops is used to build the complete I_D curve of a SGFET with automatic detection of pull-in and pull-out (Fig.5, Fig.3) and taking into consideration the roughness effect after pull-in for the contact between the gate electrode and the oxide.

SGFET Compact Model: The modeling strategy for SGFET shown in Fig.4, is based on charge based EKV formalism [3,4]. The SGFET can be considered as a capacitive divider between C_{gap} and C_{gg} as shown in Fig. 6 providing potential at the internal node (V_{int}) expressed in Eq.(1) of Fig.4., where C_{gap} and C_{gg} are the capacitance of the gap and input capacitance of MOS, respectively. The $C_{gap} = \frac{\epsilon_0 W_{beam} L_{beam}}{t_{gap0} - \Delta_y}$ is the capacitance of the gap. The displacement of the beam Δ_y is obtained by balancing the electrical and mechanical forces on the beam as shown in Eq.(2). Eq. (1) and (2) are solved together for both V_{int} and Δ_y. The solution of these coupled equation is valid only for $V_G - V_{int} < V_{PI}$, where V_{PI} is the pull-in voltage for ideal two plate case. Imposing this condition, the modified internal node potential (V_{int}^{PI}) is obtained in Eq. (3). Similarly, the internal node potential for the pull-out case (V_{int}^{PO}) is obtained in Eq. (4). Now as we know the internal node potential for both pull-in and pull-out cases, we use standard EKV formalism to derive the C_{gg} and finally, drain current (I_{DS}) for both cases. The drift-diffusion current expression shown in Eq. (5), is first normalized and then integrated from source to drain as shown in Eq. (7) and (8). Note that q, i_{ds}, δ_{sat}, ρ_v and, ξ are all dimensionless quantities. The final expression of current including velocity saturation is expressed in Eq.(9). The C_{gg} shown in Eq.(12) is obtained using total inversion charge density from Eq.(11). In fig.7 the validation of the model on FEA data is presented.

Optimization of SGFET as sleep transistor: Analytical modeling and FEA are exploited for optimization of a SGFET in order to build a high performance low-leakage sleep transistor. As the model has been validated on n- and p-type SGFETs both header and footer configurations could be used for the device (Fig.8). In Fig.9 the fine-tuning of the transfer characteristic is presented with the gap as the parameter. The simulated device has a channel length of 90nm and for 17nm of gap and with $k_{beam} = 3.9N/m$ a $V_{PI} \simeq 1.2V$ is achieved, compliant to 90nm ITRS. In Fig.7 one can observe that due to the electromechanical hysteresis of the SGFET and of the carefully chosen pull-out voltage V_{PO} ($>> 0$) a very low off-current I_{off} can be obtained up to 5 decades lower than the ITRS I_{off} ($\simeq 10^{-10}A/\mu m$) for the 90nm node. This is a major advantage for building highly efficient low-leakage sleep transistors. Based on the analytical model the output characteristic $I_D(V_D)$ is generated as a function of V_G showing the abrupt switching of the device (Fig.10). The influence of the gate material workfunction Ψ_m on the electric characteristics has also been investigated showing an increase of V_{PI} with Ψ_m (Fig.11). Dynamic analysis based on the analytical model has been performed for various optimized devices demonstrating that with proper design the response of a SGFET could be extended in the range of 100s of MHz rendering it suitable for power management (Fig.12). This study has brought us to the conclusion that the phase and the frequency f_0 of the logic signal play a major role and that the maximum operation frequency for the SGFET as a power switch is $f_{max} = f_0/4$. The role of the mechanical damping of the movable gate has also been studied showing that damping could be favorable for proper operation (Fig.13).

Conclusion: A novel FEA for MEMS-solid-state devices has been proposed. Data of this analysis have been used to develop and validate an analytical model for SGFET. Both the model and FEA have been used to optimize a 90nm SGFET for low-leakage power management applications investigating both the its static and dynamic behavior and demonstrating that such a device is a good candidate for building ultra-low off-current sleep transistors.

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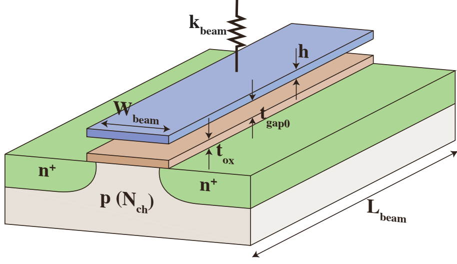

Fig. 1. Three dimensional representation of suspended-gate field-effect transistor (SGFET).

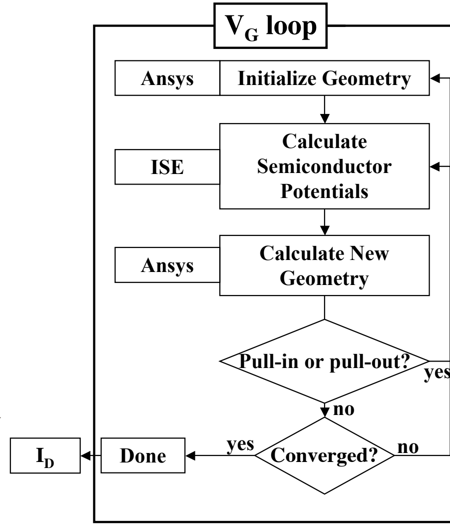

Fig. 2. Flowchart of the procedure followed during one V_G iteration by coupling ANSYS and DESSIS in a self consistent electromechanical system for finite element analysis of SGFET. At the end of each iteration outputs like the drain current I_D, V_{int}, vertical displacement of the gate and the surface potential ψ_s are generated for feeding with data the analytical model and validate it.

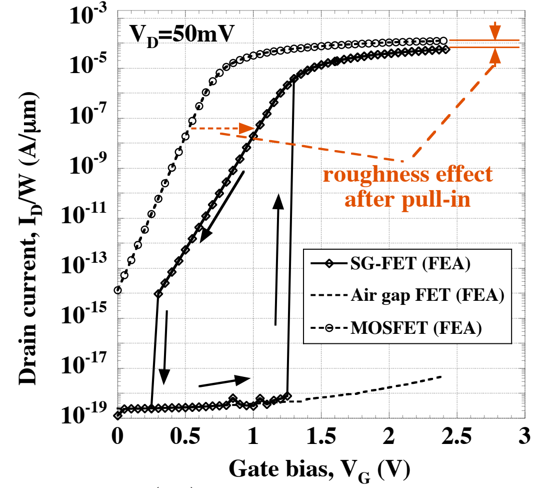

Fig. 3. $I_D(V_G)$ characteristic of an optimized SGFET for power switching application obtained by the proposed hybrid FEA using ANSYS and DESSIS software coupling. The SGFET characteristic is compared to that of a "normal" MOSFET showing the shifting of the threshold voltage and the lower maximum current due to the roughness effect at pull-in. V_{PI} is fine tuned to be around 1.2V and V_{PO} to be as close as possible to it and much higher than 0.

Potential at the internal node (oxide surface): $V_{int} = V_G \frac{C_{gap}}{C_{gap}+C_{gg}}$ (1)

Displacement of the beam Δ_y by balancing electrical and mechanical forces: $\frac{1}{2}\epsilon_0 W_{beam} L_{beam} \left(\frac{V_G - V_{int}}{t_{gap0}-\Delta_y}\right)^2 = k_{beam}\Delta_y$ (2)

V_{int} for pull-in case by solving (1) and (2): $V_{int}^{PI} = \begin{cases} V_{int}, & \text{if } V_G < V_{int} + V_{PI} \\ V_G, & \text{otherwise.} \end{cases}, \quad V_{PI} = \sqrt{\frac{8k_{beam}}{27\epsilon_0 W_{beam} L_{beam}} t_{gap0}^3}$ (3)

V_{int} for the pull-out case: $V_{int}^{PO} = \begin{cases} V_{int}, & \text{if } V_G < V_{PO} \\ V_G, & \text{otherwise.} \end{cases}, \quad V_{PO} = \sqrt{\frac{2WLk_{beam}t_{gap0}\epsilon_0}{C_{gg}^2}}$ (4)

Drift-diffusion current using first order mobility model: $I_{DS} = \frac{\mu_v}{1+\frac{\mu_v}{v_{sat}}\left|\frac{d\Psi_s}{dx}\right|} W \left(-Q_i \frac{d\Psi_s}{dx} + U_T \frac{dQ_i}{dx}\right)$ (5)

Using inversion charge linearization relation $(-Q_i = n_q C_{total}(\Psi_P - \Psi_S))$, Eq. (6) is rewritten as: $\frac{dq}{d\xi} = -\frac{i_{ds}}{\rho_v(1+2q-\delta_{sat} i_{ds})}$ (6)

where variables are normalized as: $q = \frac{-Q_i}{2n_q C_{total} U_T}, i_{ds} = \frac{I_{DS}}{2n_q \frac{W}{L}\mu_0 C_{total} U_T^2}, \delta_{sat} = \frac{2\mu_0 U_T}{v_{sat} L}, \xi = \frac{x}{L}$ (7)

Normalized i_{ds} by integrating (6) along the channel ($\xi = 0$ to $\xi = 1$): $i_{ds} = \frac{\rho_v}{1+\rho_v\delta_{sat}(q_s-q_d)}\left[\left(q_s^2+q_s\right) - \left(q_d^2+q_d\right)\right]$ (8)

From (8), i_{ds} including velocity saturation: $i_{ds} = \begin{cases} \frac{\rho_v}{1+\rho_v\delta_{sat}(q_s-q_d)}\left[\left(q_s^2+q_s\right) - \left(q_d^2+q_d\right)\right], & \text{if } q_d > q_{dsat}; \\ \frac{\rho_v}{1+\rho_v\delta_{sat}(q_s-q_{dsat})}\left[\left(q_s^2+q_s\right) - \left(q_{dsat}^2+q_{dsat}\right)\right], & \text{otherwise} \end{cases}$ (9)

where $q_{dsat} = \left(\frac{1}{2} + q_s + \frac{1}{\rho_v\delta_{sat}}\right) - \sqrt{\left(\frac{1}{2} + \frac{1}{\rho_v\delta_{sat}}\right)^2 + \frac{1}{\rho_v\delta_{sat}}(2q_s+1)}$ (10)

Normalized total inversion charge density q_c from (6): $q_c = \frac{1}{2}\left\{q_s + q_d + \frac{1}{3}\frac{(q_s-q_d)^2}{(1+q_s+q_d)}[1+\rho_v\delta_{sat}(q_s-q_d)]\right\}$ (11)

Normalized C_{gg} using (11): $C_{gg} = \left\{1 - \frac{1}{n_q} + a_2 + \frac{1}{3}\frac{\left(2a_1+3\rho_v\delta_{sat}a_1^2\right)[d_{qs}-d_{qd}]}{1+q_s+q_d} - \frac{1}{3}\frac{\{\left[a_1^2+\rho_v\delta_{sat}a_1^3\right]a_2}{(1+q_s+q_d)^2}\right\}$ (12)

where $d_{qs} = \frac{(1/n_q)}{2+(1/q_s)}, d_{qd} = \frac{(1/n_q)}{2+(1/q_d)}, a_1 = q_s - q_d, a_2 = d_{qs} + d_{qd}$ (13)

Fig. 4. Derivation of the new compact model for Suspended Gate FET. Symbols used: W and L- channel width and length, W_{beam} and L_{beam}- width and length of the beam, Ψ_S-surface potential, Ψ_P-pinch-off surface potential [3,4], n_q-slope factor [3,4], U_T-thermal voltage, v_{sat}-saturation velocity, μ_0 and $\mu_v(=\rho_v\mu_0)$- low field and vertical field dependent mobility respectively, Q_i-inversion charge, q_d and q_s-normalized drain and source charge densities respectively [3,4], C_{gg}-gate to gate capacitance of MOS, t_{gap0}-initial gap of beam, k_{beam}-spring constant of the beam, V_{PO}-pull-out voltage of SGFET. Note that, for dynamic simulation (results shown in Fig 12 and Fig 13), RHS of Eq.(2) should be replaced by ODE of Δ_y (i.e. $m\frac{d^2\Delta_y}{dt^2} + b\frac{d\Delta_y}{dt} + k_{beam}\Delta_y$).

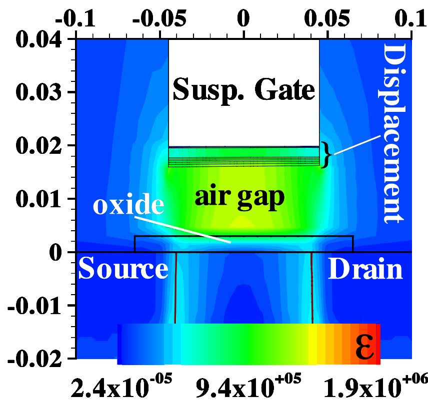

Fig. 5. FEA result in the DESSIS environment showing the displacement of the movable gate with increasing electric field (V/cm). A slight tilt of the gate can be observed due to the asymmetrical attraction from the source and drain regions.

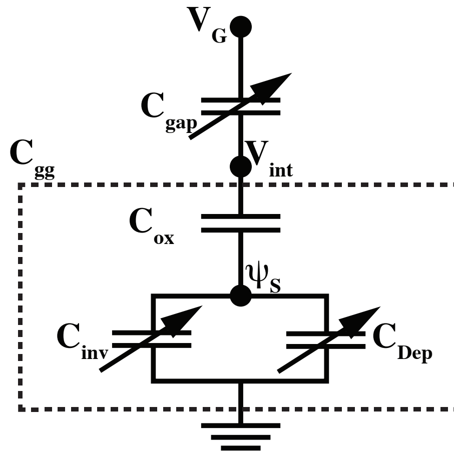

Fig. 6. Schematic of the electrical model for SGFET. Inside the dotted rectangle is the standard model of a MOSFET. Above it is the electromechanical model of the movable gate represented by varying capacitor C_{gap}.

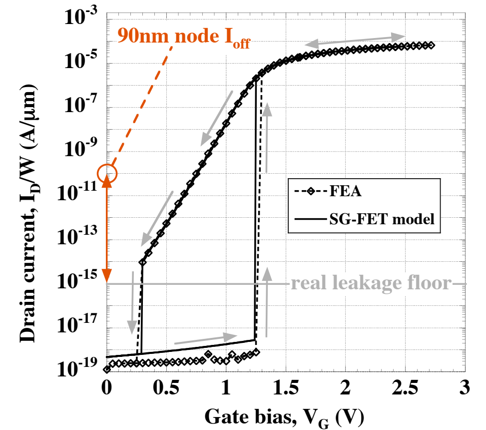

Fig. 7. Validation of the analytical model on the data generated by the hybrid FEA. The model reproduces with very good accuracy the numerical simulation. On the same graph one can notice the significant gain in off-current compared to a standard 90nm node I_{off} by carefully designing the electromechanical characteristics of the SGFET. Design characteristics: $k_{beam} = 3.9N/m$, $t_{ox} = 3nm$, $t_{gap0} = 17nm$, Ψ_m=4.4eV, channel doping $N_{ch} = 1 \times 10^{18} cm^{-3}$.

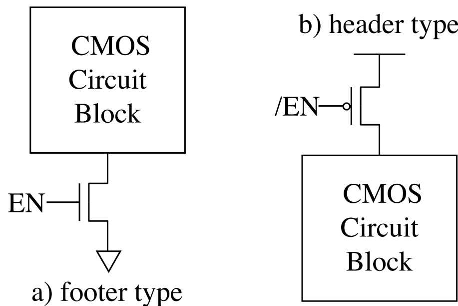

Fig. 8. Different configurations for sleep transistors: (a) footer configuration with n-type SGFET, (b) header configuration with p-type SGFET.

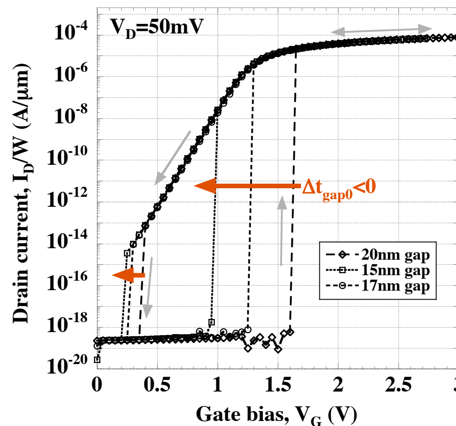

Fig. 9. Fine-tuning of the gap showing the dependence of V_{PI} and V_{PO} on t_{gap0}. In any case the I_{off} stays below the 90nm ITRS node specifications for the off-current (shown in Fig 7).

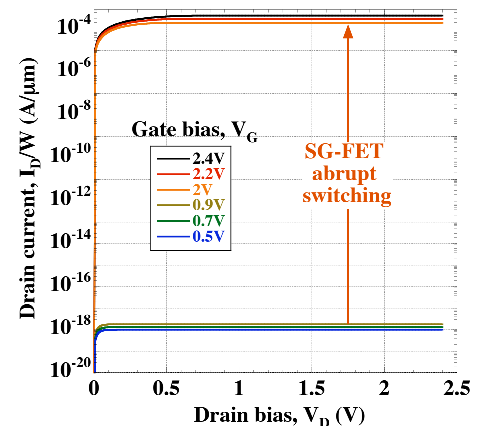

Fig. 10. Output characteristic of the SGFET shown in Fig 7 generated using the analytical model. The abrupt switching of the device is observed with over ten orders of magnitude of difference between I_{on} and I_{off}.

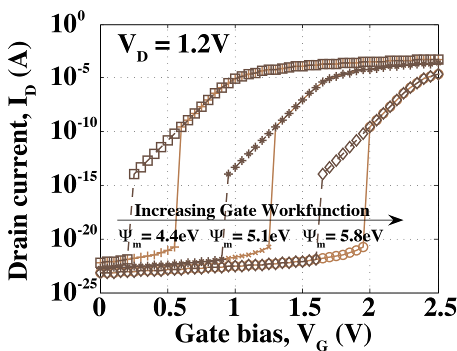

Fig. 11. Study of the role of the gate workfunction on the electromechanical characteristics of a SGFET using the analytical model. It is obvious that Ψ_m plays a significant role when it comes to nanoscale SGFETs.

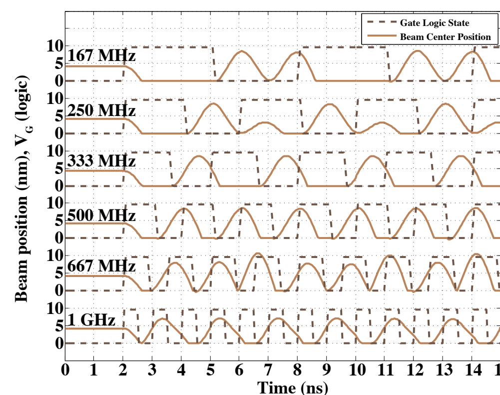

Fig. 12. Response of the same device as in Fig 13 for different frequencies. Successful switching is possible even at the mechanical resonance frequency of the SGFET, although the proper operation is a function of the phase and frequency between the logic signal and the vibrating SGFET. If the device should be on at least for half the time the logic signal is high, then the maximum operation frequency of the SGFEt is four times smaller then that of the logic signal.

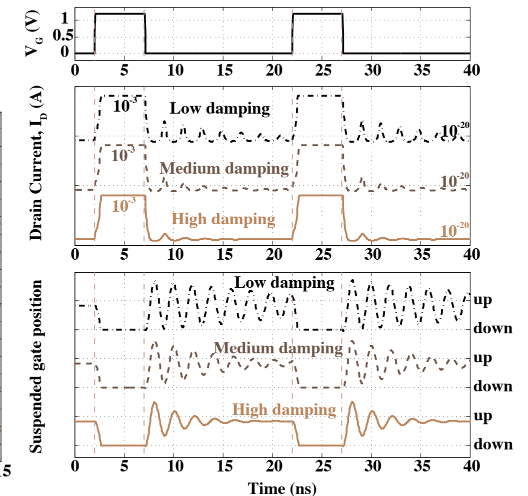

Fig. 13. Transient response of a SGFET to a logic signal applied to the movable gate. The gap assumed in this case is 5nm and damping has been added to the mechanical model of the movable gate in order to investigate its impact on the dynamic behavior of SGFET. With high damping (quality factor =20) the devices follows well the applied signal.