Design of Virtual Simulation Experiment Teaching System for Electrical Engineering and Automation Specialty

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Abstract. In order to improve the real-time interaction of virtual simulation experiment teaching system for electrical engineering and automation specialty, an experiment teaching system is designed. Through the selection of arm devices, USB interface design, hardware design of oscilloscope module and controller design, the hardware design of the system is realized. In the software part of the system, the virtual simulation transformation is designed, so as to complete the research on the virtual simulation experiment teaching system of electrical engineering and automation specialty. The experimental results show that the teaching system in this study has better real-time interaction, lower packet loss rate and strong practical significance than the traditional system.

Keywords: Electrical engineering · Virtual simulation · Oscilloscope

1 Introduction

Electrical engineering and automation are undergraduate majors in general colleges and universities, and belong to electrical majors. Electrical engineering is mainly a discipline that studies the generation, transmission, conversion, control, storage and utilization of electrical energy. This major belongs to the electrical category. It cultivates the basic theory, professional skills and practical ability related to the field of electrical engineering. It can be engaged in the design, research and development and operation of equipment manufacturing, system operation, and technology development.

With the continuous development of China's economy and the continuous development of modern industries, the electric automation technology talent market has huge potential. Especially in Guangdong, the continuous improvement of automated production technology, the continuous popularization of automation products, the application of smart buildings and smart homes, and the continuous development of smart transportation provide broad development prospects for electrical automation technology. In the professional learning process, theoretical knowledge alone is not enough. Therefore, a virtual simulation experiment teaching system of electrical engineering and its automation is designed to improve the learning effect of students.

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In order to vividly reproduce the operation process and operating status of various links in the electric power industry, let students understand the operation of electric power engineering, virtual simulation has become an important means of experimental teaching of electrical engineering, and it is the development direction of experimental teaching of electrical engineering in various colleges and universities today. The construction of the domestic electrical engineering virtual laboratory started late, but it has developed very rapidly. Tianjin University has established an electrical automation virtual simulation experiment teaching center, introducing simulation and semi-physical real-time simulation technology, and has the design and simulation capabilities of multi-source distributed power generation, energy storage, intelligent power distribution and energy management such as wind, light, and ocean energy. Northeast Dianli University has established a virtual simulation experiment teaching center for the production process of the electric power industry, which can simulate subcritical to ultra-supercritical domestic units, can simulate the power production process of nuclear power plants, and the power transmission and distribution process of 35–500 kV substations. In addition, other colleges and universities have also established electrical engineering virtual simulation laboratories. For example, Xi'an Jiaotong University has established a nuclear power plant and thermal power plant system virtual simulation experiment teaching center, the electrical engineering and automation virtual simulation experiment teaching center of Nanjing University of Science and Technology, and the transmission line engineering experiment teaching center of the Three Gorges University.

2 Teaching System Hardware Design

2.1 ARM Device Selection

The ARM workflow is as follows: After the data acquisition card is powered on, the program in the Flash is first loaded into the SDRAM designated program running space to run. The first operations to be completed after the ARM program runs are:

Reset Stop Counter:
Reset the chip ax88180 and 88e111l; set the IP address of the lower computer according to the position of the dial switch; initialize the network interface, and then wait to receive the ARP data packet from the upper computer, according to the received ARP data packet with the MAC address and IP address of the new lower computer, and then send the ARP packet to the upper computer, and inform the lower computer of the MAC address, so as to establish contact with the upper computer Communication; configure the I/O status of the board (8-way input and 10-way output), configure the pin function [1, 2]; set the corresponding memory interval configuration of FPGA and corresponding I/O port configuration; configure interrupt, f'pga output interrupt signal uses external interrupt 1. After initialization and configuration, arm enters the user mode, executes the program main cycle, and enters the working state. The work flow chart is shown in figure below (Fig. 1).

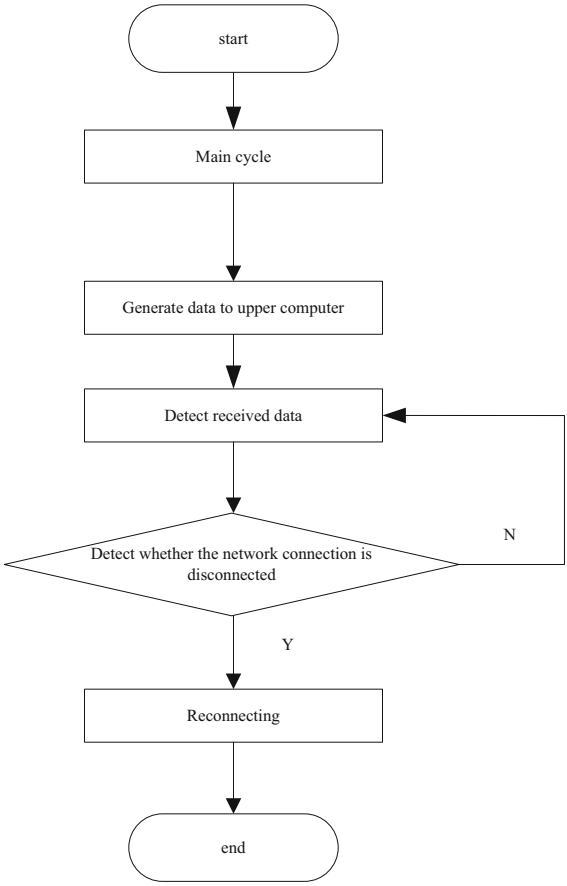

Fig. 1. Arm work flow chart

2.2 Design of USB Interface

Considering factors such as development cost, development cycle and chip purchase, we chose Cypress's CY7C64613. This chip is the second-generation product of Cypress, which supports full-speed transmission and is compatible with USBl. Version 1 and USB2.0 version (full-speed device). This chip integrates considerable resources [3], which is conducive to hardware expansion and development of various target devices. CY7C64613 is the second-generation product of Cypress, which supports USB full-speed transmission. Compared with the first-generation products, CY7C64613 has stronger performance and higher integration. It inherits the advantages of the first generation, integrating smart USB core, enhanced 8051 core, 8-Kbyte RAM and high-performance I/O on the chip, and at the same time further improves the execution speed and provides more expansion resources on this basis.

Features of CY7C64613:

1. Integrated USB transceiver, Sie (serial interface engine) and enhanced 8051 microprocessor;
2. Compatible with USB specification 1.1 and 2.0 (full speed device);
3. Software: 8051 runs code from internal or external RAM. The code can be downloaded through USB cable, loaded from EEPROM and run in external memory, such as flash;
4. Many endpoints and caches: 14 blocks, interrupt endpoints, each of which can transmit a frame of up to 64 bytes and 16 isochronal endpoints. Meanwhile, 2 KB cache can be shared by these 16 endpoints and one control endpoint, which is bidirectional;
5. Standard 8051 core with enhanced performance: each instruction cycle is 4 clock cycles [4], the clock frequency is 48 MHz or 24 MHz, determined by the configuration in the EEPROM, two asynchronous serial ports UARTS, three counters/timers, extended interrupt system, two data pointers, the general 8051 has only one DPTR;
6. Working at 3.3 V, more power saving;
7. Extended interrupt system to serve USB, FIFO and DMA interrupt events;
8. Support 12C bus; the working speed of 12C bus is 400 kHz or 100 kHz;
9. External memory expansion.

2.3 Hardware Design of Oscilloscope Module

Demand analysis, with two identical signal channels, these two channels can work independently; the amplitude of the input signal is 100–40 V, the bandwidth is 1 MHz; the DC level of the signal under test can be adjusted; multiple trigger sources are required, such as Clock trigger, internal trigger, external trigger, etc.; multiple trigger methods are required [5, 6], such as preset trigger, delayed trigger, synchronous trigger.

The oscilloscope module has two independent signal channels. When the measured signal is sent to the signal channel, the MCU writes the appropriate channel parameters, so as to adjust the measured signal to the level range suitable for ADC acquisition and send it to ADC for acquisition [7, 8]. At this time, MCU writes initialization parameters to the acquisition control logic, and then starts an acquisition. The next acquisition process is managed by the acquisition control logic. After a/D conversion, the measured signal becomes digital information and is stored in RAM. When the acquisition is finished, the control logic informs MCU that the acquisition is finished. At this time, the computer can read these digital information through the USB interface and process and display them. The function of MCU is to respond to the USB interrupt, move the data in RAM to the predetermined endpoint register, and then put the acquisition control logic in the initial state again, and start the next acquisition.

On this basis, for the signal channel design, this oscilloscope contains two signal channels CHI and CH2, these two signal channels are exactly the same, so this section only introduces channel CH1. The signal channel CH1 is composed of high-impedance attenuator, three-stage amplifying circuit and DC level generating circuit. Below we will introduce each part of the signal channel in detail.

High-impedance attenuator, the measuring range of the oscilloscope is limited, especially the digital oscilloscope, it uses the AD converter [9, 10], the input signal requirement of the AD converter that we choose is Vpp is 1 V. Therefore, the input of the first stage amplifier and the amplification factor of the amplifier must be limited. The maximum input amplitude of the oscilloscope designed this time is 40 V, and the minimum amplitude is 100 my, so the signal must be amplified or attenuated during the signal conditioning process. Two sets of attenuators are designed in the circuit to attenuate when the signal is too large, and when the signal is small, the signal passes through.

In the circuit of digital oscilloscope, the three processes of digitizing analog quantity, sampling, quantization and coding, are completed by a/D converter. An analog-to-digital converter converts an unknown continuous analog signal [11–13] (usually voltage) into a discrete digital signal for further processing, display, recording and transmission. It is the core of digital oscilloscope, which determines the storage bandwidth and resolution of oscilloscope. In digital oscilloscope, data acquisition and storage of broadband signal are involved. High speed data acquisition technology is the key technology of broadband analog signal data acquisition.

A/D converters, with the rapid development of VLSI technology and the widespread use of computer technology in the industrial field, new design ideas and manufacturing technologies for A/D converters emerge in endlessly. In order to meet the needs of various detection and control tasks, a large number of A/D conversion circuits with different structures and performances have emerged. The ADC used in this design is a chip of Analog Devices-AD9288. AD9288 is an 8-bit dual-channel monolithic integrated analog-to-digital converter with sample-and-hold circuits. It has the characteristics of low power consumption, small size, good dynamic characteristics and easy to use.

2.4 Controller Design

In addition to the interrupt signal, the interface of the SPI controller is mainly composed of the APB signal and the SPI signal. The two sets of signals are introduced below. The SPI controller provides an SPI bus to connect to the SPI device, and on the module [14–16], it is necessary to design more interface signals than the SPI bus protocol requires to meet the needs of the SPI controller configurable to work in different modes. The description of each interface signal is shown in the following table (Table 1):

Table 1. Signal description of SPI controller

Pin name	Direction	Function description
pclk	Input	Bus clock
present	Input	Global reset signal
penable	Input	The transmission enable signal can represent the second cycle of an APB transmission, and its rising edge appears in the middle of the APB transmission

(*continued*)

Table 1. (*continued*)

Pin name	Direction	Function description
psel	Input	Select the signal from the device. When the signal is high, it indicates that the current transmission is aimed at the SPI controller, and the controller needs to make the correct response
paddr	Input	Address bus signal to locate the register of the current operation
pwrite	Input	For the signal of transmission read-write type, when the level is high, it means~times of APB write access, and when the level is low, it means one time of APB read access
pwdata	Input	Write data bus signal received by SPI controller
prdata	Output	Read data bus signal of SPI controller response
spijxejntr	Output	Send FIFO air break request, when the data to be sent in transmit FIFO is equal to
spijxojntr	Output	Or less than the set threshold
spi—rxLintr	Output	The transmit flf0 overflow interrupt is generated when data is written to the full transmit FIFO
spLrxu—Intr	Output	The receive FIFO full interrupt is generated when the data received in the receive FIFO is greater than or equal to the set threshold
SS-l	Input	Receive fjfo underflow interrupt is generated when receive FIFO is empty and the FIFO is read

The specific design description of each sub-module in the module is introduced as follows:

APB slaves, according to the AMBA standard, are slave devices on the APB bus except the APB bridge [17, 18]. All hosts in the system can access the slave devices connected to the APB bus through the APB bridge. Since APB is designed for modules that do not require high bandwidth, compared with the interface of the AHB bus slave device, the interface of the slave device is much simplified, as shown in the following figure (Fig. 2):

The slave of APB is mainly responsible for address decoding, and realizes the connection between SPI controller module and APB bus. Through this module, ARM processor can read and write the corresponding registers in SPL controller in strict accordance with APB bus protocol, so that it can control the module and peripherals. When writing to the controller, the write data can be locked at the following two time points: when the PSEL is high, at the rising edge of any PCLK; when the PSEL is high, at the rising edge of the pen able. Select signal PSEL to select SPI controller, pwrite to indicate write operation, and address paddr to determine which register is updated by write operation.

The clock divider and frequency dividing logic are used to divide the PCLK clock signal in the host mode. In this design, according to the need, we only use even frequency division and use a frequency division variable bauq step to achieve frequency division control. The frequency division variable is valid when the count value of the internal subtraction counter is zero and the SPI controller is working_ Only. Included in the main

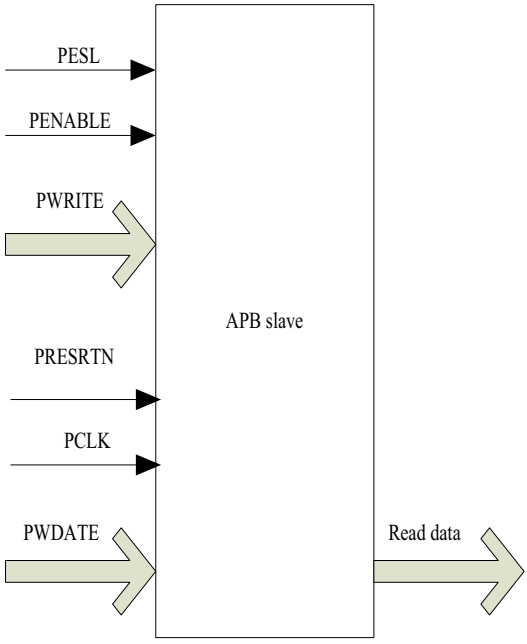

Fig. 2. APB end interface

mode state machine control logic and port control logic. When baud_ When step is high, the state machine will jump.

In the data buffer module, in the SPI controller, the data FIFO is used to buffer data, and it is divided into receiving FIFO and sending FIFO. FIFO is a first-in, first-out data buffer different from general memory. It does not have a read-write address line, and it cannot address a unit that needs to be read or written by an address line like a general memory, and data can only be written in and read out sequentially, so it is very simple to use. When designing the FIFO, the first-in-first-out data is realized by controlling the movement of the reading and writing pointer. Therefore, the key to the design is to control the movement of the read and write pointers, and the relationship between the read and write pointers to determine whether the FIFO is empty or full. The specific implementation process is: after reset, the read pointer and the write pointer are both 0 and point to the same storage unit. Each write operation to the FIFO is to write data to the storage unit corresponding to the current write pointer, and then the write pointer executes the addition. 1 operation, pointing to the next storage unit of data to be written; every time the FIFO is read, the data pointed to by the current read pointer is read, and then the read pointer performs an operation to increase by 1, thereby pointing to the next data to be read Storage unit. In this way, the requirement that data is written first and read first can be realized, which is completely consistent with the timing before and after the data cache. A valid empty signal means that the current FIFO has no data dimensions, and a valid full signal means that the current FIFO is full and data cannot be written. According to needs, our FIFO depth and width are both 32 bit.

Finite state machine is an important method to realize control logic in digital system. Most digital systems are composed of data unit and control unit. The data unit can process and transmit the data, while the control unit controls the operation of the data unit. The finite state machine is usually the main body of the control unit, and its output control signal is generated according to the external input signal and the state information of the data unit. In the main mode of this design, we use FSM to control the data transmission process, so as to realize the control of SPI controller. The key to design a state machine is to determine the state set of the state machine and the transition relationship between these states. The state transition diagram is as follows (Fig. 3):

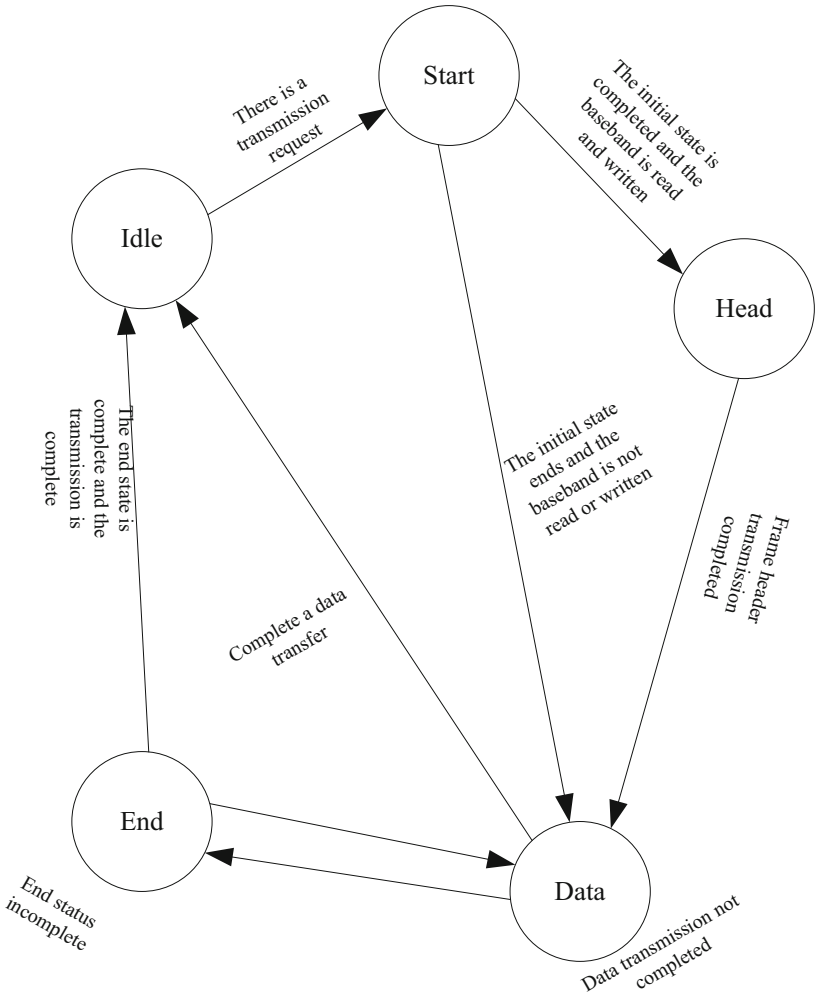

Fig. 3. State transition diagram

The register module includes control register, data register and status register. First, define the type, word length and address of all registers in SPI controller, as shown in the following table (Table 2):

Table 2. Register summary of SPI controller

Register name	Type	Width	Describe
SPCR0	R/W	16	SPI control register
SPCRl	R/W	32	Transmit control register
SPCR2	R/W	32	Receive control register
SPCR3	R	16	Baseband data register
SPDR0	W	32	Transmit FIFO data register
SPDRl	R	32	Receive FIFO data register
SPSR	R	16	Status register
SPBRR	R/W	16	Baud rate configuration register
TXFTLR	R/W	8	Transmit fif0 threshold register
RXFTLR	R/W	8	Receive fif0 threshold register
SPRISR	R	8	Interrupt original status register
SPIMR	R/W	8	Interrupt final status register
SPISR	R	8	Interrupt clear status register

3 System Software Design

In the virtual scene, the attribute transformation of 3D model, such as position, size and rotation, is based on the corresponding mathematical model. The transformation of 3D model can be regarded as the transformation of model with the coordinate system unchanged or the transformation of model with the coordinate system unchanged. The essence of three-dimensional model transformation is the calculation of linear equation by computer. The basic formula of the calculation is as follows:

$$M_v = \begin{bmatrix} m_{00}m_{01}m_{02}m_{03} \\ m_{10}m_{11}m_{12}m_{13} \\ m_{20}m_{21}m_{22}m_{23} \\ m_{30}m_{31}m_{32}m_{33} \end{bmatrix} \begin{bmatrix} v_0 \\ v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{1}$$

By performing matrix operations on the data of the three-dimensional model, the computer obtains the new data of the three-dimensional model after the specified action is completed, and realizes the translation, rotation, and scaling transformation of the three-dimensional graphics.

Graphic translation transformation. Translation refers to moving every vertex of an object by the same displacement without changing its face and face normal. The translation matrix is expressed in the following formula:

$$T\left(t_x, t_y, t_z\right) = \begin{bmatrix} 100t_x \\ 010t_y \\ 001t_z \\ 0001 \end{bmatrix} \tag{2}$$

In formula (2), $\left(t_x, t_y, t_z\right)$ represents the displacement vector of translation.

Graphics rotation transformation, rotation matrix is through the origin of the line as the axis of rotation, each vertex of the object is rotated by a certain angle. Rotation changes the direction of the vertex and face normals of an object, but does not change its face information. The three-dimensional graphics rotate around the x, y, z axis, and the rotation matrices are shown in the following formulas:

$$R_x(\theta) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta & 0 \\ 0 & \sin\theta & \cos\theta & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{3}$$

$$R_y(\theta) = \begin{bmatrix} \cos\theta & 0 & \sin\theta & 0 \\ 0 & 1 & 0 & 0 \\ -\sin\theta & 0 & \cos\theta & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{4}$$

$$R_z(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta & 0 & 0 \\ \sin\theta & \cos\theta & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{5}$$

Based on the above formulas (3)–(5), the transformation matrix rotating around any axis can be obtained.

Graphic scaling transformation, scaling refers to reducing or enlarging an object in a certain proportion. Scaling transformation changes the shape of the object. Usually the scaling matrix is also expressed as a matrix of three scaling factors relative to the three coordinate axes as shown below:

$$S\left(s_x, s_y, s_z\right) = \begin{bmatrix} s_x & 0 & 0 & 0 \\ 0 & s_y & 0 & 0 \\ 0 & 0 & s_z & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{6}$$

In formula (6), s_x, s_y and s_z represent the object's scaling factor in X, Y and Z axes respectively.

According to the above process to complete the virtual scene processing, in order to complete the design of electrical engineering and automation professional virtual simulation experiment teaching system.

4 Experimental Comparison

In order to verify the effectiveness of the virtual simulation experiment teaching system of electrical engineering and automation specialty, the experimental comparison is carried out, and the traditional system is compared with the system of this study, and the effectiveness of the two systems is compared.

4.1 Real-Time Comparison of System Interaction

The system of this study and the traditional system are used for learning, and the real-time interaction of the two systems during learning is compared (Fig. 4).

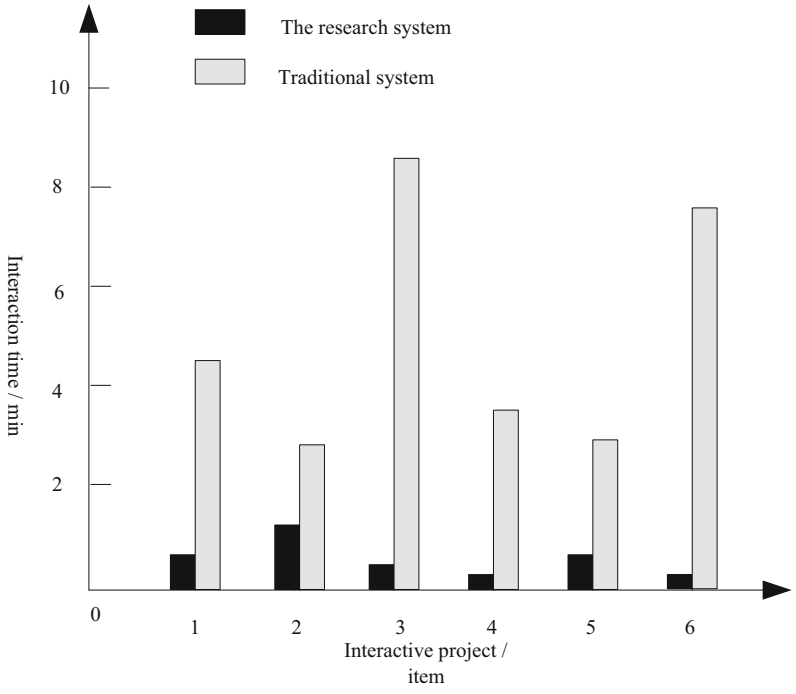

Fig. 4. Real-time comparison of system interaction

From the above figure, it can be found that the real-time interaction of the system in this study is better than the traditional system.

4.2 Comparison of System Data Transmission Packet Loss Rate

For the two systems during data transmission, the loss rate of data transmission in the system, the comparison results are shown in the following figure (Fig. 5):

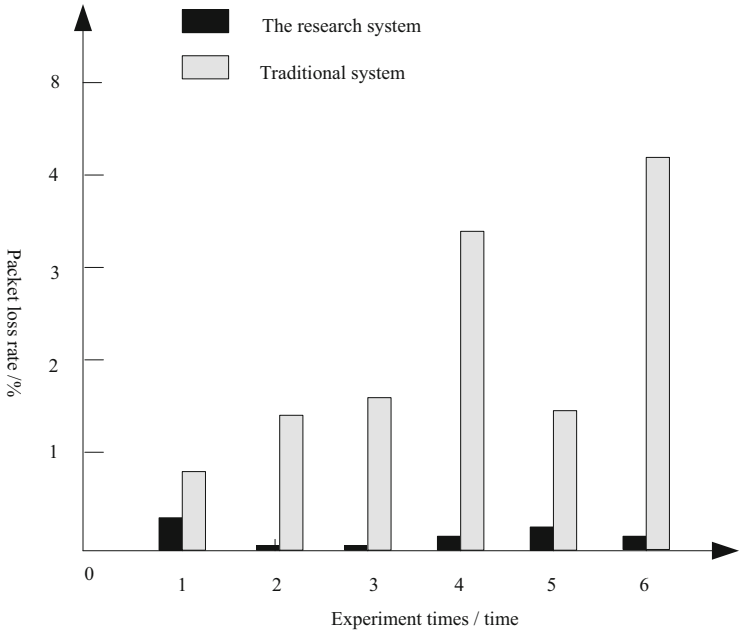

Fig. 5. Comparison of packet loss rate of system data transmission

According to the figure above, it can be found that the data packet loss of the system in this study is smaller than that of the traditional system. This paper design a virtual simulation conversion to complete the research on the virtual simulation experiment teaching system of electrical engineering and automation.

5 Concluding Remarks

This paper designs a virtual simulation experiment teaching on the basis of preliminary preparations such as investigating the existing problems of electrical engineering and automation professional experiments, conducting multiple field experiments, collecting laboratory and experimental equipment pictures, organizing experimental data, and reading a large number of documents system. After the user enters the virtual experimental system, according to the operating prompts, with the help of a computer mouse and keyboard, etc., they can learn about the punching equipment, the operation of the experiment, and the learning of the experimental principle.

In the follow-up research, the system logic design and script design should be improved to enhance the real-time nature of interaction and the fluency of operation. This is the difficulty that needs to be overcome in future research. At the same time, in the system, the user interacts with the objects in the virtual experiment scene through the computer mouse and keyboard, and the operation is not convenient enough. In the future, the experiment operation can be carried out through the helmet display, the data glove or the handle, and the immersion is stronger. This system does not involve multi-person collaboration. In the future, the virtual experiment system will develop in the direction of multi-person collaborative experiment operation. Northeast Dianli University has established a virtual simulation experiment teaching center for the production process of the electric power industry, which can simulate subcritical to ultra-supercritical domestic units, can simulate the power production process of nuclear power plants, and the power transmission and distribution process of 35–500 kV substations.

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