A Gigabit Ethternet Switch Based Software Radio Platform for Gbps Wireless Communications

Chuan Liu, Xiang Chen, Xiujun Zhang, Ming zhao, Shidong Zhou, Jing Wang
Department of Electronic Engineering, Tsinghua University
Tsinghua National Laboratory for Information Science and Technology
Beijing 100084, China
E-mail: {liuchuan86,chenxiang98}@gmail.com

***Abstract*—Software Radio (SR) is an emerging paradigm of the wireless communication system design due to its flexibility and adaptability. However, the implementation of SR platform is always challenging, especially for high date rate transmission such as up to 1Gbps. Although general-purpose processor(GPP) based SR platform can take full advantages of Software Radio, the performance is often limited due to the lack of real-time processing capacity for high-throughput radio systems, especially for high-throughput channel decoding. Therefore, hardware accelerating units(HAU) are usually also involved in the SR platform, such as field programmable gate arrays(FPGAs) and embedded digital signal processors(DSPs). As HAUs and GPPs have their own advantages for different applications in SR, the scalability of interface is a bottleneck in the implementation of SR platform. In this paper, a Gigabit Ethernet(GE) switch based programmable platform for Gbps wireless communications is presented. By means of the good scalability and flexibility of GE interface, the new structure based on GE data-switch combines the real-time computing performance of HAUs with the adaptability and programmability of GPPs, which can provide a radio platform with great scalability for the development of future wireless communication technologies. As a demonstration, a MIMO-OFDM radio system has been designed and implemented on this platform, which can achieve a throughput up to 1Gbps.**

Keywords- MIMO-OFDM; Gigabit Ethernet ; Software Radio; Gbps

I. INTRODUCTION

Software Radio(SR) [1], which suggests that current wireless communication platform implemented primarily in Application Specific Integrated Circuits(ASIC) should be supplanting by fully programmable devices, is turned out to be a new paradigm of the wireless communication systems. SR technology brings the flexibility, adaptability and cost efficiency to drive wireless communications forward. In recent years, the wide-reaching benefits of SR technology have been realized by service providers, product developers, and through to end users.

However, in practice of the SR, there are different choices which have presented developers with a dilemma. Many current SR platforms are based on general-purpose processor(GPP) architectures such as multi-core processors based Personal Computers(PCs)[2], CELL B.E.[3], which can take full advantages of Software Radio for its great adaptability and programmability. However, existing GPP-based SR platforms can achieve only limited system throughput due to the lack of real-time signal processing capacity, especially for high-throughput channel decoding. For example, the Sora system developed by Microsoft achieves only a few Mbps throughput with multi-core CPU [2]. The WiMAX demo implemented on CELL multicore platform [3] only considers the Viterbi decoding for convolutional codes with about 30Mbps throughput. Meanwhile, turbo decoding on single CELL can only approach to 10Mbps[4].

In contrast, SR platforms based on hardware accelerating units(HAU) such as field programmable gate arrays(FPGAs) and embedded digital signal processors(DSPs) can meet the requirements of real-time signal processing in high-speed wireless communications. However, the modification and upgrading of the system implemented in HAUs are usually difficult due to their relatively poor programmability and debugging.

As the GPPs and HAUs have their own advantages and limitations, a solution is to take either of them into different processing units for different functions. Therefore, interface with efficient scalability is needed to combine various kinds of processing resources together in a unique software radio platform. However, the interface used in existing SR platforms, such as PCI-e in the Sora system[2] and USB 2.0 in the GNU radio[5] cannot meet such requirements.

In this paper, a Gigabit Ethernnet(GE) switch based SR platform for Gbps wireless communications is presented. This platform is formed in a distributed structure while GE is involved in the system to provide an open interface for high-speed data exchange. By means of the scalability and flexibility of GE interface, the SR platform takes the advantages from both HAUs and GPPs to achieve good real-time processing performance with good adaptability and flexibility. Therefore, this GE based structure provides a potential universal platform with great scalability for both implementations and experiments of wireless communication technologies. As a demonstration, a MIMO-OFDM radio system has been designed and implemented on this platform, which can achieve a throughput up to 1G bps.

The rest of the paper is organized as follows. Some backgrounds on the Gigabit wireless transmission platform are given in Section Ⅱ. Then the GE switch based architecture of

This work is partially supported by National Basic Research Program of China (2007CB31060), China's Major Project (2009ZX03003-009), NCET-05-0071, IBM OCR and SUR programs, PCSIRT and China's 863 Project (2009AA011501).

the platform is presented in Section Ⅲ. In Section IV, the design and implementation of the MIMO-OFDM radio system are introduced. Finally, we evaluate the performance of the platform based on the demonstration system by field tests in Section Ⅴ and Section Ⅵ concludes the paper.

II. BACKGROUNDS ON GIGABIT PLATFORM

A. Software Radio

As the wireless standards are evolving and new algorithms are proposed rapidly, the platforms implemented primarily in ASICs are found to be difficult to catch up with the developments and upgrading of new wireless techniques. While Software Radio brings the flexibility, cost efficiency and lower power to drive communications forward. The basic idea of SR is to design an open, modular, standardized general-purpose platform, on which a variety of processing functions in wireless communications can be operated by software [1]. SR architecture emphasizes the openness and full programmability, which can change the configuration by software updating to achieve new functionality.

Based on this idea, devices with programmability such as PC, DSP, FPGA, etc. have gradually replaced some roles of ASICs in traditional mobile communications systems, making system design much more flexible and scalable. SR techniques are consequently the key points for us to build our Gbps wireless transmission platform.

B. MIMO-OFDM

MIMO systems provide an additional spatial dimension for communications and yield a degree-of-freedom gain. These additional degrees of freedom lead to obvious capacity increase: for a system with N transmit and receive antennas respectively, the capacity increase is proportional to N. Meanwhile, Orthogonal frequency division multiplexing (OFDM) modulates the information on parallel sub-carriers in the frequency domain. It has a distinct advantage in anti-fading ability than traditional single-carrier technologies.

Therefore, MIMO-OFDM [7], which combines MIMO and OFDM technologies, is considered as the physical layer scheme in our Gbps wireless transmission system, due to its distinct advantages in many aspects of system performance such as system capacity, spectral efficiency and anti-fading ability.

C. Gigabit Ethernet

IEEE 802.3ab[6], which is ratified in 1999, defines Gigabit Ethernet (GE) transmission as 1000BASE-T. Several standards such as 1000BASE-LX, 1000BASE-BX have been evolved in the following few years.

GE is inherited from standard Ethernet technologies but with much higher data throughput, which can support most protocol specifications of the original standard such as Transmission Control Protocol(TCP) and User Datagram Protocol(UDP). GE interface, which often consists of Gigabit Ethernet cables, Gigabit switches and Network chips, can achieve a variety of specific data exchange functions by using different communication protocols and GE layout structures. Actually, GE is widely used as in-out interface in many devices for its high throughput and great flexibility. Here, GE is also considered in our SR platform to connect each processing unit.

III. GE SWITCH BASED STRUCTURE

As mentioned in Section II-B, according to the OFDM theory, the whole transmission band of OFDM signals can be divided into several sub-bands. Each sub-band contains a number of non-interfering sub-carriers, which can be processed independently. The multi-band capability of the OFDM makes the design of broadband system much more flexible. However, it brings great challenges in organizing the SR platform to process different sub-bands in different units. GE interface is consequently involved in to connect each of the processing units and the RF front-ends. Based on GE interface, we establish a high-throughput pipeline for data stream, as well as a low-latency path for the control signals switched between each unit in our SR platform. A distributed processing strategy is adopted to get high-efficiency parallel computing ability and to reduce the requirements of computation capacity for each processing unit. The detailed structure of the GE switch based SR platform will be presented as follows.

A. The Architecture of GE based SR Platform

The architecture of the GE based SR platform is illustrated in the Fig. 1.

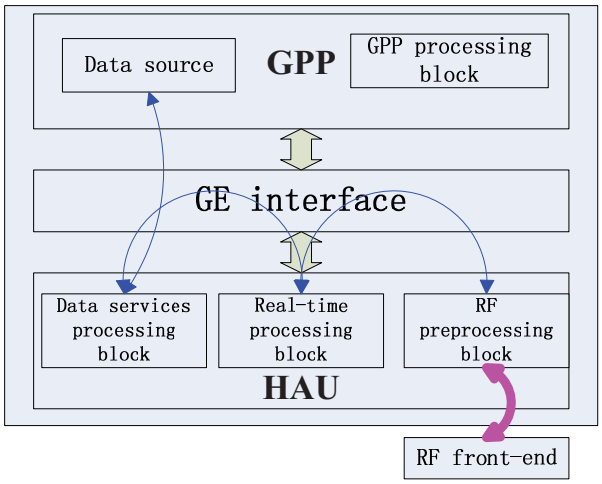

Fig.1. GE based SR Platform

As shown in Fig.1, this wireless platform can be divided into the following four function blocks: data services processing block, real-time processing block, Radio Frequency(RF) preprocessing block and GPP processing

block. Taking the transmitter side for example, we can show the data switch process on GE based SR platform as follows.

During the period of data transmission, data stream is firstly transformed into fixed-length normalized packages by data services processing block. With GE switching, data packages are distributed to different sub-bands and re-collected after frequency-domain processing (for example, channel coding, modulation, sub-carrier mapping and pre-coding) in each real-time processing block. Then the data packages in the frequency domain are distributes to each of the RF preprocessing block (performing IFFT, inserting of CP, etc) through GE interface. Finally, after time-domain processing the data streams are transferred to the RF front-ends.

The basic functional partition of GE based SR platform for the receiver side is similar to the above transmitter side. However, most complex computation processes, such as channel estimation, timing and frequency synchronization, matrix decompositions for MIMO detecting and pre-coding, have been allocated to GPP processing block. The left function for the receiver is only channel decoding module in real-time processing block for HAUs.

On the other hand, GE interface is a powerful debugging tool for system developers. It is convenient to get data samples from any in-out port in this platform by devices supported GE. For instance, the GPP processing block can obtain data samples from the stream and switch information with the others during transmission by using GE interface.

B. The Protocol of GE Interface

The data pipeline in GE interface in the above SR platform, which is separated from control path, bridge the high-speed data stream between data services processing block, real-time processing block and RF processing block. As each processing unit is identified by Media Access Control(MAC) address, the routing between different MAC address is decided by the data pipeline. For simplicity, the MAC protocol defined by IEEE 802.3 [6] can meet the requirements of data switch here, which is implemented on HAUs by using HDL.

In contrast, the throughput requirements of control path in GE interface are relatively low. However, more complicated protocol for the control path is required than that for the data path. In our SR platform, an expansion of standard MAC protocol is used as the protocol for the control path. In the expanded MAC protocol, a fixed segment in data field with a few bytes will be specifically defined to identify the functionality and address the registers on HAUs. The functionality can be achieved on HAUs by using NIOS II, which is an embedded soft-core provided by Altera[8].

IV. IMPLEMENTATION OF MIMO-OFDM SYSTEM

As a demonstration, a broadband MIMO-OFDM wireless transmission system has been designed and implemented on the above GE switch based SR platform.

In order to reach up to 1 Gbps data rate, two sets of 4x4 MIMO-OFDM systems have been deployed in our Gbps system. Each set of the equipments has nearly the same architecture both for hardware and software, but works on different frequency bands independently. Therefore, each set can achieve a throughout up to 500M bps.

The parameters of each 4x4 MIMO-OFDM equipment set are given in the following tables.

TABLE I – GENERAL LINK LEVEL PARAMETERS

Parameters	***Value***
TX/RX antennas	4x4
Carrier frequency(GHz)	14.417/14.483
Signal bandwidth(MHz)	33 for each set
Sampling frequency(MHz)	40.96
Channel coding	(7680,6400) QC-LDPC
Modulation constellation	64QAM
Channel condition	Indoor(50m LOS environments) Multi-path slow fading channels

TABLE II – OFDM-PARAMETERS

Parameters	***Value***
FFT size	256
Modulated sub-carriers	168
Sub-carrier bandwidth(KHz)	160
OFDM symbol length(us)	6.64
CP length(us)	0.39
OFDM symbols per data frame	8
Pilot / data OFDM symbols	1/64

Then we will discuss the detailed implementation of the above 4x4 MIMO-OFDM system on each block of the GE SR platform in the following subsections.

A. Data Services Processing Block

The architecture of the data services processing block can be illustrated in the Fig. 2.

As mentioned in Section III-A, the data services processing block can communicate with real-time processing block and GPP processing block through GE interface. Thus, the data services processing block bridge the Data Source from the GPP with other blocks on HAUs, which are implemented on HAUs with GE PHY chips, such as BCM546x.

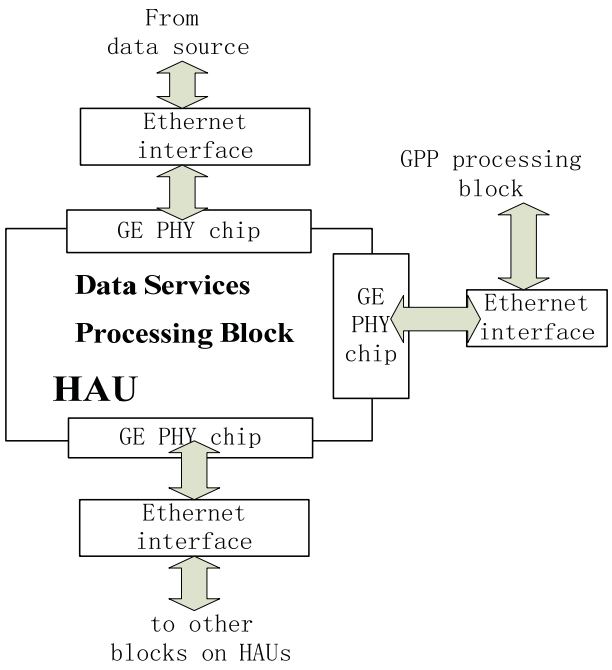

Fig.2. Structure of Data Services Processing Block

The software on the HAU developed by HDL can split or fill the data block into a fixed size, in order to transform the random data services into a steady data stream. Then the steady data stream will be passed to next block in form of MAC packages according to the 802.3 MAC protocol. The GPP processing block may adjust the parameters in data services processing during the data transmission period.

B. Real-time Processing Block

As mentioned in Section II-B, for OFDM signals, the information is modulated on orthogonal sub-carriers without interfering each other in the frequency domain. All sub-carriers can be divided into several sub-bands and processed in parallel.

Based on this principle, the real-time processing block consists of multiple basic processing units. Each unit corresponds to one of the sub-bands data processing, which operates independently. The computation requirements of each unit can be reduced by times due to the distributed processing strategy. The signal processing algorithms with more computational complexity can be introduced in frequency-domain processing to obtain better performance.

Each real-time processing unit is also implemented with HAUs and GE PHY chips, on which frequency-domain processing, such as Channel Coding/Decoding, Sub-Carrier Modulation/Demodulation and Phase Noise Correction in each sub-band can be operated independently. Similar to data services processing block, the data stream is passed to next block in the form of GE MAC packages. The GPP processing block can also adjust the parameters in frequency-domain processing block during the data transmission period.

C. RF Preprocessing Block

Through GE switches, the data streams from all sub-bands will be collected and then re-divided into several sub-streams, each of which is assigned to a single RF front-end. In general, the RF preprocessing block also consists of multiple basic processing units, which is illustrated in Fig. 3.

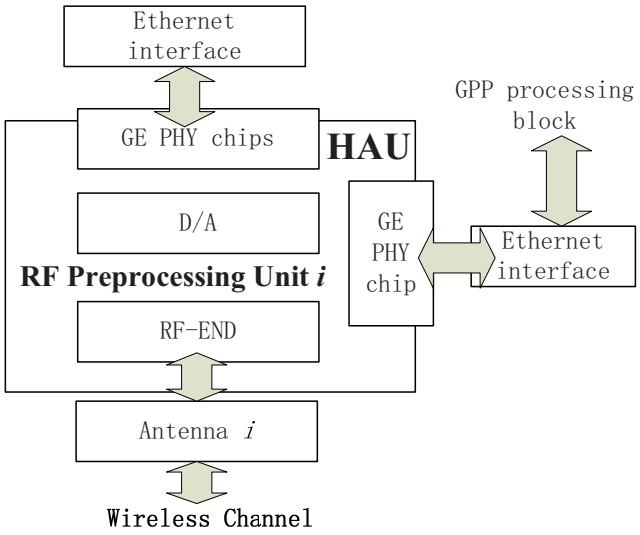

Fig.3. Structure of RF Preprocessing Unit

D. GPP processing block

Although the real-time processing capacity of GPPs cannot match the needs of Gbps transmission, the algorithms working on low-rate samples such as channel estimation, timing and frequency synchronization[1], matrix decompositions for MIMO detecting and pre-coding, could be implemented on GPPs for their great computation capability and programmability. On the other hand, the parameters of the other processing blocks could be configured or adjusted conveniently by GPPs through GE interface.

In addition, by means of the user-friendly and abundant development environments, the GPPs can provide convenient debugging tools during the system developments. For instance, the state of HAUs can be obtained by GE interface during transmission to GPPs in the form of MAC packages. Developers can analysis the data in familiar environments by sophisticated tools on GPPs.

V. EVALUATION IN FIELD TESTS

In this section, we will evaluate the end-to-end Gbps transmission performance delivered by this SR platform. In

[1] Here, timing and frequency synchronization are only performed at the beginning of the transmission, thereinafter synchronization tracking state will be checked to keep low-rate samples character.

our MIMO-OFDM demonstration over the GE switch based SR platform, a PC with dual-core CPU operating at 1.6GHz is used as the GPP at each side of transmitter and receiver. For each HAU, two Altera Cyclone 3C80 FPGA chips are used as the major components, each of which is combined a GE PHY chip (BCM546x) to support 4 ports of GE interface. The field tests are performed in the FIT Building in Tsinghua University.

In the following, we will present that the demonstration radio system can achieve 1Gbps throughput on wireless multi-path slow fading channels. Meanwhile, the system performance characterized by spectral efficiency and peak data rate in wireless communications will also be evaluated.

As mentioned in Section IV, the demonstration radio system consists of two sets of 4x4 MIMO-OFDM sub-system. Each set can achieve 500Mbps throughput in indoor environments with the transmission distance over 50m. Fig. 4 shows the transmitter and receiver built on the GE switch based SR platform, respectively.

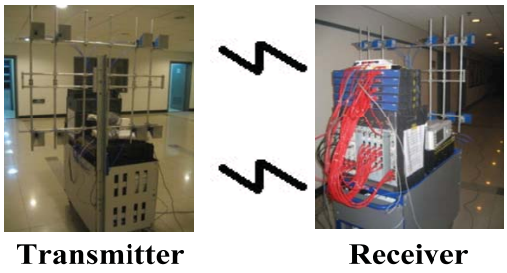

Fig.4. Transmitter and Receiver on the GE SR Platform

Table III shows the field test results of the peak data transmission throughputs of the Gbps platform for varies applications, wherein Netperf is a benchmark that can be used to measure the performance of many different types of networking. We have also developed programs to test the system throughput with TCP and UDP protocols.

TABLE III – THROUGHPUT TEST RESULTS

Application	*Throughput(Mbps)*
Netperf	**860**
UDP	**880**
TCP	**760**

Although the Gbps demonstration system on this GE switch based SR platform can provide over 1Gbps data transmission of the wireless PHY layer, the throughput of such a system is still limited for the several following reasons. First, not only the read-write speed of data source affects the performance, but also the output bandwidth is limited GE interface. Second, the actual data rate is lower than the theoretical data rate for the overhead of the Ethernet protocol.

Fig. 5 presents the spectral utilization of our Gbps wireless transmission system.

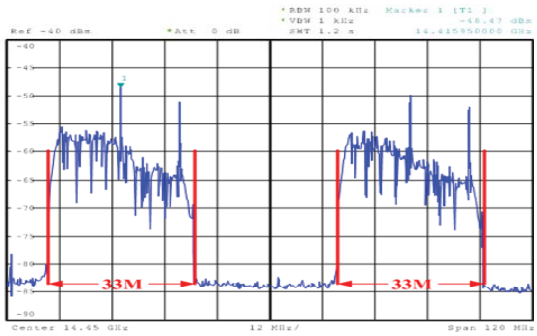

Fig.5. Illustration of Spectral Utilization

From Fig. 5 we can see that each set of 4x4 MIMO-OFDM sub-system occupies a bandwidth of 33MHz. Referring to the peak data throughput, the peak spectral efficiency is higher than 15bps/Hz.

VI. CONCLUSIONS

This paper presents a GE switch based programmable SR platform for Gbps wireless communications. Due to the good scalability and flexibility of GE interface, this platform has both the real-time processing capability in HAU and adaptability and programmability in GPP, and hence is suitable for the development of future wireless communication systems. As a demonstration, a radio system with MIMO-OFDM technique has been designed and implemented on this platform, which is proved to be able to achieve the throughput of up to 1G bps.

The flexibility provided by the GE interface make the SR platform not only a convenient tool for the development and implementation of Gbps radio systems, but also a scalable system to support even more complex signal processing algorithms in the distributed architecture. We hope that the GE switch based SR platform will contribute to the experimentations and innovations in future wireless communication technologies.

REFERENCES

[1] Joe Mitola The software radio architecture, In IEEE Communications Magazine, May 1995 26-38.

[2] Kun Tan, Jiansong Zhang, Ji Fang, et al., "Sora: High Performance Software Radio Using General Purpose Multi-core Processors," in 6th USENIX Symposium on Networked Systems Design & Implementation 2009, USENIX, 2009.

[3] Jianwen Chen, Qing Wang, Zhenbo Zhu, Yonghua Lin, “An Efficient Software Radio Framework for WiMAX Physical Layer on Cell Multicore Platform,” in ICC2009, in Dresden, Germany.

[4] Huili Guo, Juntao Zhao, etc., "High Performance Turbo Decoder on CELL BE for WiMAX System," in IEEE WCSP09, in Nanjing, China.

[5] Gnu radio. http://www.gnu..org/software/gnuradio.

[6] IEEE 802.3x Specification for 802.3 Full Duplex Operation IEEE standard 802.3,1998.

[7] Kyung Won Park An MIMO-OFDM Technique for High-Speed Mobile Channels.School of Electrical and Electronic Engineering, Chung-Aug Univ KORIA.

[8] http://www.altera.com/products/ip/processors/nios2/ni2-index.htm