Design of a All-CMOS Second-Order Temperature Compensated Bandgap Reference

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Abstract. In this paper, a second-order temperature compensated bandgap voltage source based on 0.18 μm standard COMS process with low temperature coefficient (TC) and high power supply rejection ratio (PSRR) was presented. The core structure of the circuit was the improvement of the traditional bandgap reference. The cascade structure was adopted to improve the PSRR and the line sensitivity, and the square of the proportional to absolute temperature current I_{PTAT2} was utilized to compensate the first order circuit. This circuit constitutes of all-CMOS transistors in order to save the power consumption. The simulation results show that TC of the bandgap reference source in the −25 °C–125 °C temperature range, is 4.5 ppm/°C. At low frequency, the PSRR reaches −45.63 dB@100 Hz, and the power consumption is only 287.2 μW.

Keywords: Bandgap reference source · Second-order compensation · Temperature coefficient · Power supply rejection ratio

1 Introduction

Bandgap reference (BGR) is an essential basic block in VLSI and many electronic systems. It is widely used in many analog, digital and mixed signal IC, such as A/D converter, DRAM and flash control module, so its performance will have an impact on the performance index of the whole signal processing system [1]. Bandgap voltage reference is widely used in analog and digital circuits and is an important part of the system [2].

Due to high precision and temperature independence, high precision BGR is an indispensable module in many applications, Like data and power converters. However, due to the non-linearity of base-emitter voltage of BJT, the temperature characteristics of first order temperature compensation BGR are limited. Through the study found that usually the temperature coefficient of first order compensation BGR range between 20 and 100 ppm/°C [3]. In addition, the reference voltage source provides a high-precision voltage reference for other functional modules in the circuit system, or is converted into a high-precision current reference. For analog circuit systems, the performance of reference voltage source directly affects the accuracy and performance of the whole system [4, 5]. Therefore, in order to achieve better temperature independence and

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provide a stable reference voltage for the system, we need to add a high-price compensation circuit to compensate the first-order bandgap reference circuit.

In the CMOS second-order temperature compensated bandgap reference source proposed in this paper, the structure of the first-order bandgap reference circuit adopts the standard CMOS process, which is improved in the traditional bandgap reference voltage source structure [6], the original resistance is replaced by PMOS tube, reduces the power consumption of the circuit. Not only the cascode structure can not only improve the power rejection ratio of the circuit, but also enhance the stability of the whole circuit. The second order temperature compensation circuit adopts IPTAT2 circuit to compensate the first order circuit. The circuit has the advantages of simple structure, low temperature coefficient and high power rejection ratio.

2 First-Order Compensating Bandgap Reference Voltage Source

Since the idea of bandgap reference source has been proposed, many researchers have improved and optimized this structure, a wide variety of bandgap reference source core circuits based on bipolar transistors are designed. But many structures cannot be implemented by using standard CMOS processes, since the collector of the triode PNP of the traditional Kujik structure is directly grounded, the standard CMOS process can be used to realize it [7]. Therefore, this design adopts Kujik structure as the core structure of the first-order bandgap reference voltage source.

In this paper, the first-order bandgap reference source circuit is improved by using the basic structure of Kujik, as shown in Fig. 1. Different from the traditional bandgap reference, the original resistance is replaced by the line of PMOS tube M14-M18, which helps to reduce the power consumption. On the basis of single-row PMOS tube, a layer of PMOS tube M19–M23 is connected in series. In this way, two rows of P tubes form a common source and common gate structure, which can not only improve the power rejection ratio of the circuit, but also enhance the stability of the whole circuit. Bipolar transistor Q1–Q5 will produce a positive and negative temperature coefficient, the voltage of the zero temperature coefficient can be obtained by adding the appropriate specific gravity. The resulting current is then copied to Q5 through the current mirror, and the output voltage of the first-order bandgap reference is finally obtained.

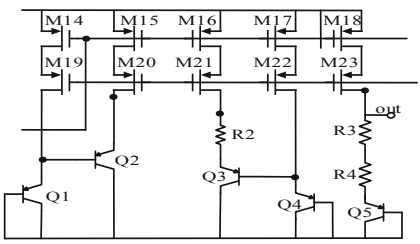

Fig. 1. First-order bandgap reference with cascade structure

Second, the PNP bipolar triode Q3 and Q4 are connected to Q1 and Q2 in series, reducing the effect of the misalignment voltage of the operational amplifier on the reference output. The collector electrodes for transistors Q1, Q2, Q3, and Q4 are all connected to the ground, and this structure is guaranteed to be implemented under standard CMOS processes. Through analysis, the output expression of the band gap reference source core circuit designed in this paper is shown in Eq. (1) by

$$V_{REF}=V_{\mathrm{be5}}+\frac{(2V_t \ln \mathrm{N}-V_{OS})(R3+R4)}{R2} \tag{1}$$

Since the base and emitter voltage V_{be} of Eq. (1) Q5 has a positive temperature coefficient and $2V_t$lnN has a negative temperature coefficient, V_{OS} is the misaligned voltage, and the output voltage V_{REF} is basically unchanged, so the effect of misaligned voltage on the bandgap reference source can be reduced through the base-emitter connection of bipolar transistors. It is also possible to adjust the ratio of R3 + R4 to R2 to obtain the first-order bandgap reference output voltage.

3 Second-Order Temperature Compensated Bandgap Reference Voltage Source

In fact, only the first order temperature coefficient of the output voltage can be eliminated by the first order compensated reference source, then the voltage independent of temperature is obtained, but the high voltage component that cannot be compensated is not eliminated, so high compensation is needed [8]. V_T is proportional to the absolute temperature and the value is small, which is the voltage of the first-order temperature coefficient, so the higher order temperature term introduced from V_T is basically negligible. High order temperature coefficient is mainly determined by the temperature characteristics of bipolar transistors V_{BE}, so it can be obtained:

$$V_{BE}(T)=V_G(T)+\left(\frac{T}{T_{\mathrm{r}}}\right)[V_{BE}(T_{\mathrm{r}})-V_G(T_r)]-\eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right)+\left(\frac{kT}{q}\right)\ln\left[\frac{I_c}{I_c(T_r)}\right] \tag{2}$$

Where V_G is the bandgap voltage of silicon at 0 K, η is the electric field factor, T_r is a given constant temperature. Since I_C is related to temperature, it can be set $I_C(T)=FT^{\delta}$, δ is a coefficient introduced by resistance, bring it into the above formula:

$$V_{BE}(T)=V_G(T)+T\left\{\frac{V_{BE}(T_{\mathrm{r}})-V_G(T_{\mathrm{r}})}{T_{\mathrm{r}}}+\frac{\mathrm{k}}{\mathrm{q}}\left[\ln\frac{F}{I_C(T_{\mathrm{r}})}+(\eta+\delta)\ln T_{\mathrm{r}}\right]\right\}-T\mathrm{lnT}\frac{(\eta-\delta)\mathrm{k}}{\mathrm{q}} \tag{3}$$

The last term is the nonlinear component of the TlnT, so it still exists after the first order compensation [9].

The I_{PTAT}^2 second order temperature compensation circuit is introduced in this paper. As shown in Fig. 2, the overall circuit structure is shown in Fig. 3. The second-order temperature compensation circuit consists of M24-M33, M24 is the voltage supplied by the output of the previous amplifier as the conduction voltage, which then produces the bias current I_{PTAT}. The conduction voltage of M25 and M26 is provided by the previous bias circuit, M25 and M26 themselves constitute the bias circuit, which can provide the bias voltage for the second-order compensation circuit. M26, M27 and M29, M30, and M33 can produce a current with a negative temperature coefficient, which is squared with the offset current of M24. The conduction voltage of M31 and M32 is provided by the bias voltage generated by M25 and M26, and they are proportional. The resulting I_{PTAT}^2 current is compensated to the output end through the first-order bandgap reference via M32.

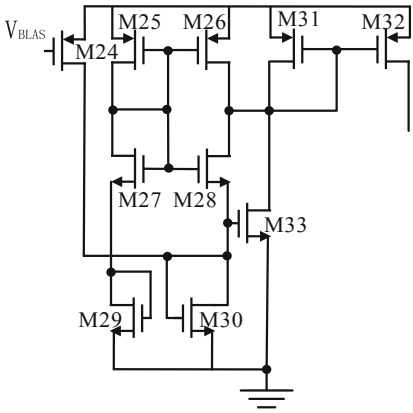

Fig. 2. I_{PTAT}^2 second-order temperature compensation circuit

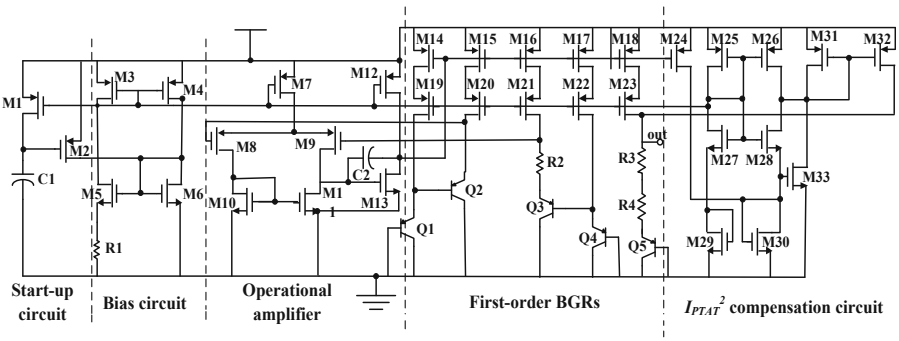

Fig. 3. Second-order temperature compensated bandgap reference voltage source

Analyzed in Fig. 3, V_{BLAS} is the bias voltage of the second-order compensation circuit, which is the output voltage of the operational amplifier. Set the aspect ratio of M25 and M26 to work in the saturation area, the width/length ratio of the pipe M26 is twice that of M25, so the current flowing through M26 is twice that of M25. If the circuit of M25 is, then the current of M26 is $2I_a$. Let $V_{GS28} = V_b$, $V_{GS30} = V_a$, $V_{28} = V_a + V_b$, Set M28 to have the same aspect ratio as M30. It is assumed that all MOS tubes work in the saturated zone and the back gate effect is ignored. If the open voltage of M28 and M30 is set as V_t, it can be obtained through analysis:

$$I_{M28} = \frac{K}{2}(V_b - V_t)^2 \tag{4}$$

$$I_{M30} = \frac{K}{2}(V_a - V_t)^2 \tag{5}$$

$K = \mu_n C_{ox}$, μ_n is the mobility of carrier, C_{ox} is the capacitance of gate oxide layer, so:

$$I_{M30} - I_{M28} = \frac{K}{2}(V_{28} - 2V_t)(V_a - V_b) = I_{PTAT} \tag{6}$$

Then, it can be obtained:

$$I_{M30} + I_{M28} = \frac{1}{4}K(V_{28} - 2V_t)^2 + \frac{(I_{M30} + I_{M28})^2}{K(V_{28} - 2V_t)^2} = \frac{1}{4}K(V_{28} - 2V)^2 + \frac{I_{PTAT}^2}{K(V_{28} - 2V_t)^2} \tag{7}$$

Suppose M27, M29 and M28, M30 have the same, and the parameters of M27 and M29 match perfectly, then:

$$\frac{1}{4}K(V_{28} - V_t)^2 = 2I_a \tag{8}$$

$$I_{M30} + I_{M28} = 2I_a + \frac{I_{PTAT}^2}{8I_a} \tag{9}$$

It can be obtained from Eqs. (6) and (9):

$$I_{M30} = I_a + \frac{I_{PTAT}}{2} + \frac{I_{PTAT}^2}{16I_a} \tag{10}$$

$$I_{M28} = I_a - \frac{I_{PTAT}}{2} + \frac{I_{PTAT}^2}{16I_a} \tag{11}$$

Set the aspect ratio of M33 equal to M30, then:

$$I_{M33} = I_{M30} = I_{\mathrm{a}} + \frac{I_{PTAT}}{2} + \frac{I_{PTAT}^2}{16I_{\mathrm{a}}} \tag{12}$$

Suppose the aspect ratios of M31 and M32 is A, simultaneous Eqs. (10) and (12), the current flowing through M32 can be expressed as:

$$I_{M32} = AI_{31} = I_{M33} + I_{M28} - I_{M26} = A\frac{I_{PTAT}^2}{8I_a} = KI_{PTAT}^2 \tag{13}$$

Among them $K = \frac{A}{8I_a}$, in order to make the tube work in the right area, it need $I_{M28} \geq 0$, so we can be obtained from formula (13). The leakage current of M32 is in a second-order positive temperature relationship, herefore, in the case that all the MOS tubes of this circuit are working in the saturated zone, the aspect ratios of M31 and M32 can be adjusted and set I_a to adjust the leakage current of M32. Finally, the current is introduced to the output end. Finally, the temperature coefficient of the output voltage of the bandgap reference source is corrected.

Analyzed by Fig. 3, this second order temperature compensation reference voltage is including starting circuit, biasing circuit, operational amplifier. Startingup circuit: when it power on, the voltage of C1 can't change suddenly, it amount to break, the grid voltage's absolute value of M2 is power voltage, M2 breakover, the output current will break the original balance of the bias circuit, and get rid of degeneracy point, the circuit starts working normally. Then the power supply began to charge C1, when the voltage of C1 rises to a certain point, the M2 tube stops working, the reference voltage source circuit starts working normally, the starting circuit is off. Biasing circuit: M3 and M4 are constituting the PMOS current mirror, copy the offset current to M7 and M12, provides offset current for two-stage operational amplifiers. M8 and M9 are differential input stage, their grid electrodes are connected to a first-order compensation circuit to clamp the voltage on a bipolar transistor. M10 and M11 are constitute the NMOS current mirror, and Copy the generated current to the output. M7's gird connects biasing circuit, provide stable bias current for the entire operational amplifier. Output stage is constituting by M12 and M13, M13 is common-source amplifier, M12 is output load of the second stage, and also provide the constant current for M13. Miller's capacitor C2 compensates the frequency of the operational amplifier circuit, to prevent the output shock when it works.

4 Simulation Results and Comparison

The design of all the circuits was completed by 0.18 μm standard COMS technology. The simulation of the whole circuit was performed by using Spectre tool. Under the 1.8 V power supply voltage process, the power consumption of the whole circuit was

287.2 μW. At −25 °C–125 °C temperature range, temperature coefficient of the first-order compensation is 9.7 ppm/°C, the power rejection ratio at low frequency is −33.29 dB; Temperature coefficient of the second order compensation is 4.5 PPM/°C, the low frequency power supply rejection ratio reaches 45.63 dB, It is shown that the temperature coefficient and power rejection ratio of the first order bandgap reference are improved obviously after the second order compensation, performance is enhanced. The simulation results are respectively shown in Figs. 4, 5, 6 and 7.

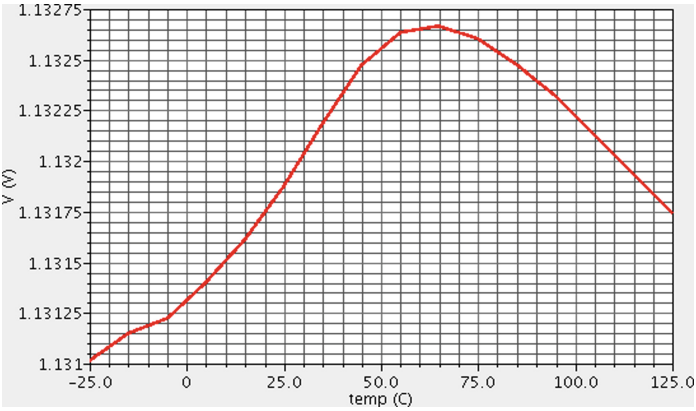

Fig. 4. The first-order compensated BGR voltage versus temperature

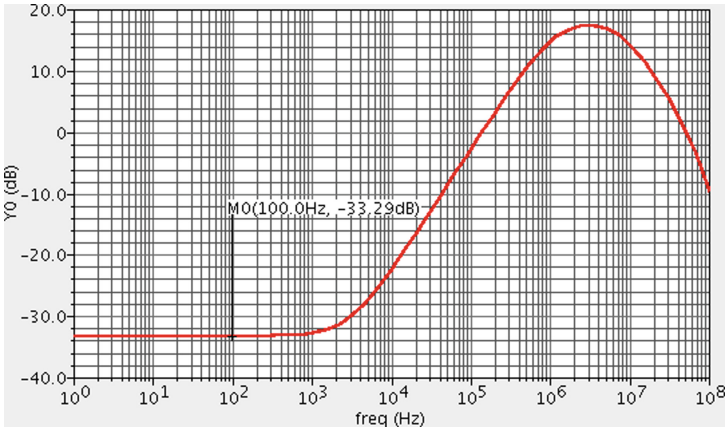

Fig. 5. The PSRR of first-order compensated BGR

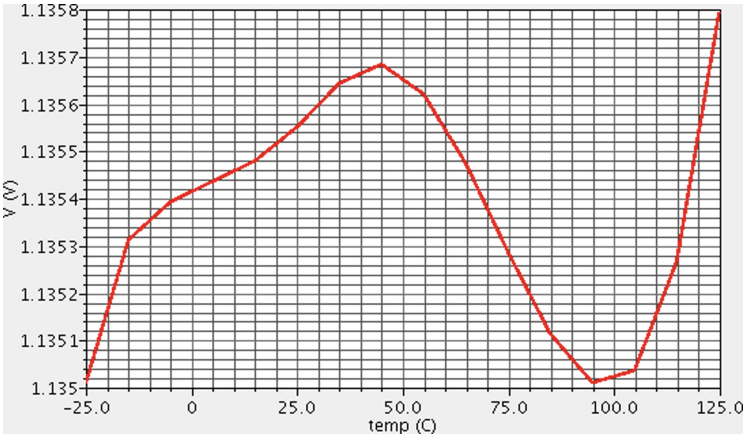

Fig. 6. The second-order compensated BGR voltage versus temperature

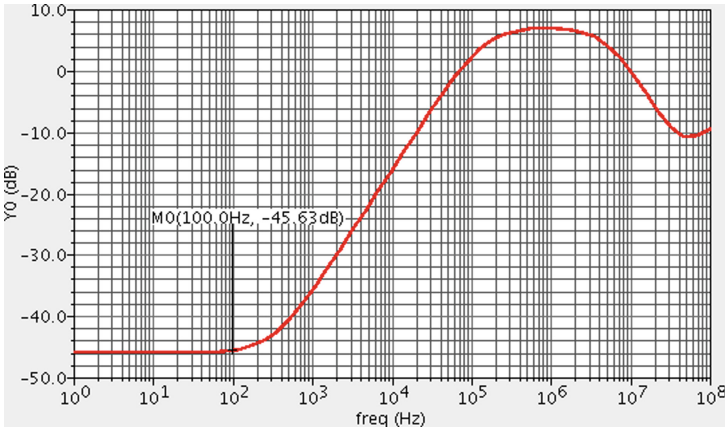

Fig. 7. The PSRR of second-order compensated BGR

This is a comparison between second-order compensated bandgap reference voltage source parameters and the voltage reference parameters of other circuits, as shown in Table 1 below.

Table 1. Comparison of reported second-order compensated BGR

	This work	The literature [5]	The literature [10]	The literature [11]
Process	0.18 μm, CMOS	0.5 μm, CMOS	0.13 μm, CMOS	0.5 μm, CMOS
Temperature range (°C)	−25–125	−50–125	−40–125	−30–130
The power supply voltage	1.2 V–1.8 V	1.24 V–5 V	3 V–3.6 V	2.4 V–5 V
Power consumption	287.2 μW	860 μW	370.37 μW	62.28 μW
Temperature coefficient (ppm/°C)	4.5	14.2	6.2	3.4
PSRR@100 Hz	−45.63 dB	−86.3 dB	−85.4 dB	−43 dB

5 Conclusion

A design of a bandgap reference voltage source with second-order compensation is proposed in this paper,which consist of all-CMOS transistors in order to simplify the circuit and reduce the power consumption. The core circuit is an Kujik structure, using PMOS to take place of the resistance of the traditional structure to enhance the stability and decrease the power dissipation. In addition, the cascade structure can improve the PSRR of the circuit. Second order compensation is achieved by producing I_{PTAT2}. Using 0.18 μm standard CMOS process, TC is 4.5 ppm/°C in −25 °C–125 °C temperature range. PSRR reaches −45.63 dB@100 Hz, with power consumption is 287.2 μW.

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