Design and Implementation of a RF Transceiver Front-End for UHF RFID Localization System

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Abstract. Current RFID readers have a narrow operating bandwidth and not suitable for carrier-phase based RFID localization system requirements. To solve this problem, this paper designs a hardware circuit of the transceiver front-end of ultra-high frequency (UHF) radio frequency identification (RFID) system with wideband operating frequency range. The proposed front-end includes DDS module, transmission module and reception module. Benefiting from the fast switching frequency and wideband output frequency range of DDS, this system can achieve fast frequency hopping within a wide operating bandwidth, which satisfies the requirements of carrier-phase based localization. The results show that the whole hardware system can work correctly within the bandwidth of 700 MHz to 1 GHz, which can meet the design requirements of UHF RFID transceiver front-end.

Keywords: UHF RFID · FPGA chip · DDS chip · Transceiver front-end

1 Introduction

RFID is a wireless communication technology, a complete RFID system consists of readers, antennas, electronic tags [1]. The basic working principle is that the electronic tag enters the magnetic field after reader transmits the signals of specific frequency, the tag sends out a signal by the energy obtained of induced current (Passive tag), or the tag actively sends a signal of a certain frequency (Active tag) [2, 3], then reader obtains the information from the signal and decodes it.

There have already matured RFID chips and readers on the market, such as chips from Texas Instruments and Cypress, Speedway readers from IMPINJ [4] and so on, which comply with EPC global UHF Gen2 (ISO 18000-6C) international standards [5, 6]. The commercial readers also integrate FPGA, modem, power amplification and other modules with good sensitivity and stability. These special chips and readers which have characteristics of reduced development difficulty, easy debugging ability and guaranteed stability, are suitable for RFID system. However, there have more advantages of broadband communication system in localization [7–9], the

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shortcomings of these commercial readers are I/Q data is unavailable and the working bandwidth is so narrow, which cannot be applied in UHF RFID localization system.

To solve these issues, this paper proposes a transceiver to use DDS as its local oscillator to achieve a wide working bandwidth and fast frequency hopping. The receiving front-end can also obtain the I/Q two-way data directly.

2 System Structure of RFID Transceiver

Commercial readers currently on the market have a narrow working bandwidth, result in limited location and distance estimation accuracy. The localization accuracy is related to the bandwidth [10], so the wider bandwidth it has, the higher accuracy can get. This system designs a hardware transceiver front-end using DDS technology, which can achieve a wider working bandwidth to satisfy UHF RFID localization requirement.

2.1 System Structure

System structure diagram is shown in Fig. 1. The system is mainly divided into three modules, DDS module, transmission module and reception module. DDS module is used to provide a local oscillator frequency source for the transmission module and reception module. The modulator up-converts the baseband signal generated by DAC with the local oscillator source, and the output signal of modulator is amplified by a three-stage amplifier. Reception module receives the RF signal through the circularly polarized antenna, amplifies the echo signal by a low noise amplifier, then down-converts with the local oscillator source to get I/Q signals, these I/Q signals is amplified and filtered by the variable gain amplifier and low-pass filter for baseband processing. The system is designed to be one-path transmission and three-path reception. The three-path reception link can make the obtained data more accurate. For simplicity, only one reception-path is shown here. All reception-paths are consistent in structure.

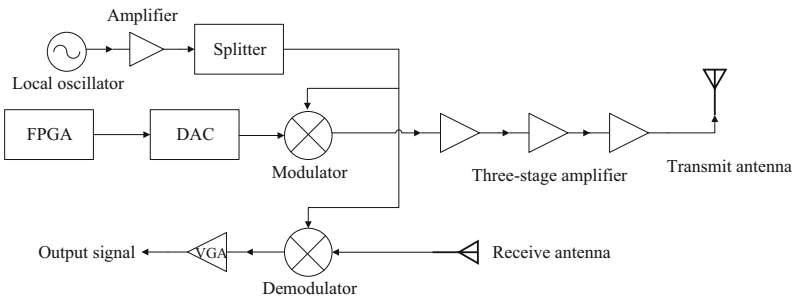

Fig. 1. System structure diagram

3 Circuit Design

3.1 DDS Module Design

The DDS structure diagram is shown in Fig. 2. The DDS module selects AD9914 chip of Analog Devices (ADI) as local oscillator source, the chip can be driven by a 3.5 GHz external clock frequency and have the fast frequency hopping feature [11]. It can generate stable signal that satisfies the operating frequency range. In this system, the AD9914 is controlled by the FPGA chip.

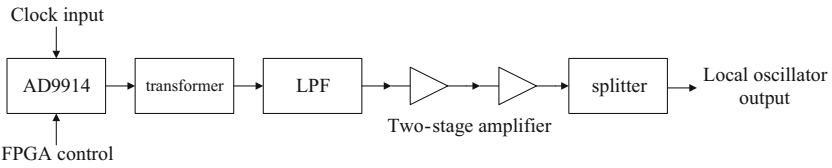

Fig. 2. DDS structure diagram

The differential signal generated by the DDS chip convert to single-ended output by the RF transformer structure, and a low-pass filter is cascade to filter out the out-of-band noise through. This module needs to provide local oscillator for the transmission module and multi-channel reception module. The output of DDS is amplified by two-stage amplifier to satisfy the frequency mixer input power requirements of local oscillator.

3.2 Transmission Module Design

The transmitter structure diagram is illustrated in Fig. 3. The main control chip of this module is EP3C16Q240C8 N (Altera's hurricane triple-series FPGA chip), AD9122 is the DAC (Digital to analog converter) chip of ADI, AD9156 is the clock chip of ADI. The FPGA chip controls AD9516 to generate the desired clock frequency for DAC chip. FPGA controls the DAC internal register through a 16-bit differential cable, the digital signals received by the input-end are converted into analog signals. The modulator mixes the output signals with the local frequency source and then pass a three-stage amplifier. The three-stage amplifier includes the RF gain module, the RF digital control VGA (Variable Gain Amplifier), the RF amplifier. As the required transmit power is large, multistage amplifier circuit needs to be designed. However, the input signal of the third stage amplifier has power limitation, so the second stage amplifier adopts digital control VGA. If the second level amplifier's output signal power exceeds the input power rating of the next stage amplifier, it can be attenuated by the FPGA chip.

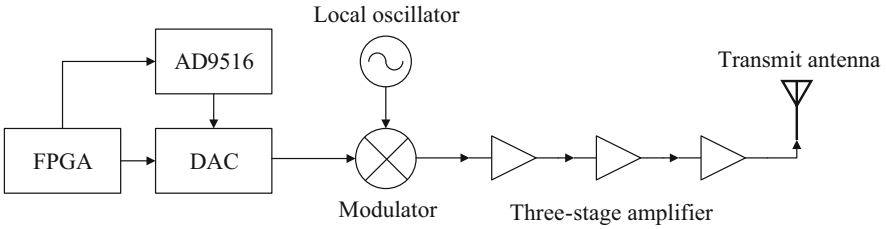

Fig. 3. Transmitter structure diagram

3.3 Reception Module Design

The receiver structure diagram is shown in Fig. 4. This module receives the echo signals through the circularly polarized antenna, performs the primary power amplification by the low-noise amplifier to control the noise coefficient of reception link. Then the I/Q signals can be obtained by down-conversion with the local oscillator frequency source, the output powers of the demodulator output signals can be adjusted by VGA chip. Then the signals pass through the low-pass filter and for processing.

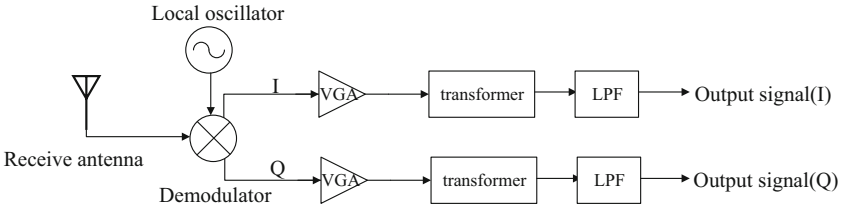

Fig. 4. One of the receiver structure diagram

4 System Test Results

Figure 5 shows the system test environment and Fig. 6 shows the hardware platform.

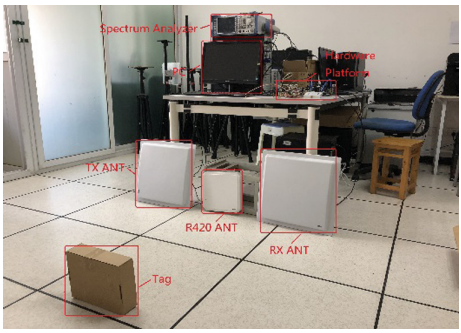

Fig. 5. System test environment

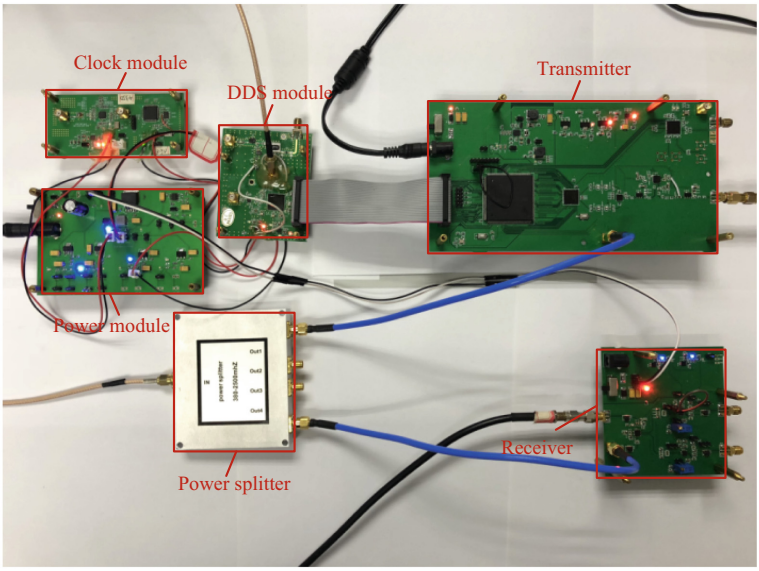

Fig. 6. Hardware physical picture

4.1 Transmitter Test Result

The transmitter uses the local oscillator to up-convert with the signal generated by ADC, then the amplified signal is transmitted to the air through the antenna. The output power of the transmitter in the bandwidth of 700 MHz to 1 GHz is shown in Fig. 7, and the spectrogram of output power near 900 MHz is shown in Fig. 8. The result shows that this transmitter has good performance within the entire operating frequency range.

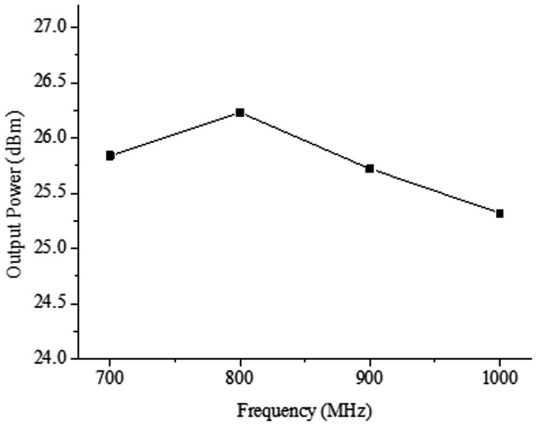

Fig. 7. Transmitter output signal power

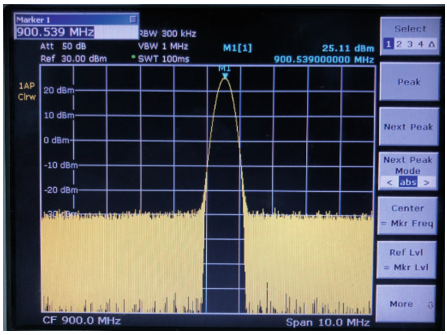

Fig. 8. Output power near 900 MHz

4.2 Receiver Test Result

The signal received by antenna is down-converted with the local oscillator, and the output power can be adjusted through the VGA. Figures 9 and 10 show the measurement results of the receiver with different VGA gains. The obtained signal center frequency is 4.246 MHz, and the output powers of the signals are −10.95 dBm and −1.18 dBm.

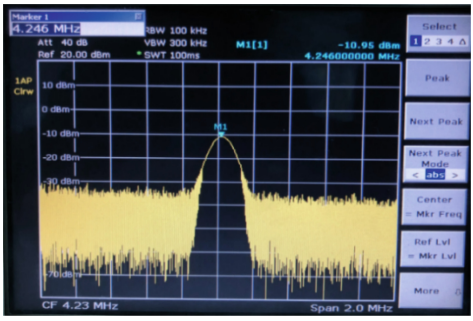

Fig. 9. Baseband amplifier output power

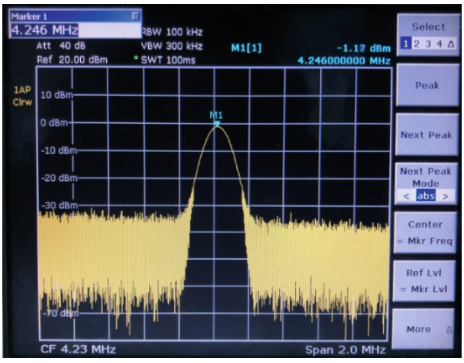

Fig. 10. Baseband amplifier output power

5 Conclusion

This paper designs a UHF RFID transceiver front-end based on discrete components, which utilizes the advantages of DDS technology for fast frequency switch and multi-frequency point output. Using the fast frequency hopping technology in a wide bandwidth of DDS, the system can achieve a high accuracy and high stability local oscillator signal output. The measured results show that the system basically satisfies the design requirements of UHF RFID transceiver front-end for localization, which verifies the correctness and rationality.

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