Test Scheduling of Interposer-Based 2.5-D ICs Using Enhanced Differential Evolution Algorithm

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Abstract. Interposer-based 2.5-dimensional integrated circuits (2.5D ICs) are seen as an alternative choice and they are rising as a precursor toward 3D integration. However, as the number of dies embedded in the interposer increases, the efficient test of 2.5D ICs becomes more difficult. In the design of test wrapper and test scheduling, both the test-time and the hardware cost have to be take into account. This paper presents an innovative differential evolution algorithm with dynamic subpopulations and adaptive searching strategy for the optimization of 2.5D IC test scheduling and hardware cost control. The whole population are partitioned into subpopulations dynamically using affinity propagation based clustering algorithm. In the subpopulations, a new mutation scheme which is controlled automatically by fitness values and distances between individuals is also presented. Parallelism among subpopulations and the proposed adaptive mutation and rotation crossover strategy can increase the speed of evolution without losing population diversity. Test wrapper scan chain balance design and the test scheduling algorithm, which combine the DE variant algorithm show an excellent performance in optimization ability comparing with the integer linear programming formulation (ILP) and some other configurations. It can make a good balance between the hardware cost and the test-time cost.

Keywords: 2.5D ICs test scheduling · Adaptive mutation mechanism · Dynamic subpopulations · Test cost

1 Introduction

Integrated circuit technology is taking mankind to a better future at an unprecedented rate, and Moore's law, which has been recognized in academia and industry, is potentially and permanently changing our lives. With the increase of the scale of integrated circuits, the characteristic size of IC decreases continuously, while the size of interconnect wire does not decrease in the same proportion. Therefore, the integrated chip is becoming more and more crowded in the traditional two-dimensional (2D) environment, and the proportion of line delay in total delay increases rapidly. In an effort to meet the needs of microelectronics chip development, 3D technology, which can significantly reduce the bottlenecks in IC designs by using TSVs instead of the long global wires and vertically arranging the logic dies, is gradually emerging.

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However, due to some technical difficulties, the large-scale commercial production of 3D integrated circuit cannot be realized yet. Nowadays, interposer-based 2.5D ICs are emerging and becoming a good transition from 2D to 3D ICs [1].

In 2.5D ICs, the method of stacking multiple active dies vertically is not adopted. Dies are placed abreast on top of the silicon interposer and they are interconnected through the interposer. The silicon interposer can communicate different dies and connect dies with packages. With micro-bumps, the silicon interposer can make dies stack on it. Die-to-die and die-to-package are interconnected through the silicon interposer using TSVs. A number of metal layers of wires and the silicon substrate interposer are included in the interposer. Moreover, there are a cluster of TSVs that provide vertical interconnections between the dies and package in silicon substrate. The top of the silicon interposer are metal layers which can make different dies interconnect horizontally. The processes of fabricating interconnects in multiple metal layers of the interposer is as same as the processes of fabricating interconnects in the silicon dies. Today, high-density I/O ports can be used inside the interposer. Therefore, 2.5D integrated circuits can provide better performance while reducing power consumption [2].

2.5D integrated circuit testability design is an important means to ensure the reliability of its function and performance. The test structure of 2.5D IC consists of three parts: test access mechanism, test package and test scheduling. Due to the difference of design and integrated technology, 2.5D IC testing has new research contents and restrictive factors besides the problems often encountered in 2D testing [3, 4]. In this paper, we describe solutions for two of these challenges in detail, namely test wrapper test chain balance design and test scheduling.

The article is arranged as follows. The related prior work is presented in Sect. 2. Section 3 presents the proposed modified differential evolution algorithm. In Sect. 4, we will give a detail explanation of the test chains balance design. Section 5 presents the test scheduling algorithm for 2.5D ICs which is combined with the proposed DE variant. Simulation results are presented in Sect. 6. Section 7 concludes this paper.

2 Related Prior Work

No matter the 2.5D ICs test or the 3D ICs test, the final implementation is the IP core test. 2.5D IP core test package scan chain balance technology is one of the important methods to reduce the time cost and hardware cost and ensure the high efficiency of IP core test. The existing 2D IP core scanning chain balancing methods have been well developed, ILP algorithm and heuristic algorithm. The rectangular packing model has also been applied to the problem and made good performance [5–8]. However, considering the complex structure and different integration processes of 2.5D ICs, the test wrapper test chain balance methods of 2D ICs IP cores are no longer applicable. As for 3D ICs test wrapper test chain balance design, many attempts have been proposed. Some researchers consider TSV consumption and power consumption as the main factors of 3D scan chain balancing technology, respectively [9, 10]. Moreover, IEEE 1500 wrapper is expanded to 3D space in [11–13]. Some 2D ICs test chain balance algorithms, like BFD, FFD et al. are combined with some revise algorithms to solve problems in 3D ICs [14, 15]. Moreover, the ILP algorithm and heuristic algorithm are

also taken into consideration in [16]. However, few publications present algorithms related to 2.5D test package scan chain design. Moreover, comparing with 2D ICs test chain balances design, hardware costs like RDL and TSV consumptions have to be considered.

Due to the limitations of the test pins, conventional test methods is not feasible for the test of 2.5D ICs. In addition, as integration level increases, the test application time and test power consumption of 2.5D ICs increase accordingly. Thus, in the design of 2.5D IC testability, these factors must be taken into account. In order to reduce the test application time and meet the limits of power budget and fault coverage at the same time, a test scheduling and optimization technique for multicast is proposed [17]. Lu et al. combined several dies into one macro die which is connected to other dies to form a daisy chain for testing. At present, researchers have also made some progresses in 3D ICs test scheduling, where different restriction conditions are considered and several optimization methods are adopted [19, 20]. Considering the multilayer stacking structure of 3D integrated circuits, it is more common for many researchers to take temperature as a limiting condition for test scheduling [21]. Moreover, in [22], the physical location of IP core in SOC is taken into consideration and the routing overhead is seen as an important limiting condition. In terms of the optimization methods, the greedy algorithm, simulated annealing and other intelligent algorithms as well as the packing model have also been well applied [19, 23].

3 Modified Differential Evolution Algorithm

Differential evolution (DE), proposed by Price [24] and Storn et al. [25], has been proved to be an effective and simple method to solve optimization problems in practical applications. DE is arguably one of the most powerful and multifunctional evolutionary algorithms. Since its inception in 1995, DE has been successfully applied to diverse fields of real-world optimization problems. Moreover, DE has attracted extensive attention from researchers around the world resulting in a great deal of variants of the basic algorithm with improved accuracy, computational speed, and robustness.

3.1 The Conventional Differential Evolution Algorithm

The classical DE includes four main steps: initialization, mutation, crossover, and selection, and it only need 3 control parameters: the scale factor, the crossover rate and the population size. DE algorithm is a stochastic search method based on population of NP D-dimensional parameter vectors and it aims to minimize the objective function in continuous domains:

$$\vec{X}_{i,G} = \left\{x_{1,i,G}, x_{2,i,G}, \ldots, x_{D,i,G}\right\}, i = 1, 2, \ldots, NP \tag{1}$$

Where G ($G = 0, 1, \ldots, G_{\max}$) represents the evolution generation.

Initialization: The initial population is evenly randomized within the search range given the minimum and maximum bounds at the generation $G = 0$:

$$x_{j,i,0} = x_{j,\min} + rand_{i,j}[0, 1] \cdot \left(x_{j,\max} - x_{j,\min}\right) \quad (2)$$

where $rand_{i,j}[0, 1]$ is a uniformly distributed random number ranging from [0, 1].

Mutation: After initialization, a mutant vector $\vec{V}_{i,G} = \left(v_{1,i,G}, v_{2,i,G}, \ldots, v_{D,i,G}\right)$ is created responding to each population member of target vector $\vec{X}_{i,G}$ in each generation. There are diverse methods for the selection of parents in DE families and the most frequently referred mutation strategy is:

$$\vec{v}_{i,G} = \vec{x}_{r1,G} + F \cdot (\vec{x}_{r2,G} - \vec{x}_{r3,G}) \quad (3)$$

where the exponents *r1*, *r2*, and *r3* are different integers randomly selected from the set $\{1, 2, \ldots, NP\}$ and they are all different from *i*. Parameter *F* is called scaling factor.

Crossover: There are two kinds of crossover methods: exponential and binomial, in which binomial is more popular.

When the randomly generated number between [0, 1] is less than or equal to the *Cr* value, it is performed for each *D* variable. In this case, the number of parameters inherited from the donor has a (nearly) binomial distribution. Formulations below give an explanation of the scheme:

$$u_{j,i,G} = \begin{cases} v_{j,i,G} & \text{if } (\text{rand}_{i,j}[0, 1] \leq Cr \quad \text{or } j = j_{rand}) \\ x_{j,i,G} & \text{otherwise.} \end{cases} \quad (4)$$

Where, $i = 1, 2, \ldots, NP$, $j = 1, 2, \ldots, D$, and $rand_{i,j}[0, 1]$ is a uniformly distributed random number lying between 0 and 1 which is generated for each *j*, $jrand \in [1, 2, \ldots, D]$. And it is a randomly selected index, which ensures that $\vec{U}_{i,G}$ gets at least one component from $\vec{V}_{i,G}$. It is instantiated once for each vector per generation. The crossover rate $Cr \in [0, 1]$ is the probability of the event that a component of the trial vector will be inherited from the donor vector.

Selection: The one-to-one competition based selection operator between the target vector and trial vector are formulated as follows:

$$\vec{X}_{i,G+1} = \begin{cases} \vec{U}_{i,G}, & \text{if } f\left(\vec{U}_{i,G}\right) \leq f\left(\vec{X}_{i,G}\right) \\ \vec{X}_{i,G}, & \text{otherwise.} \end{cases} \quad (5)$$

3.2 The Modified Differential Evolution Algorithm

In terms of the mutation strategy of standard DE, on the one hand, the traditional operation of multiplying the difference vector with the scaling factor results in poor local search ability. On the other hand, for multimodal functions, we want to separate

out as many peaks (or minimum values) as possible, and search around these peaks or minimum values to increase the search rate, accuracy, and probability of finding a global optimal solution. Based on the above consideration, we raise an innovative differential evolution algorithm with dynamic subpopulations and adaptive searching strategy. The improvement of mutation operation is divided into two parts: subpopulation partition and adaptive mutation strategy.

Subpopulation Partition. The whole population is partitioned into subpopulations dynamically using affinity propagation based clustering algorithm. Messages between data points are passed between individuals in the population until a high-quality set of centers and corresponding clusters gradually emerges.

Adaptive Mutation Strategy. In the subpopulations, a new mutation scheme which is controlled automatically by differences of fitness values and distances between individuals is also presented. Parallelism among subpopulations and the proposed adaptive mutation strategy can increase the speed of evolution without losing population diversity. For composition functions and multimodal optimization, the affinity propagation based clustering method can be used to divide the whole population into several non-overlapping groups. The subpopulation only needs to search around one or a small number of optima and the searching accuracy will be improved dramatically. Moreover, the proposed mutation scheme can be easily applied to mutation strategies of several other variants of DE with small changes. Formulations of the revised mutation scheme are presented as follow:

$$\vec{V}_{i,G} = \vec{X}_{i,G} + S \cdot sym \cdot \left(\vec{X}_{r0,G} - \vec{X}_{i,G}\right) \tag{6}$$

Where S is the individual adjustment distance within the population and *sym* is a symbol denoted to indicate the adjustment direction of the individuals. The adjustment distance S can be described in the following formulation:

$$S = 0.5 + \frac{K}{2K_{\max}} \cdot 0.5 \tag{7}$$

Where $K_{\max}$ represents the maximum value in the array K, and the range of S is [0.5, 0.75]. K is the adjustment step controlled by individual fitness difference and distance in a group, of which the formulation is presented as follows:

$$K = \frac{\left|f\left(X_{r0,G}\right) - f\left(X_{i,G}\right)\right|}{\frac{1}{sNP}\left(\sum_{r=1}^{sNP}\left(f\left(X_{r,G}\right) - f\left(X_{i,G}\right)\right)\right)} \cdot \frac{dist_{i,r0}}{\frac{1}{sNP}\sum_{r=1}^{sNP} dist_{r,i}} \tag{8}$$

$$dist_{i,r0}\left(\vec{X}_{i,G}, \vec{X}_{r0,G}\right) = \sqrt{\sum_{j=1}^{D}\left(\vec{X}_{i,j,G} - \vec{X}_{i,j,G}\right)} \tag{9}$$

As for the conventional crossover strategy, in the situation where most of the target vectors are similar, difficulties are encountered in finding the search location for the loss of population diversity. On this basis, we try to overcome the defects of the standard binary crossover operator and propose a rotating crossover operator based on multi-angle searching strategy. The program tactically expands the search space and effectively guides the optimal evolution of the population to the overall situation, thereby preventing the population from generating disadvantaged individuals. The final expression for the improved mutation operation is as follows:

$$u_{i,G} = \begin{cases} \left(R_{i,G} \cdot \left(sym \cdot \left(v_{i,G} - x_{i,G}\right)/2\right)\right) + v_{i,G} & \text{if } (\text{rand}_{i,j}[0,1] \le Cr \quad \text{or } j = j_{rand}) \\ \left(R_{i,G} \cdot \left(sym \cdot \left(v_{i,G} - x_{i,G}\right)/2\right)\right) + x_{i,G} & \text{otherwise.} \end{cases} \tag{10}$$

Where G represents the current evolution generation. $R_{i,G}$ is the rotating control vector and the rotating radium decreases as the generation increases, which accelerate the convergence of late evolution. Detail information about the improved crossover scheme can be presented in [26]. Figure 1 gives a detail explanation of the proposed crossover operator. By multiplying the rotation control vector and the differential vector of the target and donor vector, trial vectors are generated in the elliptical region around the donor and target vector. The rotation angle and radius adjust with the modulus and angles of the rotation control vector.

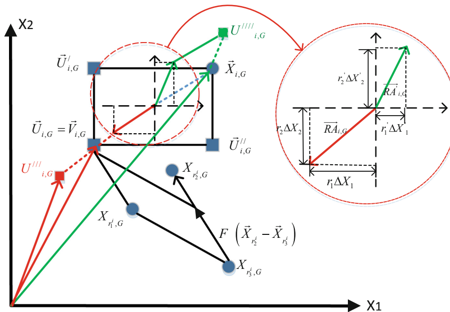

Fig. 1. Detail explanation of rotating crossover operator in 2-D space

4 Optimization Algorithm for Wrapper Scan Chains Balance

Both the 2D SoC and the 2.5D SoC test will eventually be implemented as the IP core test. In order to reduce the test time of a single 2.5D IP core, it is necessary to reduce the length of the longest test encapsulation scan chain in the IP core. 2.5D IP core test encapsulation scan chain balancing technology is one of the important methods to reduce the time cost and ensure the high efficiency of IP core test.

4.1 Scan Chain Balance Design in 2.5D IP Core Test Package

There are three cases of scan chain balance design in 2.5D IP core test package: the IP core is in a single die, the IP core and other IP cores are in one die and the IP core straddles multiple dieses. The first case is consistent with the traditional SoC in scanning chain balance design method; In the second case, it is easy to realize the balanced design of scan chain by drawing on 2D SoC scan chain balance design method and making comprehensive balance design for multiple IP cores with similar test vector data in the same die; For the third case, the balance of the scan chain is related to the number of RDL interconnects, which is the focus of this section. As shown in Figs. 2, 3 and 4 test chains in two dies need to be encapsulated into two scan chains.

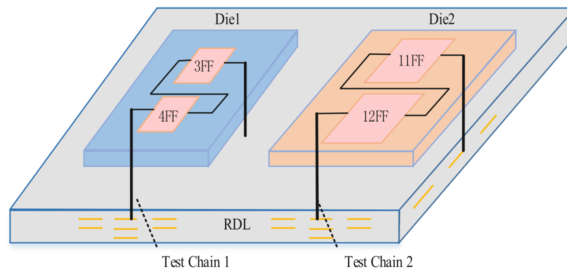

Fig. 2. Example of scan chain balance.

From Fig. 2 we can observe that two internal scan chains in each die are packaged into a scanning chain. It uses four RDL interconnects, with the length of the two scan chains is 7 and 23, respectively.

Two inner scan chains in different dies are packaged into one test chain, and it consumes 8 RDL interconnects with two test chains whose length are all 15 in Fig. 3. The scanning chain balance is realized with the additional 4 interconnections RDL.

In this paper, the proposed differential evolution algorithm is used to assign the best wrapper scan chains and realize the co-operation between the overall test time and hardware overhead.

4.2 Mathematical Model of Wrapper Scan Chain Balance Problem

We assume that the 2.5D IC is consisted of N Dies and M cores namely C_i ($i = 1, 2 \ldots M$). The automatic test equipment (ATE) can provide the maximum bandwidth W_m which can be divided into P parts. The width of each part is known, namely W_k ($k = 1, 2 \ldots P$) is given. CT (C_i, W_j) indicates the test application time for core C_i on the bandwidth W_j. The goal is to determine the cores' allocation for a given width of TAMs, thereby minimizing the total cost of SOC testing, including time and hardware costs. In general, the formula for packaging the scan chain balance problem is as follows.

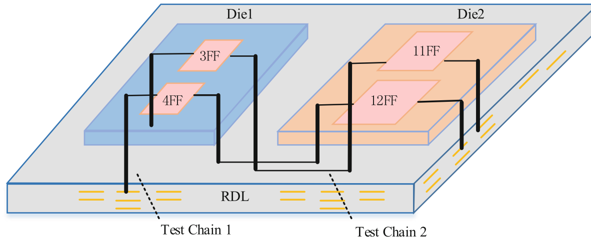

Fig. 3. Example of scan chain imbalance.

The objective function: minimize the maximum value of CT(j), which is the fitness function.

$$
\begin{aligned}
& x_{i,j} = \begin{cases} k & \text{core } C_j \text{ assigned to width } w_k \\ 0 & \text{otherwise} \end{cases} \\
& CT(i) = \max(L_{i,k}) + HC
\end{aligned}
\tag{11}
$$

Where HC represents hardware connection RDL consumption, $\max(L_{i,k})$ denotes the length of the longest scan chain and the goal of the optimization is to make a balance between test chain balance and hardware consumption so that the test costs can be minimized. The proposed differential evolution algorithm is used to make the best arrangement of the cores in each die to the given test chains. The matrix X represents the possible solutions to the problem.

$$
X_{i,j} = \{x_{i,1}, x_{i,2}, x_{i,3}, \cdots, x_{i,M}\}, i = 1, 2, 3, \cdots, NP \tag{12}
$$

Where NP is the number of individuals and it also represents the solution number of this problem. $X_{i,j}$ is integer coding ranging from 1 to P, which represents which scan chain these cores belong to. Thus, the initialized result is integer coding rather than real coding. Considering that after mutation and crossover operation, the value of each individual will be real coding, an integer function is needed to convert the real number to an integer. Table 1 gives an example of the integer conversion function which convert real numbers to integers ranging from 1 to 3.

Table 1. The integer conversion function.

Function [x_{int}]= integer(x_{real})
1.Input x_{real};
2.Step=1/3(max(x_{real})-min(x_{real}));
3.x_{int}=zeros;
4.d1= x_{real}<min(x_{real})+Step;
5.d2=(x_{real}<=min(x_{real})+Step&x_{real}<min(x_{real})+2Step);
6.d3= x_{real}>=min(x_{real})+2Step;
7.x_{int}=d1.*ones(NP,Dim)+2d2.*ones(NP,Dim)+3d3.*ones(NP,Dim);
8.return x_{int};

In terms of the fitness evaluation of the individuals, integers representing different scan chains need to be separated to calculate population fitness.

5 Test Scheduling and Optimization

5.1 Test Scheduling Problem

Along with the number of dies embedded in the interposer increases, test scheduling of dies are drawing attention of researchers. In the case that dies are tested in sequence, only one test architecture is needed for the test. In this case, the total test length will be unacceptably high for die testing will be the sum of test lengths of each die. However, if all dies are tested in parallel, the test time will be the test length of the longest die. While the test hardware cost will be very high because every die need to be equipped with the test architecture. Moreover, in the case that all dies are tested simultaneously, it is easy to exceed the power limit. Thus, both the test-time and hardware cost should be taken into account during the die test scheduling design. Hence, multiple test chains are adopted and each test chain has one test structure. Dies arranged in the same test chain have to be tested sequentially [1].

5.2 Mathematical Model of Test Scheduling Optimization

The mathematical model of test scheduling optimization can be described as follows: Given M dies stacked on the interposer of a 2.5D IC, and the cost of test per unit time be a. In addition, assuming that the cost of one test architecture is b, the maximum power that the 2.5D IC can support is P_{max}. The test power consumed by the die is denoted as P_i. Each test chain includes multiple dies, so each die is included in one test chain and the consolidation of all test chains includes all dies. For parallel test dies, their consumption of test power should be under the upper limit. Our goal is to make an optimal configuration that minimizes the cost of the entire test:

$$C=a \cdot \sum_{j=1}^{n} T_j + b \cdot N \tag{13}$$

$$b = area_{BIST} \cdot \cos t_{die} \tag{14}$$

Where variable N and n are respectively the number of test chains and test groups.

6 Simulation Results

The test wrapper scan chain balance design and the test-chain scheduling and optimization problem was solved using MATLAB R2014a.

6.1 Simulation of the Test Wrapper Scan Chain Balance Design

In this part, the balance results for the cores in each die stacked on the interposer are presented. The following describes the experimental results of the ITC'02 SoC benchmark. We chose SoC d695 from Duke University for experimental verification.

Table 2. Scan chain balance results for the test cases.

Die	DE		P1		P2	
	L_{Max}	Cost	L_{Max}	Cost	L_{Max}	Cost
Case 1	**3203**	**3221**	3224	3242	4439	4457
Case 2	**3191**	**3209**	4636	4642	3718	3736
Case 3	**3186**	**3204**	3511	3517	3794	3812
Case 4	**3194**	**3212**	4153	4159	3453	3471
Case 5	**3184**	**3202**	3223	3229	3424	3442
Case 6	**3194**	**3212**	3336	3342	3910	3928

In order to evaluate the above method, we proposed two different test-scan balance configurations. In the first case (P1), cores in the same die are assigned to the same test chain. In the second baseline, cores are randomly assigned to the scan chains. From Table 2 we can observe that scan chain balance design method combining the proposed DE algorithm can minimize the maximum length of test chains and the overall cost.

6.2 Test Scheduling Results

In this section, we will detail the scheduling results. Test lengths and power consumption of each die in test mode can be referred to [1]. The parameter $area_{BIST}$, which is the area of the intest BIST, is 993 μm^2; the parameter c_{die} is \$ $4.24 \cdot 10^{-8}/\mu m^2$ [27, 28]; and the test frequency f is 50 MHz

In these experiments, we also took three baselines. In the first case (B11), each die is assigned to different test chains so that all dies can be tested in parallel. However, dies have to be separated into groups because of the limit of P_{max}, and the dies in each group are tested concurrently. In the second case (B12), all dies on the interposer are tested in sequentially in one test chain. Moreover, the ILP algorithm for test scheduling proposed in [1] is also taken into comparison. In these configurations, the test time of B11 is the shortest, but the hardware cost is the largest, and the hardware cost of B12 is the smallest, but the test time is the highest.

In the first baseline, four dies are stacked on a common interposer and there are eight smaller dies in the second baseline. The detail information of the dies can be obtained in [1]. In Table 3, dies on the same line are in the same test chain and commas separate the test groups. Moreover, dies on the two sides of character "||" are tested concurrently.

From Table 3 we can find that method B11 has the least cost of test time in both of the two cases because of its full parallel strategy. The proposed DE variant cost more time than method B11 while it can make a good balance between test time and

Table 3. Scheduling results for the test cases.

	DE Case1	ILP Case1	B11 Case1	DE Case2	ILP Case2	B11 Case2
Configuration	1,2 4,3	2,4 3,1	2‖3 1‖4	2,5,4 & 7 1,8,3 & 6	1,8,4 & 7 2,5,3 & 6	1 2‖4‖5‖6 3‖7‖8
Test time(s)	**0.206**	**0.206**	0.206	**0.031**	**0.301**	0.028
Test cost($)	**1115**	**1115**	1762	**238**	**238**	477

hardware cost. Considering the small number of dies in the experimental data, the DE algorithm can get similar results of configuration. However, when there are only 8 dies stacked on the interposer in the experiment, the computational speed of DE is 8 times that of ILP. As the number of dies increase, the superiority of DE algorithm compared with ILP algorithm will be more prominent.

Further comparison experiments are presented in Fig. 4. The range of P_{max} is from 2500 μW to 6500 μW, with an interval of 500 μW. The other parameter settings remain unchanged.

From Fig. 4 we can observe that as P_{max} increases, more dies can be tested in parallel and thus the total cost of the test decrease. Although the optimization results of ILP and DE are similar, the running time of these two algorithms is much different. With the value of P_{max} decreases, the optimization difficulty increases, and the calculation time of the ILP algorithm greatly increases.

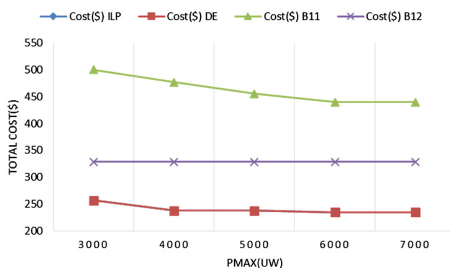

Fig. 4. Total cost with varying P_{max}.

7 Conclusion

In this paper, an improved differential evolution algorithm with dynamic subpopulations and adaptive searching strategy are proposed to solve the 2.5D IC test wrapper scan chain balance and test scheduling problem. The proposed DE variant which consists of adaptive mutation strategy and rotating crossover strategy can increase the speed of evolution without losing population diversity. Test wrapper scan chain balance design method and the test scheduling algorithm, which combine with the proposed DE algorithm show an excellent performance in both optimization ability and convergence rate.

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