Ultra Low Power Programmable Wireless ExG SoC Design for IoT Healthcare System

Mahesh Kumar Adimulam(✉) and M. B. Srinivas

EE Department, Birla Institute of Technology and Science – Pilani,
Hyderabad Campus, Hyderabad 500078, India
mahesh.kumar@ieee.org

Abstract. An 8-channel ultra low power programmable wireless ExG (ECG, EMG and EEG) system-on-chip (SoC) design for bio-signal processing applications is presented in this paper. The proposed design consists of a capacitive coupled programmable gain instrumentation amplifier (CC-PGIA) with an improved transconductance of amplifier. A 12-bit programmable hybrid SAR-Cyclic analog-to-digital converter (ADC) is introduced for improved performance and low power consumption that consists of a 6-bit SAR ADC (SADC) followed by a 6-bit cyclic ADC (CADC). The remaining blocks implemented in the SoC are programmable low pass filter (PLPF), programmable wireless transmitter (PWT), power management unit (PMU) and a digital block. The proposed programmable wireless ExG (PW-ExG) design is implemented in 180 nm standard CMOS process with a core area of 4 mm^2. The performance parameters are found to be, power consumption of 286 μW @ 0.6 V supply voltage, input referred noise voltage of 0.96 μV_{rms} over 0.5 Hz–1 kHz range, gain of 30–65 dB and signal-to-noise-and-distortion ratio (SNDR) of 69.2 dB.

Keywords: PW-ExG (ECG, EMG and EEG) SoC · CC-PGIA
Cyclic-SAR ADC · Programmable wireless transmitter · Ultra low power
IoT healthcare system

1 Introduction

Technologies related to IoT have been developed recently to improve the interface between healthcare architectures and portable bio-medical systems [1]. The main advantage of IoT technology is that it enables real time monitoring of the patient's health by integrating wireless transmitting systems with, let us say, ExG signal processing circuits. In bio-medical signal processing applications, remote monitoring of signals such as electrocardiography (ECG), electromyography (EMG) & electroencephalography (EEG) through wireless is difficult due to challenges such as signal radius coverage meeting clinical requirements and designs that consume ultra low power, low cost and higher efficiency [2, 3].

In last two decades, significant amount of research has been carried out both at architectural level and circuit implementation for analog front end (AFE) and wireless transmitters [1–4] to improve the performance and power efficiency. The AFE consists of instrumentation amplifier (IA), PLPF and ADC. The operational transconductance

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amplifier (OTA) is the fundamental building block for IA design; different topologies of OTA such as folded cascode, recycling structure, and improved recycling structure [5] have been implemented to improve the ratio of transconductance. In this paper an improved transconductance amplifier with DC offset adjustment circuit is used in CC-PGIA to improve the performance such as common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) and input referred noise without increasing the power consumption and area.

The performance and power consumption of AFE also depend up on ADC sub-block while the ADC performance and power consumption are very critical in processing the bio-signals. Successive approximation register (SAR) ADC is most commonly used for bio-potential signal processing applications [6, 7] which at higher resolutions ($\geq$ 10-bits) has performance degradation due to capacitive mis-matches also power consumption increases significantly due to dynamic switching of the digital-to-analog converter (DAC). In this paper, authors introduce a hybrid SAR-Cyclic ADC for 12-bit operation with low power consumption and improved performance. The proposed SAR-Cyclic ADC overcomes the limitations of the conventional SAR ADC.

Apart from AFE, power consumption by the wireless transmitter is also significant in overall ExG SoC design. In this work, a low power wireless transmitter, operating in the unlicensed 2.4 GHz ISM band, has been designed following IEEE 802.15.4 specifications [8]. The power consumption of this transmitter is reduced by operating at lower supply voltage ($\sim$0.4 V) generated from the internal low power regulator and the power efficiency is improved by calibration.

The organization of this paper is as follows: Sect. 2 describes the architecture of the proposed PW-ExG SoC, Sect. 3 describes the circuit implementation, Sect. 4 presents the simulation results and finally Sect. 5 presents the conclusion.

2 Architecture of the Proposed PW-ExG SoC Design

Figure 1 shows the architecture of the proposed 8-channel PW-ExG SoC design. The operation of the single channel signal path from input electrodes to wireless transmitter output can be described as follows: the differential analog inputs $V_{INP, INM}$ are applied to CC-PGIA block through electrodes, the CC-PGIA circuit can be programmed for a gain of 30–65 dB with digital control bits based upon ExG input signal amplitude levels and the differential outputs of the CC-PGIA are given as inputs to PLPF which is a second order filter. The bandwidth of the PLPF can be programmed from 500 Hz–4 kHz with digital control bits based upon ExG signals operating frequency bands and the filtered outputs are given to the proposed 12-bit hybrid SAR-Cyclic ADC through 8 $\times$ 1 ADC MUX. The proposed SAR-Cyclic ADC can be programmed for 10-bit or 12-bit resolutions based on ExG signal amplitude level, the SAR-Cyclic ADC consists of 6-bit SAR ADC followed by 6-bit Cyclic ADC for 12-bit operation. The 12-bit SAR-Cyclic ADC converts analog input provided from PLPF to digital format. The digital data from ADC is post processed through digital block and transmitted over wireless transmitter, while the post processed digital data can also be displayed on display system for monitoring. The performance and power efficiency of the proposed PW-ExG SoC are

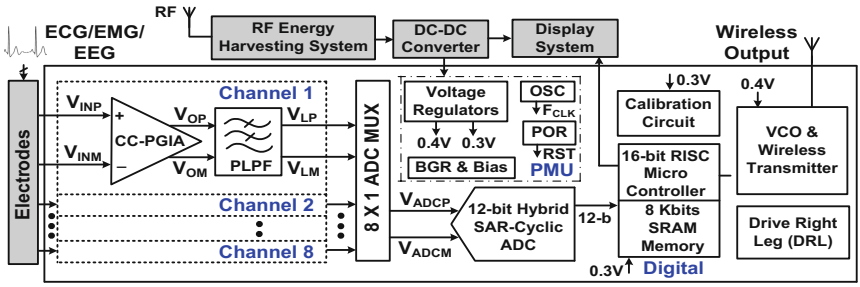

Fig. 1. Architecture of the proposed PW-ExG SoC design

improved by implementing an improved transconductance amplifier with DC offset cancellation and with proposed 12-bit SAR-Cyclic ADC.

The timing operation of the PW-ExG SoC design can be described as follows: the power-on-reset (POR) circuit generates RST signal with 10 mS delay after power supply ramp up while the PMU sub blocks settle within 50 mS time. The calibration circuit provides codes for signal processing path circuits within 15 mS. The analog front end (AFE) channel processes input signal in 12 mS while 12-bit hybrid SAR-Cyclic ADC converts analog input to digital format in 50 uS and the digital block performs post processing in 5 mS. Finally, the data is transmitted by the wireless transmitter which has a settling time of less than 0.5 ns.

3 Circuit Implementation of the PW-ExG SoC Design

3.1 CC-PGIA Design

Figure 2(a) shows the block diagram of the CC-PGIA design. The differential analog inputs $V_{EIP,\ EIM}$ are applied to CC-PGIA and the differential outputs $V_{OM,\ OP}$ are captured. The gain of the CC-PGIA design is given as $\Delta V = C_{IN}/C_F$, where C_{IN} is digitally programmable for the gain range of 30–65 dB based upon ExG signals amplitude levels and the ADC input dynamic range.

The improved transconductance amplifier with DC input common adjustment circuit is shown in Fig. 2(b). The transistors M_{1P}–M_{6P} & M_{3N}–M_{8N} form fully differential amplifier while the transistor M_{1N}–M_{2N} are implemented to improve the transconductance. These transistors are biased by M_{5R}. The transistors M_{1R}–M_{5R} adjust the input common mode voltage to V_R and this reduces the DC offset voltage due to electrodes. The transistors M_{1C}–M_{8C} forms the static CMFB circuit to adjust the output common mode voltage. The improved transconductance amplifier increases the DC gain, CMRR, PSRR and reduces the input referred noise voltage.

Table 1 shows the performance of CC-PGIA and a comparison with recent designs. Performance parameters are found to be CMRR of 122 dB, PSRR of 124 dB, input referred noise of 0.96 μV_{rms} and SNDR of 75.8 dB @ 500 Hz input frequency. Power spectrum analysis has been carried out to capture SNDR and Fig. 3 shows the SNDR to be 75.8 dB @ 500 Hz input frequency. The results demonstrate that most of the

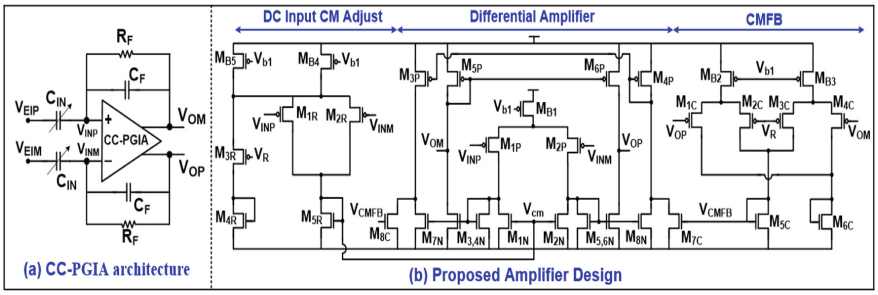

Fig. 2. Block diagram of CC-PGIA and proposed amplifier design

Table 1. Performance parameters comparison

	[9] 2012	[10] 2016	This work
Technology (nm)	180	180	180
Supply voltage (V)	0.6	0.5	0.6
Supply current (μA)	1.0	1.1	0.48
CMRR (dB)	>120	102	122
PSRR (dB)	>120	104	124
Input referred noise (μV_{rms})	5.41	1.32	0.96
SNDR (dB)	63.0	N/A	75.8

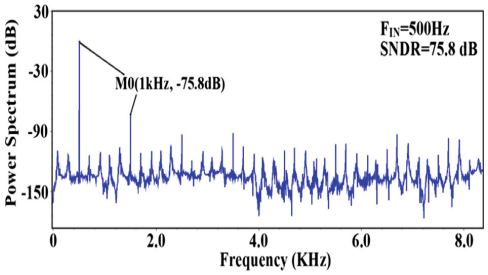

Fig. 3. CC-PGIA SNDR vs frequency

performance parameters are better than those of recent designs and highly suitable for bio-medical applications.

3.2 SAR-Cyclic ADC Design

In the proposed PW-ExG SoC design authors introduced a fully differential hybrid 12-bit SAR-Cyclic ADC to improve the performance and power efficiency. Figure 4 shows the architecture block diagram of the SAR-Cyclic ADC. The coarse ADC is implemented with 6-bit SAR architecture [6, 7] while the fine ADC is implemented

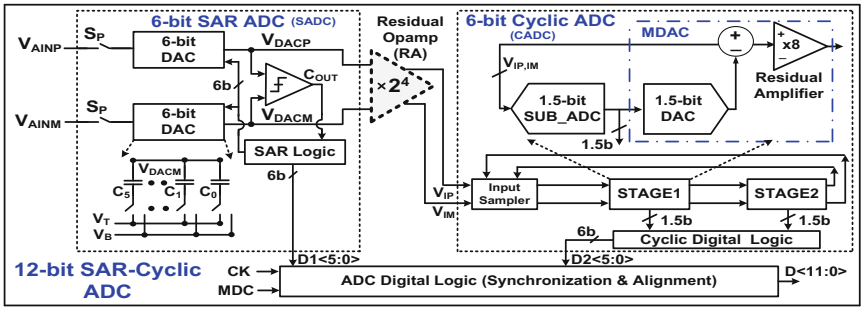

Fig. 4. Architecture of the proposed SAR-Cyclic ADC

with 6-bit cyclic architecture [11] and the integration of the both ADCs is carried out using residual amplifier [12]. The advantage of this architecture is that it reduces the capacitor mis-matches for improving performance and reduces the DAC switching logic for improving power efficiency in conventional SAR ADC at higher resolutions. The selection of Cyclic ADC for fine resolution is due to the requirements of lower sampling speeds, high performance and lower power consumption.

The functional description of the SAR-Cyclic ADC is provided as follows: the differential analog inputs $V_{AINP, AINM}$ are applied to coarse SADC which performs 6-bit operation and provides coarse digital output D1<5:0> to ADC digital logic. The error voltage from the SADC is amplified by a gain of 16 using residual amplifier (RA) which improves voltage dynamic range and provides output to fine 6-bit CADC. The CADC performs 6-bit operation and provides fine digital output D2<5:0> to ADC digital logic. The ADC digital logic performs data synchronization, error correction and combines D1<5:0> & D2<5:0> bits to provide a 12-bit D<11:0> digital output.

The circuit implementation of the 6-bit SADC is adopted from [6] and its performance is improved by reducing the capacitor mis-matches. The cyclic ADC architecture is adopted taken from [11] and designed at 0.6 V supply voltage while the RA circuit is fully differential-bias based inverter with common mode feedback (CMFB). The proposed ADC is programmable to 10-b mode (i.e., 5-b SADC and 5-bit CADC) using MDC control bit.

The performance parameters of the SAR-Cyclic ADC for both 10-b/12-b operation and comparison with recent designs are provided in Table 2. The design has a differential non-linearity (DNL) of ±0.4 LSB and integral non-linearity (INL) of ±0.51 LSB while among dynamic parameters, ENOB is found to be 11.24. Power spectrum analysis was carried out to capture SNDR, Fig. 5 shows an SNDR of 69.4 dB @ 500 Hz input frequency. Thus, it can be safely said that most of the performance parameters of the proposed ADC are better than those of recent designs and the ADC is highly suitable for bio-medical applications.

Table 2 Performance parameters comparison of the proposed ADC with recent designs

	[6] 2014	[7] 2015	[11] 2016	This work	
Technology (nm)	180	180	180	180	
Supply voltage (V)	0.6	0.6	0.9	0.6	
Architecture	SAR	SAR	Cyclic	SAR-Cyclic	
Sampling rate (KHz)	100	20	500	100	
Resolution (bits)	10	10	12	10	12
DNL (LSB)	0.5	0.46	±0.5	±0.34	±0.4
INL (LSB)	0.89	0.44	+3.2/−2	±0.42	±0.51
SNDR (dB)	57.14	58.34	62.68	58.7	69.4
ENOB (bits)	9.2	9.4	10.1	9.46	11.24
Power (W)	390n	38n	120µ	124n	308n
FOM (fJ/conv-step)	6.7	2.8	241	1.76	1.27

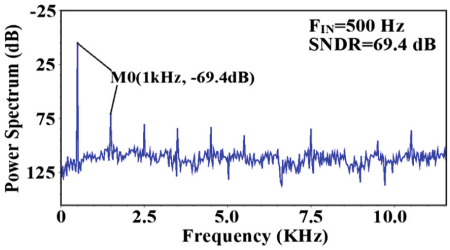

Fig. 5. ADC SNDR vs frequency

3.3 Low Power and Programmable Wireless Transmitter

In design of the wireless transmitter, the super-regenerative OOK transmitter architecture is used [3] following the IEEE 802.15.4 specifications. Figure 6(a) shows the programmable wireless transmitter block diagram where the voltage controlled oscillator (VCO) is designed with complementary cross coupled NMOS/PMOS structure and RF varactor capacitor is used for frequency tuning. Calibration is done to improve performance by controlling V_C voltage and aspect ratios of P[1–4] and N[1–4] devices. The power consumption of the circuit is reduced by operating on 0.4 V internal supply voltage. Figure 6(b) shows the TX output power spectrum at 2.4 GHz tuning frequency and output power is found to be −27.89 dBm compared to −16.36 dB in [3]. Power consumption of transmitter is 276.5 μW @ 0.4 V supply voltage.

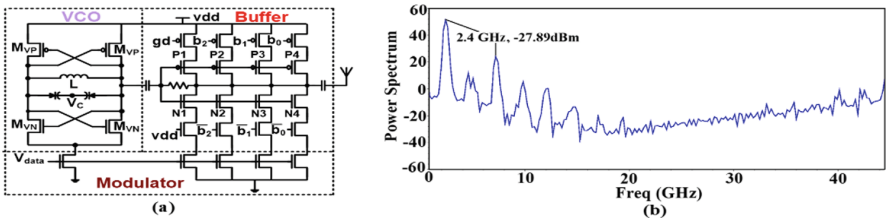

Fig. 6. (a) Block diagram of programmable wireless transmitter (b) Transmitter output spectrum

The PLPF block is designed with improved transconductance amplifier to improve the performance and remaining sub-blocks PMU [6], calibration & digital [3] are designed considering PW-ExG performance and power efficiency.

4 Simulation Results

In this section simulation results of the proposed PW-ExG SoC design are discussed. The proposed design is implemented in 180 nm standard CMOS process with a core area of 2 mm × 2 mm. The worst-case RC post layout simulations are carried out to capture the performance parameters at block level and PW-ExG top level. Figure 7(a) and (b) shows the ±3σ Montecarlo offset voltages for SAR ADC comparator and

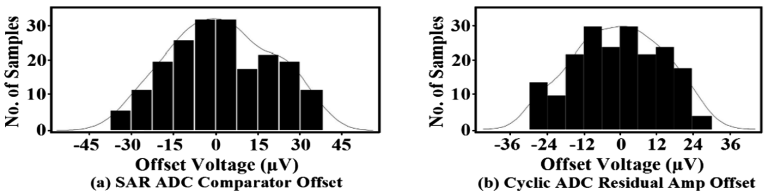

Fig. 7. (a) SAR ADC comparator offset voltage (b) Cyclic ADC residual amplifier offset voltage

Cyclic ADC residual amplifier. The SAR ADC comparator offset voltage is ±36 μV and the same for Cyclic ADC residual amplifier is ±30 μV. The variation of the offset voltages is reduced by one time calibration. Results show that the comparator and residual amplifier designs meet 12-bit accuracy.

Figure 8(a) shows the simulation setup to validate the results at receive end and Fig. 8(b) shows the data transmission bits at the input of the transmitter, output of the transmitter and output of the receiver model. Data from the PW-ExG SoC design is transmitted over antenna with 2.4 GHz carrier frequency. The Verilog-a model of receiver is built to capture the digital data, de-modulate and analog output is captured for performance analysis after filtering through programmable 12-bit ideal DAC. Results show that there are no data errors, meaning the transmitted data is recovered fully at the receiving end.

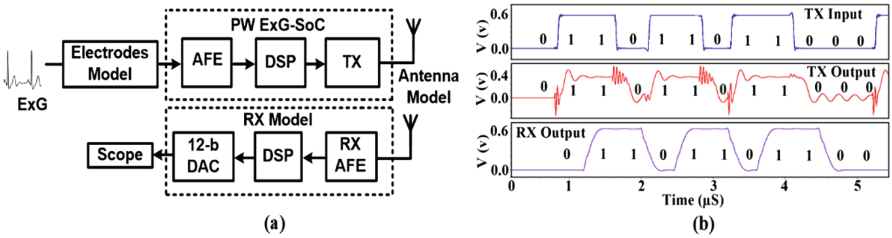

Fig. 8. (a) PW-ExG SoC simulation setup (b) Transmitter and receiver data pattern

The ExG signals are taken from [14, 15] and given as inputs to the 8-channel PW-ExG SoC and the results are captured at the output of the ideal 12-bit DAC. Results show SNDR @ 100 Hz input signal as 69.9 dB for ECG signals and at 500 Hz input signal is 69.2 dB for EMG signals. Figure 9(a) and (b) shows the ECG and EMG

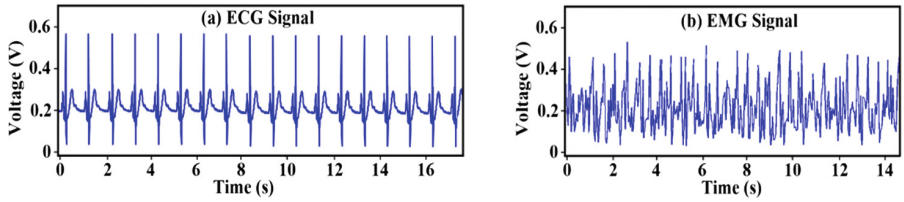

Fig. 9. ECG and EMG signals captured at the output of the Ideal DAC

Table 3. Performance parameters comparison with recent state of art designs

	[13] 2013	[4] 2015	[3] 2015	[2] 2016	This work
Technology (nm)	130	130	180	180	180
Supply voltage (V)	1.0	1.0	1.2	0.95	0.6
Sensor type	Neural, ExG	ExG	ECG	ECG	ExG
Number of channel (s)	1	4	1	1	8
AFE gain (dB)	42–78	40–78	20–28	34	30–65
Input ref noise (μV_{rms})	–	<2	–	16	0.96
ADC arch	8-bit SAR	8-bit SAR	12-bit SDM	8-b LC ADC	12-b SAR-Cyclic
TX data rate	100 kb/s	200 kb/s	5 Mb/s	90 kb/s	5 Mb/s
TX band (GHz)	0.433	0.433	2.4	0.402	2.4
TX O/P power (dBm)	−16.0	−18.5	−16.36	−16.0	−27.89
Power consumption (μW)	500 @ (100% duty cycled)	19 @ (0.013% duty cycled)	606 @ (50% duty cycled)	9.72 (-)	286 @ (50% duty cycled)
Area (mm)	2.5 × 3.3	3.3 × 2.5	1.52 × 1.55	1.9 × 2.0	2.0 × 2.0

signals captured at the output of the Ideal DAC. Table 3 shows the performance parameters of the proposed design and a comparison with recent state of art designs.

5 Conclusion

In this paper, a design of ultra-low power PW-ExG SoC for IoT healthcare system has been presented. It has 8-channels supporting various ExG signal amplitudes and frequency bands. Its performance is improved by CC-PGIA design, hybrid SAR-Cyclic ADC, PWT and calibration technique while the power consumption is reduced by operating on a 0.6 V supply voltage and sub-threshold region. The results in Table 3 show that most of the performance parameters are better than that of recent designs making the design suitable for bio-medical and IoT healthcare applications.

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