A Six-Segment SRRC Pulse Generator for IEEE 802.15.6 WBAN Standard

Babita Jajodia
babita@iitg.ernet.in

Anil Mahanta
anilm@iitg.ernet.in

Rafi Ahamed Shaik
rafiahamed@iitg.ernet.in

Department of Electronics and Electrical Engineering
Indian Institute of Technology Guwahati
Assam, India - 781039

ABSTRACT

A piece-wise linear approximated baseband Square Root Raised Cosine (SRRC) pulse and its up-conversion to IR-UWB WBAN (Impulse-Radio UWB Wireless Body Area Networks) channel in compliance to the IEEE 802.15.6 Standard is proposed. The baseband SRRC pulse is designed on a six-segment model. The proposed approximation conforms to the specified spectral mask at the mandatory low band channel at the central frequency of 4 GHz and having a bandwidth of 500 MHz. The key features of the proposed design is reduced hardware complexity due to the use of sampler based up-conversion circuitry followed by switched capacitor band pass filter. The circuit is designed using 0.18μm standard CMOS technology. The simulation results show that, the average energy consumption for generation of SRRC RF pulse is around 43.7 pJ/pulse.

Keywords

WBAN, IEEE 802.15.6 Standard, IR-UWB, SRRC, Pulse Generator

1. INTRODUCTION

Wireless Body Area Networks (WBAN) is expected to boost health monitoring systems providing affordable and reliable health-care technology for efficient service for all, ultra low power consumption and high data rate are the major requirements for the WBAN Technology [1]. Existing technologies like Wireless Personal Area Networks (WPAN) technologies i.e. Bluetooth and ZigBee when used for WBAN applications are prone to interference due to co-existence of other devices operating in the same band along with larger size and high power consumption. UWB technology is considered as an emerging technology for ultra-low power applications in WBAN due to its advantages over other narrowband technologies [1]. Hence, IR-UWB technology is the best suited candidate for WBAN applications [1].

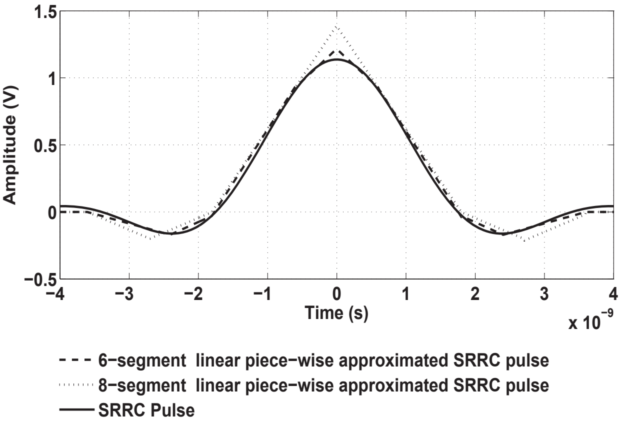

Figure 1: Piece-wise Linear Approximations of SRRC pulse

The pulse generator architecture [1] proposed for WBAN is realized using capacitor charging principle followed by up-conversion with multiplier. The IR-UWB pulse generators reported in literature are structured on conventional techniques using LC oscillators and mixers [2], and some on analog topologies [3, 4]. More recently, the extensive use of digital architecture has paved the way for ultra-low power consumption and reduced hardware complexity [2,5–8]. The pulse generation technique employed in [5] for generation of a raised cosine envelope introduces an all-digital architecture by use of pattern generator (PG) cells discarding the need for external filtering. However, the design has high complexity, high power consumption and a −10 dB bandwidth of 1.4 GHz. Although this technique generates a raised cosine pulse, but it does not meet the specifications of the standard making it unsuitable for WBAN applications. In this paper, we propose a low complex SRRC pulse generator and corresponding up-conversion of the signal suitable for IEEE 802.15.6 WBAN Standard.

2. PRINCIPLE OF OPERATION

The WBAN standard defines a few IR-UWB Pulses such as short SRRC pulse, chaotic pulse and the chirp pulse. Our target to design short SRRC pulse shape with the flexibility that the pulse generator can be used in both single and burst pulse modes of operation. The reference pulse specified in [10] for the selection of IR-UWB short SRRC pulse shape is shown in Fig 1. The SRRC pulse of Fig 1 is not a physically realizable waveform. Hence for practical realization in

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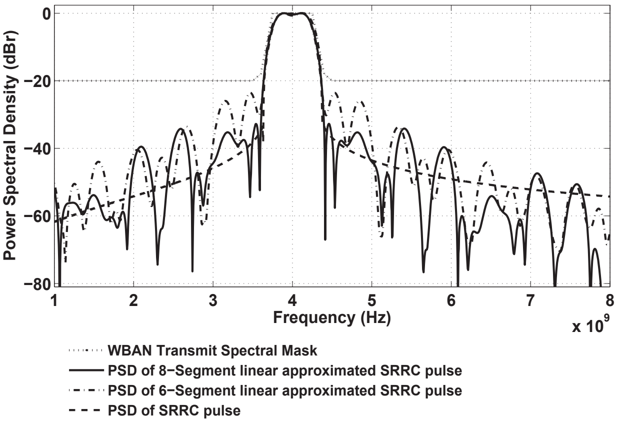

Figure 2: Power Spectral Density of the Up-converted piece-wise linear approximated Models of SRRC Pulse

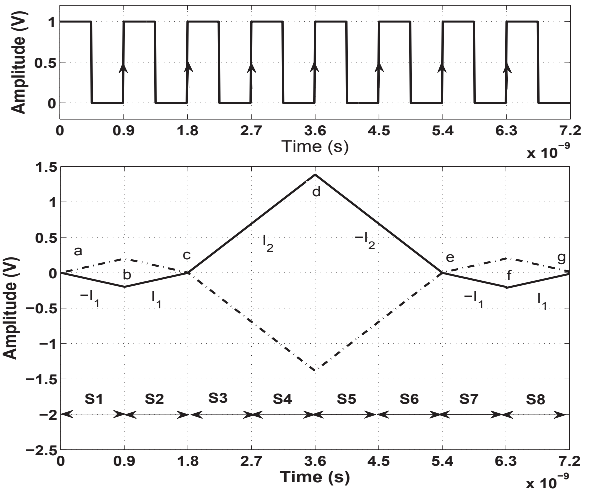

Figure 3: Piece-wise linear approximation of 6-segment SRRC pulse as function of states

standard CMOS technology, we first make a piecewise linear approximation of the pulse and consider the realization of the line segments as the voltages across an output capacitor charged by a sequence of controlled current sources of different magnitudes and polarity.

Simulations were carried out for a 6-segment and a 8-segment piece-wise linear models as shown in Fig 1. From the simulation results, one can infer that, even by closely approximating the pulse by increasing the number of segments, the power spectral density of the pulses is more or less invariant and closely follows the mandatory transmit mask in the main lobe while being well within the mask in the side lobes as shown in Fig 2. Keeping reduced hardware complexity in mind, it is found that the 6-segment model of SRRC pulse suits well for simple circuit level pulse realization.

3. PROPOSED DIGITALLY CONTROLLED PULSE GENERATION METHOD

The proposed digitally controlled pulse generation method is illustrated in Fig 3. For simplicity, we assume that the duration of each segment in Fig 3 as a multiple of some basic time duration T. Referring to the Fig 3, on a start signal, the controller enters the first state and starts discharging an output capacitor thereby generating the segment a-b (Fig 3). At the end of T, the controller enters next state where it disconnects the current source $-I_1$, connects the capacitor to the current source $+I_1$ and generates the segment b-c. In a similiar manner by switching the output capacitor to the appropriate current sources, all the six line segments (Fig 3) of the output waveform V_0 are generated in time $8T$. Simultaneously, the negated version V_{01} of the piecewise linear SRRC pulse is also generated as shown in Fig 3. The transition from one state to another is determined by the two triggering signals marked as V_{mos} and V_{switch} which determine the polarity and the magnitude of the current source respectively. Fig 4 shows the circuit realization of the six-segment SRRC approximation where V_0 and V_{01} respectively are the waveform representing the SRRC pulse and its negated version. A negative slope is realized by the discharge of C_0 through M_6 and M_5 while a positive slope is realized by the charge of C_0 through M_8 and M_7. This in turn, is effected by the control signal V_{mos} from the controller. The magnitude of this current (charging/discharging) in the current mirror is controlled by the gate voltage of M_3 (and M_5) which in turn is set to either V_1 or V_2 depending on the control signal V_{switch}. M_1 and M_2 are pass transistor to pass either V_1 or V_2. When $V_{switch} = 1$, V_1 is passed to the gate of M_3 and M_5. When V_{switch} =0, V_2 is passed. The values of V_1 or V_2 for a particular current in the current mirror is determined using the relation $I_{1,2} = C_0 \frac{\Delta V}{\Delta T}$ where, $I_{1,2}$ = Magnitude of the current (charge/discharge), $\frac{\Delta V}{\Delta T}$ = Magnitude of the slope of a particular segment and C_0 = Output Capacitor. The value of the bias voltage V_1 (or V_2) for realizing the current source I_1 (or I_2) can be obtained as $I_{1,2} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{1,2} - V_{th})^2$ where, $I_{1,2}$ = Magnitude of the current (charge/discharge), $V_{1,2}$ = Bias voltage V_1 (or V_2). The negated version of the SRRC approximation is obtained by a similiar circuit simply by driving the output MOS devices by a control signal V_{mos1} instead of V_{mos}.

4. SAMPLER BASED UP-CONVERSION

The motivation behind generating two pulses V_0 and V_{01}, the outputs of digitally controlled pulse generator is to obtain the up-converted version using sampler based up-conversion avoiding the use of analog multipliers. The circuit in Fig 5 based on simple MOS transmission gates alternately sample the baseband SRRC pulse and its negated version by a clock at the frequency 4 GHz to generate the rectangularly sampled and amplitude modulated RF pulse train.

5. SWITCHED CAPACITOR BAND-PASS FILTER

The rectangularly sampled amplitude modified pulse train obtained in the previous stage is passed through a band pass filter to meet the transmit spectral mask specifications of the pulse shape. The minimum bandwidth requirement specified in [10] of the up-converted baseband pulse at the mandatory low-band IR-UWB WBAN physical layer is 500 MHz at the central frequency of 4 GHz. The band pass filter is realized by cascading a high pass filter and a low pass filter. The low pass filter is designed for the upper cut-off frequency $f_{upper} = \frac{1}{2\pi R_1 C_2}$ where, f_{upper} = Upper cut-off

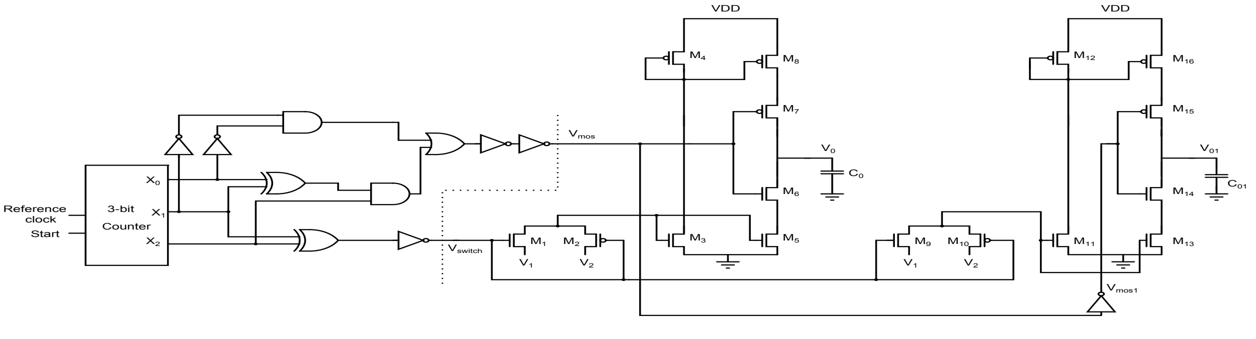

Figure 4: Digitally Controlled Pulse Generator

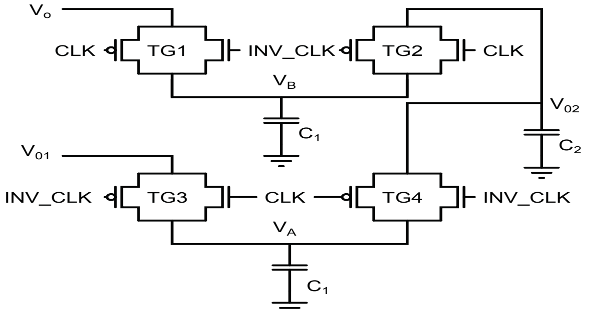

Figure 5: Sampler based Up-conversion Circuitry

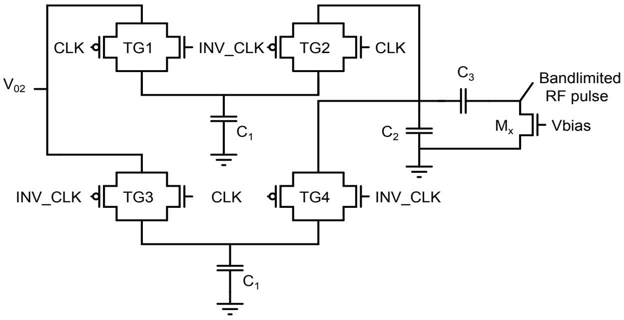

Figure 6: Switched Capacitor Band Pass Filter

frequency of the low-band mandatory IR-UWB channel = 4.25 GHz. The resistance, in turn, is realized using simple switched capacitor methodology. Based on this methodology, the resistance depends on the switched capacitor C_1 and the switching clock frequency f_{clk} as per the relation $R_1 = \frac{1}{f_{clk}C_1}$ The high pass filter is similiarly designed with a lower cut-off frequency specification of 3.75 GHz corresponding to the mandatory low-band IR-UWB channel as per $f_{lower} = \frac{1}{2\pi R_2 C_3}$ The high pass filter is realized by the series combination of a capacitor C_3 and a NMOS transistor M_x, the NMOS being biased suitably in the linear region to exploit its resistive action. The bias voltage is related to the resistance R_2 by the equation $R_2 = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{bias}-V_{th})}$ where, V_{bias} : bias voltage, V_{th} : threshold voltage, $(\frac{W}{L})_n$: Aspect ratio of NMOS transistor and $\mu_n C_{ox}$: Technology parameters of the MOS transistor.

6. SIMULATION RESULTS

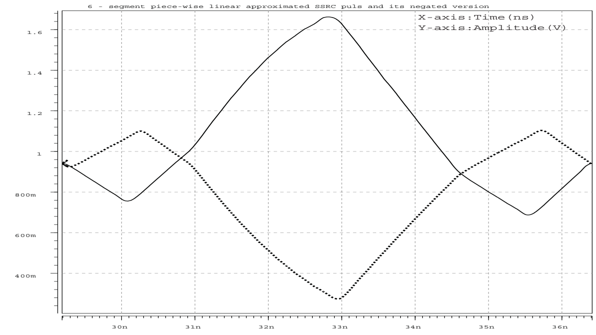

Figure 7: Simulated Baseband and and its negated 6-segment piece-wise linear approximated SRRC Pulse

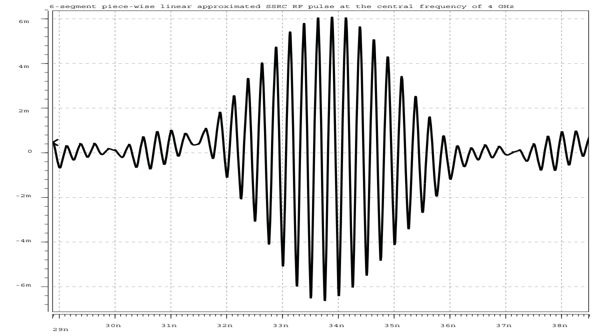

Figure 8: Simulated Up-Converted 6-segment piece-wise linear approximated SRRC Pulse at the central frequency of 4GHz

The proposed IR-UWB WBAN SRRC pulse generator circuit design is designed using 0.18μm standard CMOS technology. The circuit generated baseband SRRC pulse and its negated version is shown in Fig 7. The corresponding SRRC RF pulse is shown in Fig 8. Further, the normalized PSD of the simulated RF pulse is shown in Fig 9.

7. PERFORMANCE COMPARISON

It is difficult to directly compare each methodology employed for design of different IR-UWB pulse generators due to its implementation in different CMOS technologies and various specifications. Nevertheless, the performance of some of the reported IR-UWB pulse generators meeting some of the WBAN specifications is summarized in Table 1. The energy consumption per pulse is calculated as a figure of merit for the comparison of the performance of various IR-

Table 1: Performance Comparison of the Proposed IR-UWB WBAN Pulse Generator (Simulation Results) with Reported WPAN & WBAN Pulse Generators (Measured Results)

References	**Pulse Type**	**Up-conversion Methods**	**CMOS Technology/Supply Voltage**	**Pulse width/BW**	**Energy Consumption (pJ/pulse)**
[1]	Triangular pulse	Ring Oscillator	0.18μm /-	1 ns/0.5 GHz	65
[5]	Raised cosine pulse	Pattern Generator	0.18μm / 2.2 V	1.75ns/1.4 GHz	29.7 mW (for Tx)
[2]	Multi-cycle pulse	LC tank oscillator	0.18μm / 1.5 V	3.5ns/520 MHz	16.8
[9]	Multi-cycle pulse	All-Digital Oscillator (ADO)	0.13μm / 1.2 V	0.5 GHz	48
[8]	Multi-cycle pulse	Ring Oscillator	0.13μm / 1.1 V	0.5 GHz	32
[11]	Multi-cycle pulse	All-digital DLL	0.09μm / 1 V	550 MHz	47
Proposed Method	Square Root Raised Cosine pulse	Sampler based Up-conversion	0.18μm / 1.8 V	7.2ns/0.5 GHz	43.7

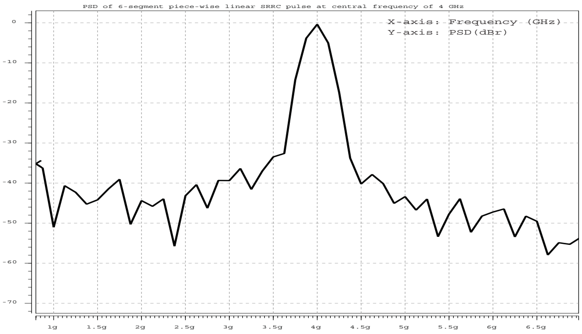

Figure 9: Simulated Normalized Power Spectral Density of 6-segment piece-wise linear approximated SRRC RF Pulse at the central frequency of 4 GHz

UWB pulse generators. The average energy consumption is nearly equal to 43.7 pJ/pulse. Although some of the IR-UWB pulse generators shown in Table 1 shows lower energy consumption, it is due to different CMOS technologies, bandwidth requirement and pulse duration. The average energy consumption of the proposed method makes this design efficient enough to be used for WBAN IR-UWB pulse generator meeting the specifications of the IR-UWB pulse shape specified in the IEEE 802.15.6 Standard for WBAN applications.

8. CONCLUSIONS

We have presented a low complex SRRC IR-UWB pulse generator required for WBAN applications and designed using 0.18μm standard CMOS technology. The simulation results show that, the pulse meet the specifications of the transmit spectral mask of the IEEE 802.15.6 standard. The proposed design has advantages over other reported pulse generator designs in terms of reduction in hardware complexity and low energy consumption. The average energy consumption is nearly equal to 43.7 pJ/pulse thus making it suitable for battery operated devices appropriate for WPAN and WBAN health monitoring systems.

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